uBGA's
Solder & Oven Profiles -- Critical Process Variables

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ABSTRACT

uBGA's and CSP packages have gained popularity over the past few years, and more and more designs are requiring these smaller package sizes in order to provide the highest package density possible while using the smallest amount of PCB real estate possible. The typical solder sphere size on a uBGA can range from .010" to .020" in size with a pitch range of less than .020" to .031". The pad sizes for a uBGA are typically one to one and therefore have the same size range as the uBGA solder sphere size. Printing and reflowing solder paste on pads of these sizes can prove to be challenging. Even the slightest process change, intentional or unintentional, in the wrong direction will narrow your process window, which will result in lower yields. This experiment was intended to evaluate the relative effects of two process variables affecting the test yields of a uBGA 16MB mini-card design. Historical test yields were anywhere from 50-80%. In addition, other uBGA designs were in the process of development, which would place further demands on manufacturing. It was imperative that the critical process variables affecting the first pass yields be identified and brought under control.

The process variables that were theorized to be affecting the first pass test yields were thought to be solder paste and oven profiles. These theories were developed based on previous experiments that had been performed. During FA and visual inspection solder joints as shown in Figure 1 were found and it was discovered that by simply refluxing and reflowing the module again, using the same oven profile, 90% of the failing modules would be repaired. During further FA a cross-sectioning analysis of a different uBGA module found an open solder joint. See Figure 2.

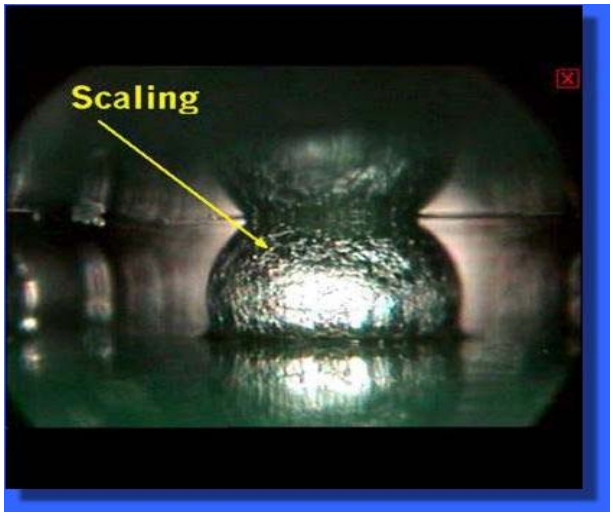


Figure 1
As Received
First row of Solder Spheres
Visual Inspection
Photograph @ 100x

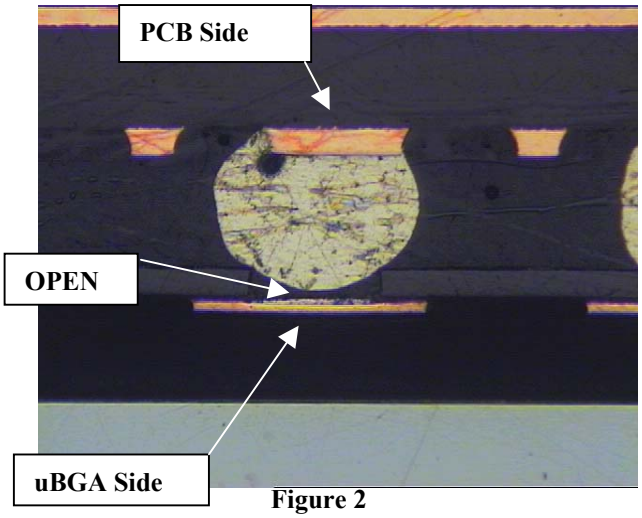


Figure 2
As Received
First row of Solder Spheres
Vertical Micro-section
Photomicrograph @ 140X

These findings led to the development of several theories. First it was theorized that an insufficient quantity of flux was being deposited with the solder paste and the oven profile TAL was too high, which was burning off all the flux activators. This in turn was leading to solder joints as shown in Figure 1. Second it was theorized that due to the size of the stencil apertures VS type III solder paste grain size, in some cases an insufficient amount of solder was being deposited during the stencil printing process. In turn this was resulting in open solder joints as shown in Figure 2. In order to validate these theory's a DOE was developed that would allow a comparative analysis of 3 different solder pastes and PPT (Precision Pad Technology or Solid Solder Deposit (SSD)) VS 2 different oven profiles.

Key Words: uBGA, solder paste, oven profiles, DOE

PRODUCT BACKGROUND

The uBGA 16MB mini-card design is a single sided thin PCB with a thickness range of .015" to .020". The final finish on the PCB's was gold flash, over nickel, over copper. The PCB array design was 1X6. The uBGA's used were Intel's 5V STRATAFlash uBGA memory device and there were 2 uBGA's per module. The uBGA's used had 56 solder spheres that were .012" in diameter with a .031" pitch, and the PCB pad geometry was 1:1. The product was assembled using standard type III water-soluble solder paste, a fully automated SMT manufacturing line, and an 8-zone convection oven. No AOI equipment was available for inspecting solder paste deposition, and solder paste height measurement was not possible due to the limitations of the solder paste height measurement system in plant. The stencil apertures for the uBGA's were .014" square

openings. The end use of the product is Internet routers, and is shown in figures 3 and 3A. Due to proprietary reasons this is all the background information that can be provided on the product.

FIGURE 3
Cased uBGA 16MB Mini-Card

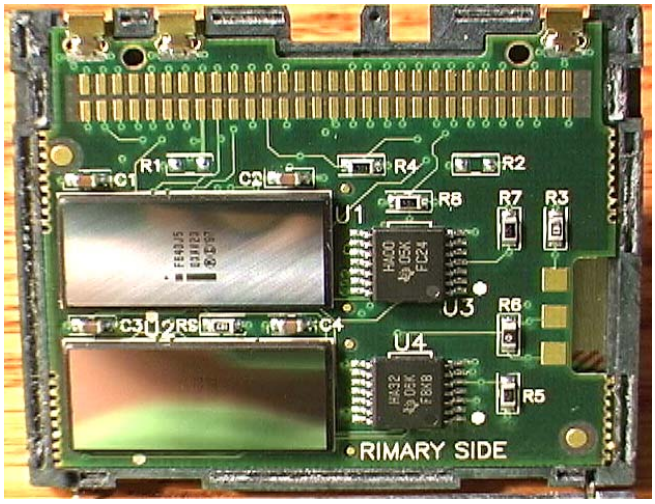


FIGURE 3A
Un-Cased uBGA 16MB Mini-Card

DOE DEVELOPMENT

Solder Paste

Three different OMG solder pastes were identified as candidates for use in the DOE analysis. These solder pastes were selected based on the current manufacturing processes. The "P3" solder paste is the standard type III solder paste that is currently used on all CCA's. The "P3A" solder paste is the same type III solder paste as the "P3", but with a more active flux. The "P4" solder paste is a type IV finer grain solder paste. The "PPT" is a patented solid solder deposit by MASK TECHNOLOGY, INC. MASK TECHNOLOGY gross prints and reflows the solder using a patented reflow machine. The end result of the PCB SMT land is shown in Figure 4. In the PPT case, we stencil printed OMG's water-soluble tack flux on the PCB, placed the components, and reflowed.

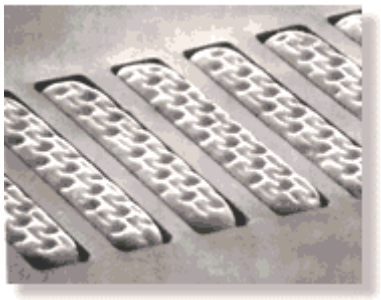


FIGURE 4
PPT PCB

Oven Profiles

Two different oven profiles were used. The first oven profile that was used was the "standard" oven profile, which was used on all products with a total mass density of 3.5 to 8.5 g/cm^3. The second "alternate" oven profile was developed based on a total mass density calculation under 3.5 g/cm^3. Extensive profile analysis for both oven profiles was performed to verify TAR (Time Above Reflow) and TAL (Time Above Liquidous). The "Standard" oven profile is shown in Figure 5, and the "Alternate" oven profile is shown in Figure 6.

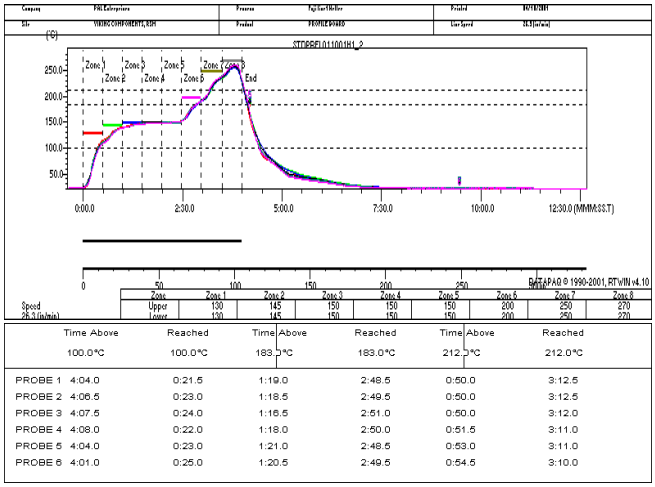
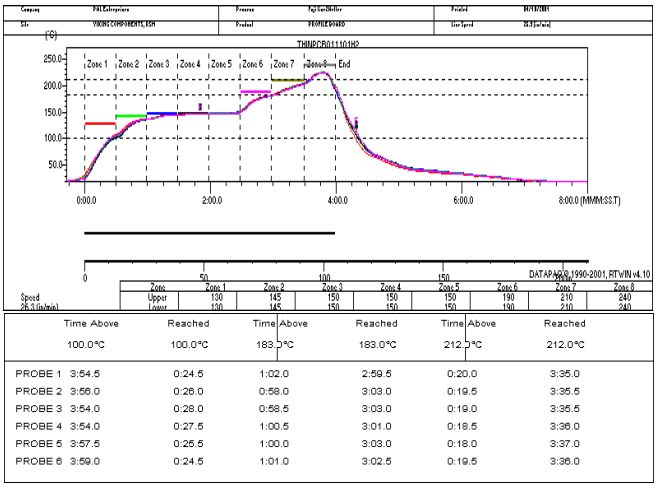


FIGURE 5
"Standard" Oven Profile



	Time Above 100.0°C	Reached 100.0°C	Time Above 183.0°C	Reached 183.0°C	Time Above 212.0°C	Reached 212.0°C
PROBE 1	3:54.5	0:24.5	1:02.0	2:59.5	0:20.0	3:35.0
PROBE 2	3:56.0	0:26.0	0:58.0	3:03.0	0:19.5	3:35.5
PROBE 3	3:54.0	0:28.0	0:58.5	3:03.0	0:19.0	3:35.5
PROBE 4	3:54.0	0:27.5	1:00.5	3:01.0	0:18.5	3:36.0
PROBE 5	3:57.5	0:25.5	1:00.0	3:03.0	0:18.0	3:37.0
PROBE 6	3:59.0	0:24.5	1:01.0	3:02.5	0:19.5	3:36.0

FIGURE 6
"Alternate" Oven Profile

When comparing the two oven profiles, one will find the zone settings differ only in the last three zones. Zone 6 in the "standard" oven profile is 200^0C and in the "alternate" oven profile is 190^0C. Zone 7 in the "standard" oven profile is 250^0C and in the "alternate" oven profile is 210^0C. Zone 8 in the "standard" oven profile is 270^0C and in the "alternate" oven profile is 240^0C. See Figure 7.

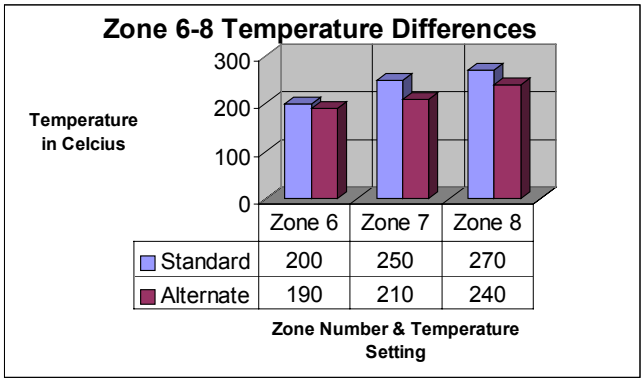


FIGURE 7
Zone 6-8 Temperature Differences

These changes in the last three zones of the oven resulted in lower TAL and TAR times for the "alternate" oven profile. The "standard" oven profile TAL had a minimum of 1:16.5 and a maximum of 1:21.0, while the "alternate" oven profile had a minimum TAL of 58.0 and a maximum of 1:02.0. The "standard" oven profile TAR had a minimum of 50.0 and a maximum of 54.5, while the "alternate" oven profile had a minimum TAR of 18.0 and a maximum of 20.0. See Figures 8 and 9.

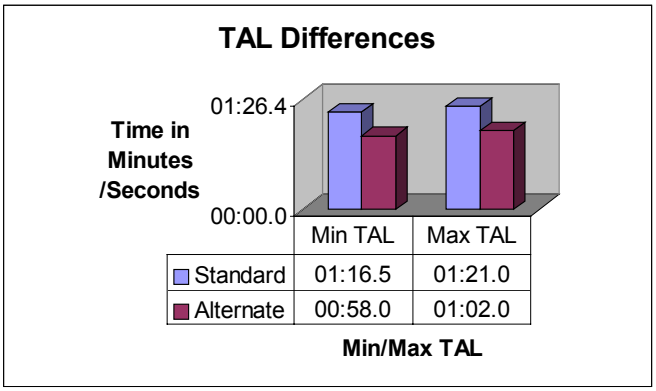


FIGURE 8
TAL Differences

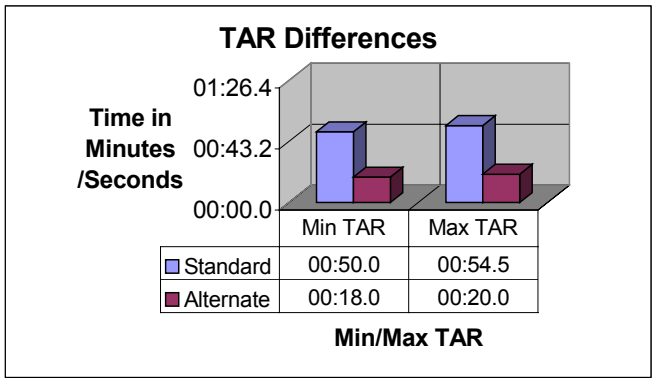


FIGURE 9
TAR Differences

DOE Analysis Outline
Based on the information stated previously the following DOE Analysis Outline was developed:

uBGA 16MB Mini-Card DOE

Purpose: To examine the theoretical variables thought to be affecting the manufacturing yield of the uBGA 16MB Mini-Card.

Three main factors will be controlled in order to determine their relative effect upon test yield. These main factors are PCB type, Solder paste type, Oven profile.

I. Experimental Factors

A. PCB Type
1. Regular (existing design for screened solder)
2. PPT (existing design with pre-deposited solid solder)

B. Solder Paste Type
1. P4 (Type IV finer grain solder)
2. P3 (Type III existing solder)
3. P3Active (Type III existing solder with a more active flux)
4. None (Tacky flux only on PPT PCB's)

C. Oven Profiles
1. "Standard Profile"- Existing oven profile. (TAL = 76 to 81 seconds)

2. "Alternate Profile" - New, cooler oven profile in three zones. (TAL = 58 to 62 seconds)

II. Experiment Matrix

Lot	Solder	PROFILE Std	PROFILE Alternate	PCB
A	p4	30 (A1)	30 (A2)	reg
B	p3	30 (B1)	30 (B2)	reg
C	p3Active	30 (C1)	30 (C2)	reg
D	tacky flux	30 (D1)	30 (D2)	ppt
	Total	120	120	

III. Serial Numbering

Lot	Solder	PROFILE Std	PROFILE Alternate	PCB
a	p4	**a1-a30**	**a31-a60**	reg
b	p3	**b1-b30**	**b31-b60**	reg
c	p3Active	**c1-c30**	**c31-c60**	reg
d	tacky flux	**d1-d30**	**d31-d60**	ppt

IV. Procedure

A. Sample lots shall be run as identified. The oven profile will be checked using a calibrated oven reflow analysis system before each run. Lot "a1-a30" will be set up and run with the Std profile. The oven profile will be changed to the new setting. The oven profile will be measured using a calibrated oven reflow analysis system to confirm. Then lot "a31-a60" will be run with alternate profile. Oven profile will be reset to Std, then verified using a calibrated oven reflow analysis system, then lot "b1-b30" will be run until all lots are ran.

B. All samples to be built in one shift.

C. All samples to be tested on the same day, same shift, and same tester.

D. Samples pulled from each lot and tested on router. N=4 each lot.

E. No samples to be reworked or altered by any one except experiment team.

F. Run experiment on one shift only, one line, one Test system.

V. Analysis of DATA

A. Data collected is pass-fail (attributes) data from Test, with confirmation from Internet routers.

B. Failed data from Test will be listed by output from Text (I.e. device ID fails, man ID fails, erase fails, pattern verification fail, etc.)

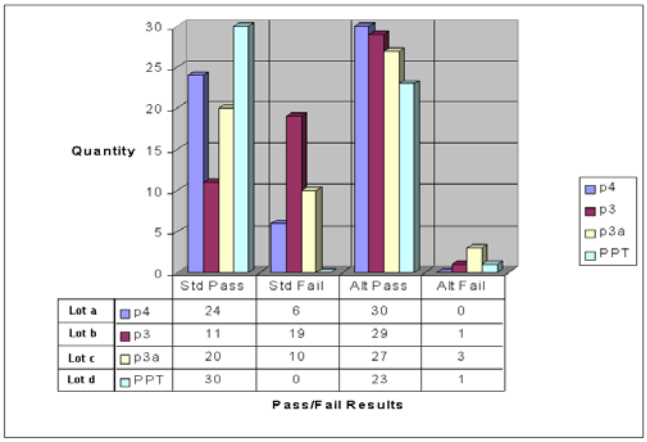
C. Failed units will be opened and inspected. Results will be listed. Induced damage will be noted. Failures due to handling damage or other induced damage will be removed from count of failures.

D. Chi-square to be used for analysis of pass-fail data. (Variable data is not being collected in this experiment - trace or ball resistance, shear strength, etc - so analysis cannot be done with ANOVA).

DOE ANALYSIS RESULTS

Overall DOE Analysis Results:

	Std Pass	Std Fail	Alt Pass	Alt Fail	Totals
p4	24	6	30	0	60
p3	11	19	29	1	60
p3a	20	10	27	3	60
PPT	30	0	23	1	54
Total	85	35	109	5	234



Note: The total quantity for the PPT Alternate was reduced to 24 due to a 6 up array being mishandled during the assembly process, which caused the uBGA's to misalign. The 6 pieces were removed from the analysis.

Failure Analysis

There were a total of 35 modules that failed in lot a, b, and c using the standard oven profile. After further investigation via x-ray and visual inspection it was determined that the repair process for 32 of the 35 modules would be reflux and reflow. All 32 modules passed functional test after performing this rework process. Three randomly selected modules, serial numbers a10, b1, and c2 were set aside for further root cause analysis. The results of this analysis will be presented in a follow-up report. See Table 1.

Lot	Solder Type	"Std" Fail	Qty Reworked & Passing	Module Selected for Root Cause Analysis	
Lot a	p4	6	5	a10	
Lot b	p3	19	18	b1	
Lot c	p3a	10	9	c2	
Lot d	PPT	0	0	N/A	
		35	**32**	**3**	**Total**

TABLE 1
"Standard" FA Summary

There were a total of 5 modules that failed in lot b, c, and d using the alternate oven profile. After further investigation via x-ray and visual inspection it was determined that the repair process for 2 of the 5 modules failing in lot c would be reflux and reflow. Both modules passed functional test after performing this rework process. The one module that failed in lot d had a missing component, and once the missing component was installed it passed functional test. Two randomly selected modules, serial numbers b60 and c60 were set aside for further root cause analysis. The results of this analysis will be presented in a follow-up report. See Table 2.

Lot	Solder Type	"Alt" Fail	Qty Reworked & Passing	Module Selected for Root Cause Analysis	
Lot a	p4	0	0	N/A	
Lot b	p3	1	0	b60	
Lot c	p3a	3	2	c60	
Lot d	PPT	1	1	N/A	
		5	**3**	**2**	**Total**

TABLE 2
"Alternate" FA Summary

Chi-Squared Test

Chi-square is a non-parametric test of statistical significance for the analysis of the degree of association between two variables. Any appropriately performed test of statistical significance lets you know the degree of confidence you can have in accepting or rejecting a hypothesis. Typically, the hypothesis tested with Chi Square is whether or not two different samples are different enough in some characteristic or aspect of their behavior that we can generalize from our samples that the populations from which our samples are drawn are also different in the behavior or characteristic. Due to the DOE test results being pass-fail; the attributes data can be analyzed using the Chi-Squared test to determine the confidence level that the analysis performed is repeatable. If the calculated χ^2 are large it indicates that actual data is nonrandom, and there is a high probability that the resulting data pattern shows a real, repeatable pattern. This in turn indicates that the association between the variables, as seen in the data, is real.

The two variables studied were solder type and oven profile. Raw data collected was test pass or fail. Subsets of the data were also analyzed. These subsets examined solder type versus Pass/Fail and oven profile versus Pass/Fail. For this test, the chi-square results indicate that there is a real, non-random pattern in the data. If the test were to be repeated, the chance of getting the same results is very high. The patterns in the data are:

1. PPT will have the highest yield of all the solder types.
2. Alternate profile will have higher yields than Standard profile.

Contingency Table of Results:

	Std Profile		Alt Profile		Std	Alt
	P	**F**	**P**	**F**	**Total Yld**	**Yld**
"a"P4	24	6	30	0	**60 80%**	**100%**
"b"P3	11	19	29	1	**60 36.7%**	**96.7%**
"c"P3A	20	10	27	3	**60 66.7%**	**90.0%**
"**d**"PPT	30	0	23	1	**54 100%**	**95.8%**
Total	**85**	**35**	**109**	**5**	**234**	
Yield	**70.8%**		**95.6%**			

Chi-Squared (χ^2) Values:

1. **Overall, Solder Type and Oven Profile: Chi-Sq = 0.223 + 0.986 + 0.151 + 1.282 + 5.347 + 11.200 + 0.040 + 0.062 + 0.148 + 0.117 + 0.032 + 2.302 + 5.498 + 8.077 + 0.184 + 0.021 = 35.669**
   DF=9, P-Value = 0.00005. This is a statistically significant result.

2. **Solder Type: Chi-Sq = 0.09 + 0.33 + .42 + 1.02 + 3.66 + 4.68 + 0.08 + 0.08 + 2.72 + 9.85 + 12.60 = 17.79**
   DF = 3, P-Value = 0.0005. This is a statistically significant result.

3. **Oven Profile: (χ^2) Chi-Sq = 0.83 + 3.00 + 3.83 + 4.42 + 15.86 + 20.28 = 24.11**
   DF = 1, P-Value = 0.0000009. This is a statistically significant result.

SUMMARY OF DOE ANALYSIS

This analysis demonstrated that the "PPT" coated PCB's were better in terms of yield than the other types of wet solders and the oven profile was not a significant factor when assembling uBGA CCA's using PPT coated PCB's. This in turn indicates there is more room for variation within the oven profile, which allows for a wider process window.

In addition this analysis confirmed that the oven profile was a significant factor when assembling uBGA CCA's using wet solders and the "Alternate" (cooler) oven profile was better in terms of yield than the previous "Standard" profile. Furthermore, this analysis showed that the "P4" solder paste was clearly better in terms of yield than the "P3" solder pastes when used in conjunction with the "Alternate" (cooler) oven profile.

CONCLUSION

The process variables that were theorized to be affecting the first pass test yields were thought to be solder paste and oven profiles. These theories were clearly validated in the DOE analysis as summarized previously, and one can further conclude that the combination that will produce the highest probability of 100% yield is PPT coated PCB's used in conjunction with the "Alternate" oven profile.

As component package sizes continue to shrink it will become more and more apparent on how critical it is to control the solder paste printing and oven profile processes. Considering the fact that the solder paste printing process is

one of the most difficult processes to control, PPT will continue to become a more viable option, allowing CCA manufacturers to finally realize their dreams of zero defects.

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