IMPACT OF VIA STUB AND OFFSET ON 28 GIGABIT PER SECOND NRZ FORMAT SERIAL DATA TRANSMISSION

Matt Isaacs, 2015-06-03

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INTRODUCTION

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- **Data transmission at 28 Gbps on printed circuit boards is a testament to the inherently powerful underlying physics of old and simple PCB technology.**
- **Beyond 5 Gbps, IC designs require circuitry to compensate for PCB-related losses, except for very short paths (i.e., chip-to-chip/module).**
- **Beyond 10 Gbps, IC designs generally require circuitry to also compensate for dispersion and reflections, especially for long paths.**
- **Interference, noise, and EMI issues are improved by use of inner layers.**
- **Vias are essential interconnect for high-layer count PCBs between chips/connectors and inner-layer traces.**
- **The manufacturing variation of via fabrication has received moderate attention, due to its importance.**
- **More complex modulation schemes are being utilized to reduce the demands on PCB technology while increasing rates.**

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KEY REQUIREMENTS FOR (CAPABILITIES OF) PCB TECHNOLOGY FOR 25+ Gbps DATA TRANSMISSION

- **Low-loss path through use of low Dk and low Df materials.**
- **Minimal reflection throughout the PCB is achieved by consistency in dimensions and chemical/physical composition:**
  - Conformance to absolute impedance by absolute dimensional and electrical characteristics control targets and enables better source/load impedance match to components (IC drivers/receivers, connectors).
- **Sufficient time-invariance to be able to utilize circuitry with either fixed gain and filtering or an achievable range of adaptive gain and filtering:**
  - PCB loss variation over environment (humidity, temperature) is a challenge for high-speed serial data transmission.
  - The wider the range of adjustment, the more risk of instabilities or convergence problems.

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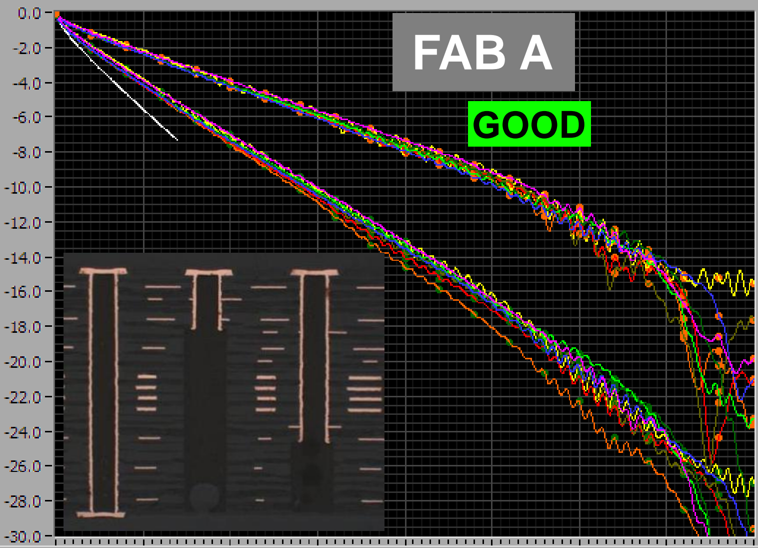
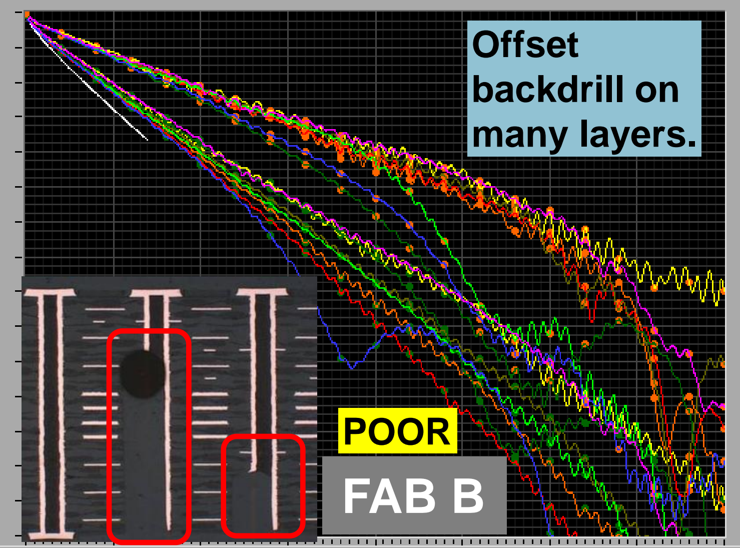
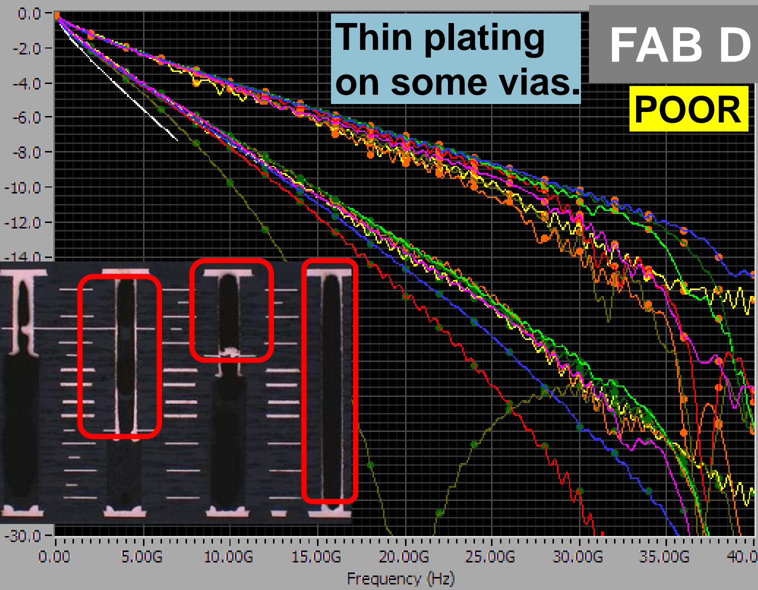
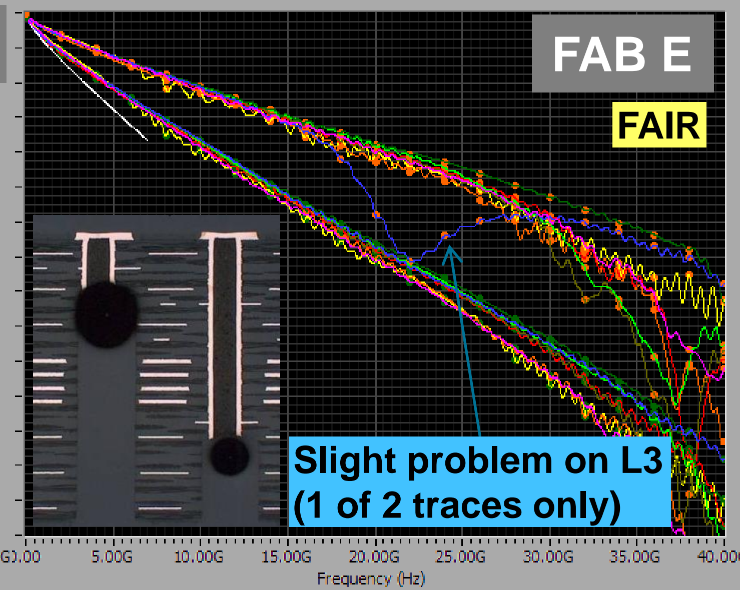
STUDY OF FIVE FABS THAT BUILT THE SAME PCB SHOWED VIA QUALITY WAS #1 ISSUE

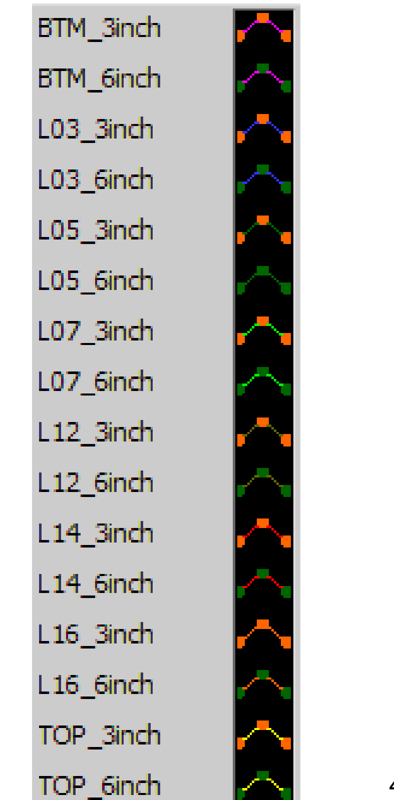
Via fabrication seems to dominate electrical performance (if the trace uses a via)!











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STACKUP FOR RECENT DV BOARD THAT WAS USED FOR SIMULATIONS TO 40 GHz/28 Gbps

24 Layers

Megtron6 HVLP

High-speed signals on layers:

14, 16, 18, 20, and 22

(chose lower layers to ease backdrill challenge; preferred to use upper layers, however)

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	1.70	.5 oz			Foil .5 oz
			3.64	3.56	Prepreg Megtron6 3313(54) 185
2	1.20	1 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
3	0.60	0.5 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
4	1.20	1 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
5	0.60	0.5 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
6	1.20	1 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
7	0.60	0.5 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
8	1.20	1 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
9	0.60	0.5 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
10	1.20	1 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
11	0.60	0.5 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
12	1.20	1 oz			
			3.42	3.00	Core Megtron6 3mils 1078 1 oz / 1 oz RTF
13	1.20	1 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
14	0.60	0.5 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
15	1.20	1 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
16	0.60	0.5 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
17	1.20	1 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
18	0.60	0.5 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
19	1.20	1 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
20	0.60	0.5 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
21	1.20	1 oz			
			3.22	4.61	Prepreg Megtron6 1035(73)/1035(73) 185
22	0.60	0.5 oz			
			3.64	3.90	Core Megtron6 3.9mils 3313 0.5 oz / 1 oz HVLP
23	1.20	1 oz			
			3.64	3.56	Prepreg Megtron6 3313(54) 185
24	1.70	.5 oz			Foil .5 oz
				115.62	Thickness over Laminate
				119.02	Thickness over Copper
				120.02	Thickness over Soldermask

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OVERVIEW OF HFSS STRUCTURE USED FOR SIMULATION (MXP CONNECTOR AND PCB)

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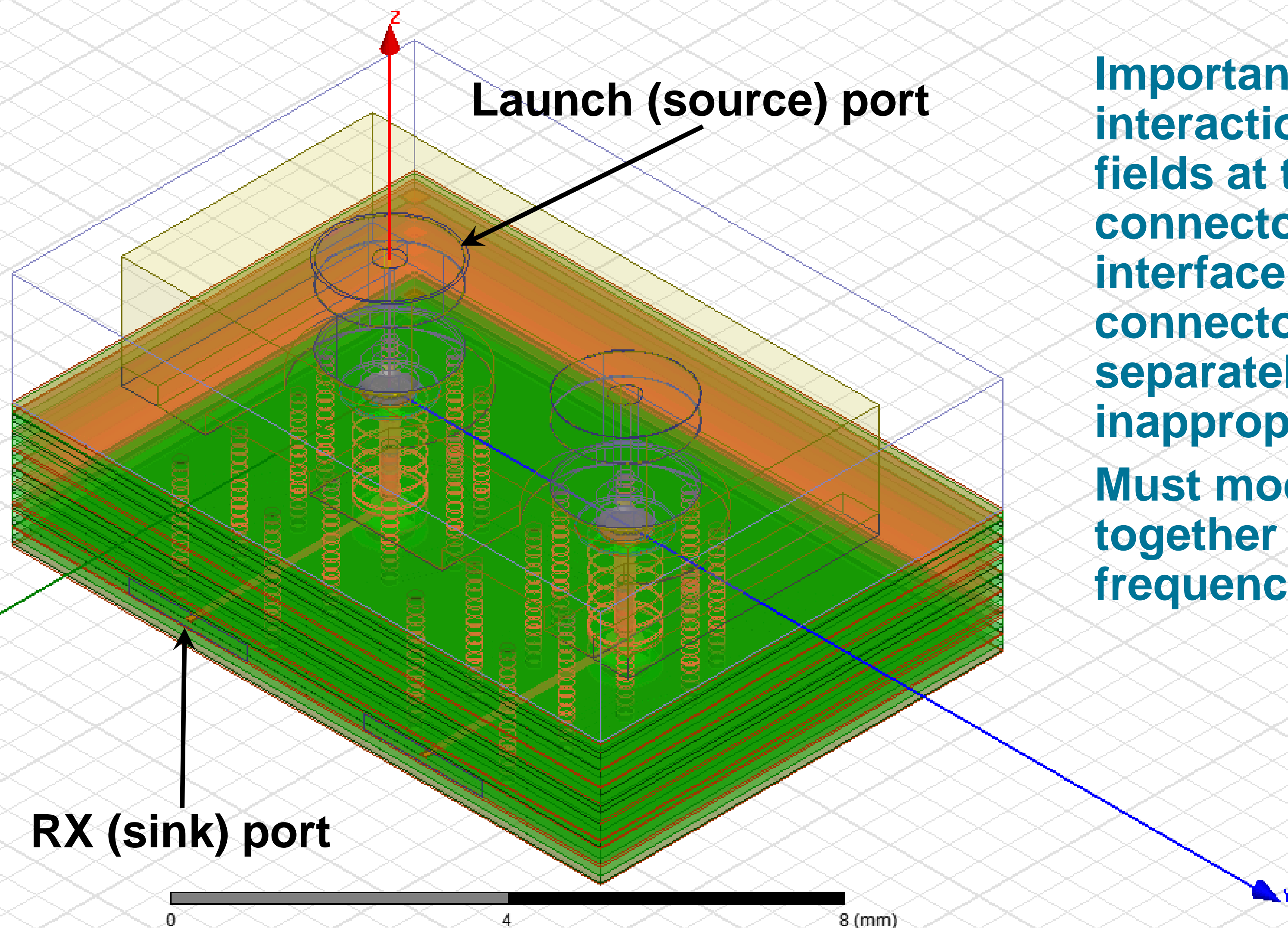
PCB features are highly parameterized to vary them and examine effects by using “Optimetrics”



Important: Due to interaction of the EM fields at the connector-PCB interface, modelling connectors and PCBs separately is inappropriate.

Must model them together at high frequency.

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OVERVIEW OF HFSS STRUCTURE USED FOR SIMULATION – SIDE VIEW

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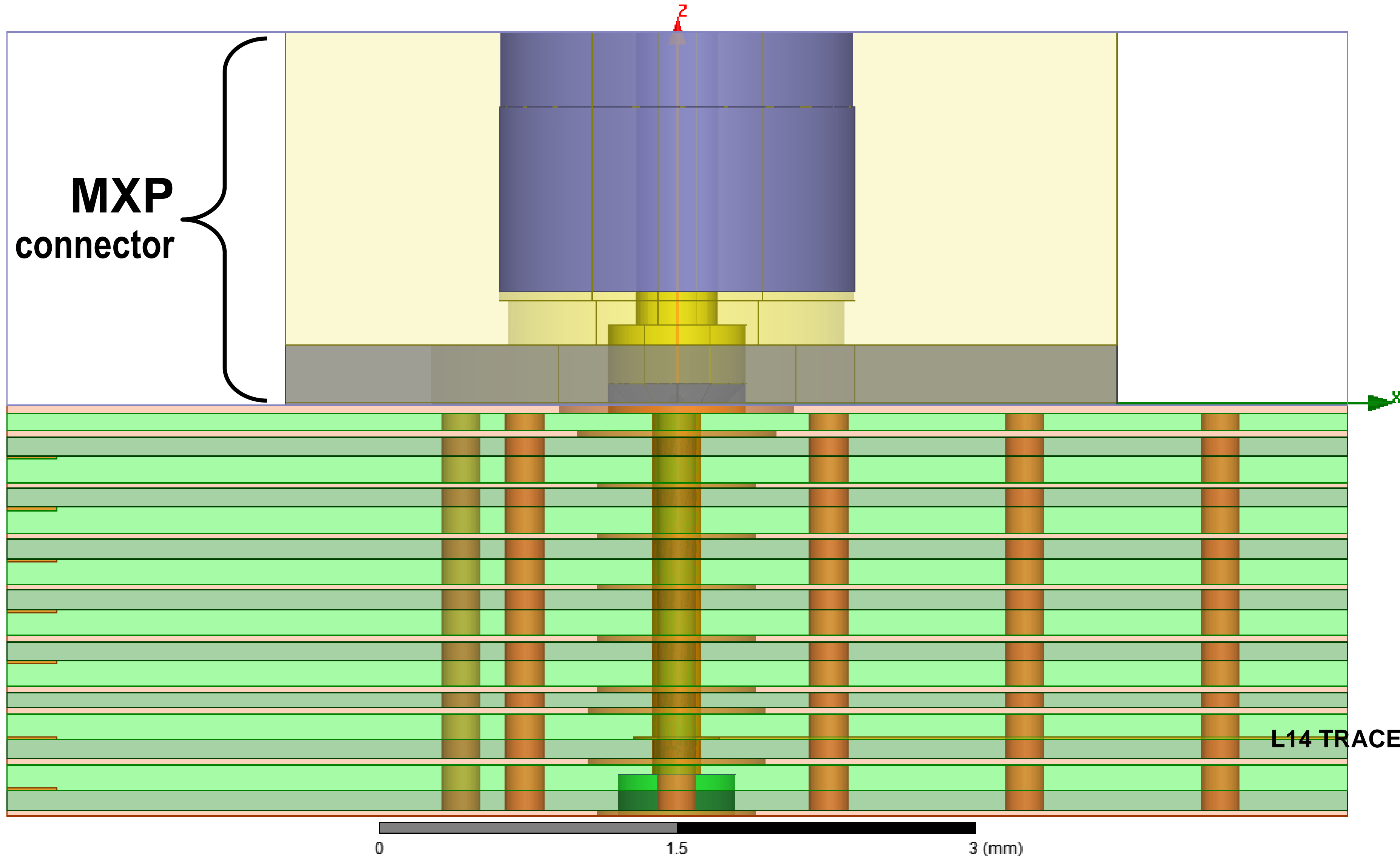
Optimized antipads (different for different layers) shown here.



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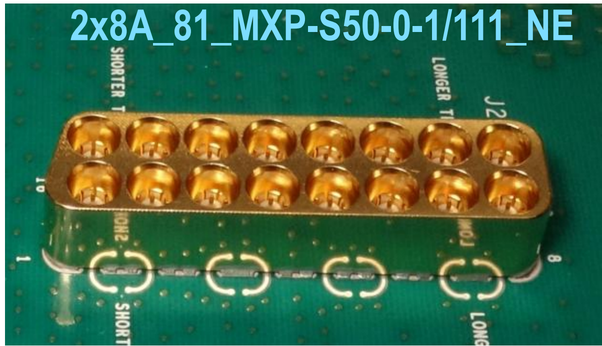
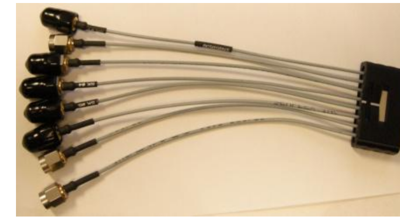
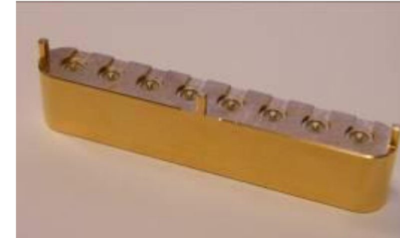
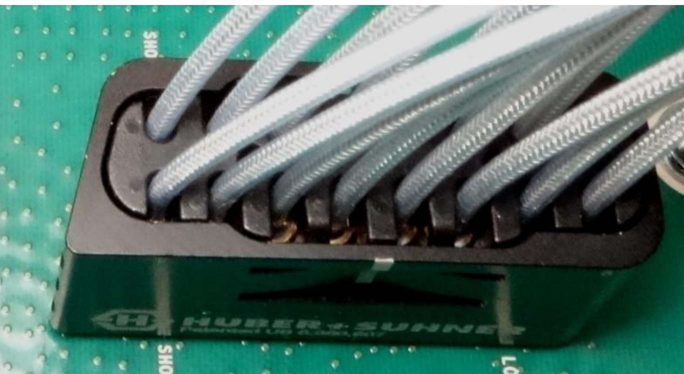
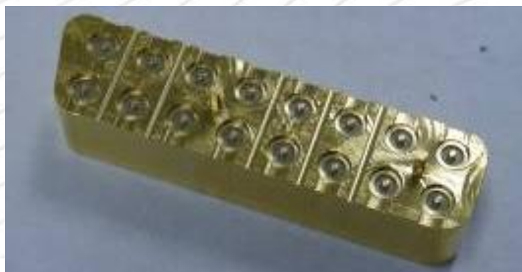
MXP is a family of interconnect products that provides 8 or 16 coaxial connections in a single mating operation, which is rapid and reliable, with < 10dB RL > 40 GHz.



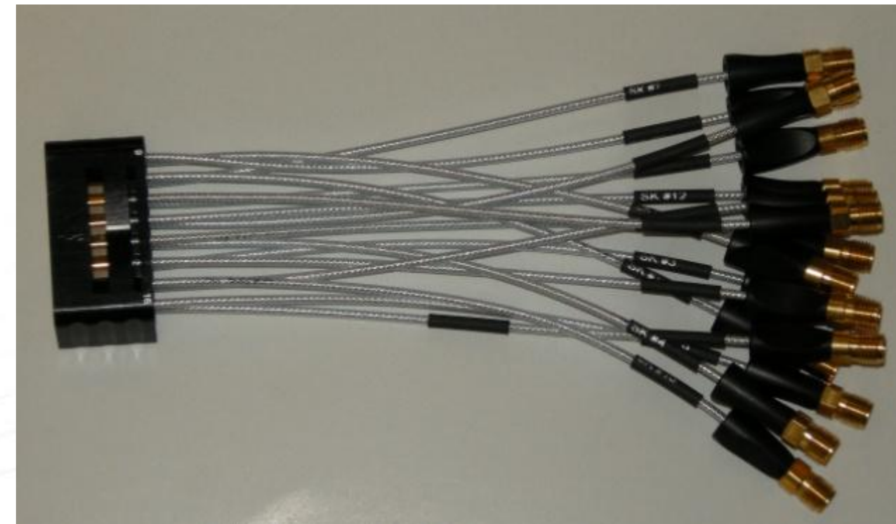








MXP is solely available from Huber+Suhner



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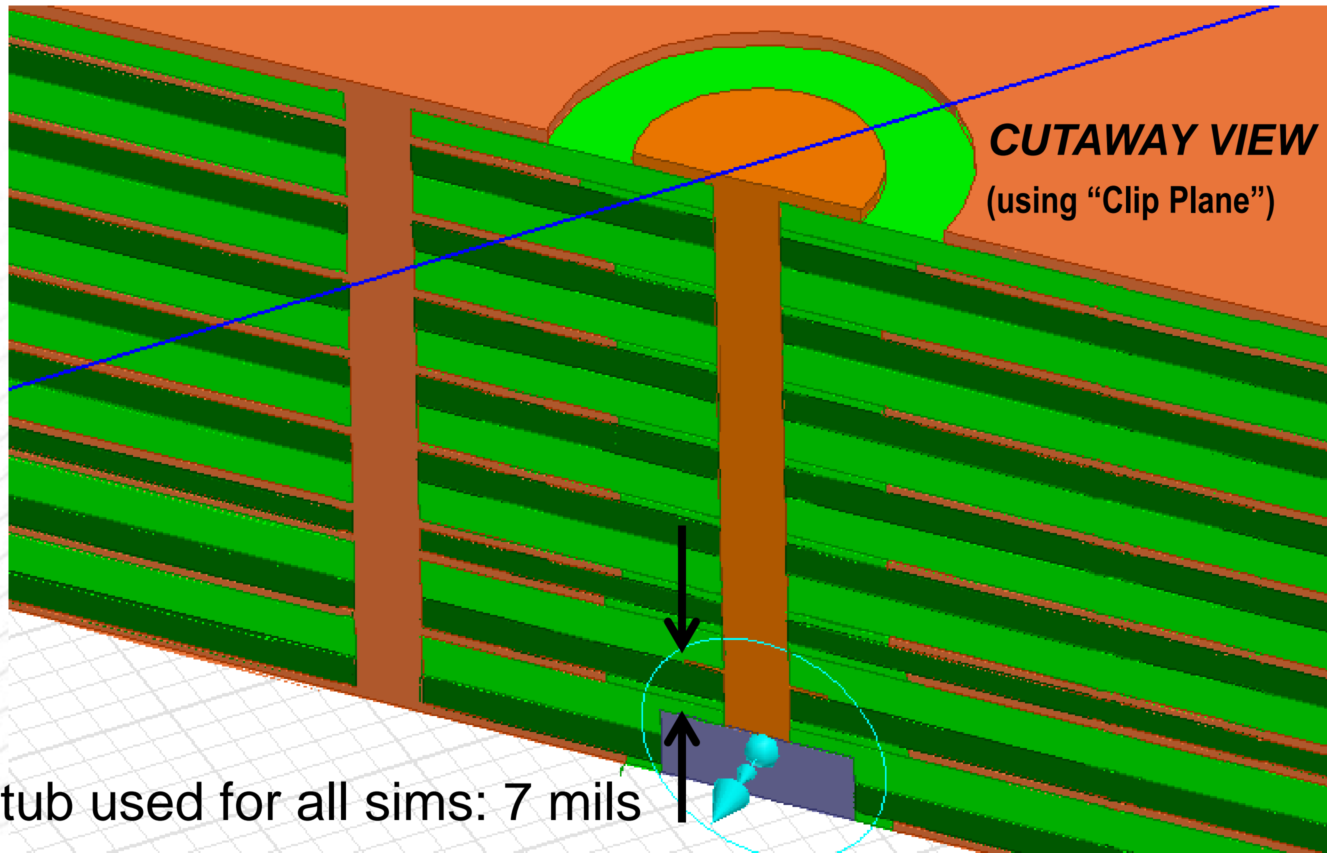
OVERVIEW OF HFSS STRUCTURE USED FOR SIMULATION – ANGLE VIEW

Optimized antipads are shown here.

Performance is best with slightly large antipad for layers 2, 13, and 15 as compared to layers 4, 6, 8, 10, and 12. It is speculated that the reasons for this are:

- **The pad for the MXP pin is large, so less capacitance to GND is desirable with a larger L2 antipad.**
- **The via ring for L14 is larger than the via barrel, so less capacitance to GND is desirable with larger L13 and LI15 antipads.**



Backdrill stub used for all sims: 7 mils

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OVERVIEW OF HFSS STRUCTURE USED FOR SIMULATION – BACKDRILL INFO

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Properties

Name	Value	Unit	Evaluat
$AntipadRadius	16	mil	16mil
$AntipadRadius_SL	18	mil	18mil
$BackdrillRadius	0.3	mm	0.3mm
$BackdrillStub	7	mil	7mil
$ConnEr	3.05		3.05
$DistanceRingGNDvias	1.1	mm	1.1mm
$GapNeck2GND	10	mil	10mil
$GapPad2GND	0.25	mm	0.25mm
$GapTrace2GND	10	mil	10mil
$GviaDrillRadius	0.1	mm	0.1mm
$GviaRingWidth	0.125	mm	0.125mn

stdGarcVias.v2a - MXPx2 - Modeler]

Clip Planes: MXP_VIP_L14bd(tol17),Meg6,stdGar...

Plane | Options

Name	Enabled	Show Cap	Show Handle	Flip
ClipPlane1	✓	✓	✓	

Add | Reset | Delete | Close

CUTAWAY VIEW

(using "Clip Plane")

Measure Data

Position1(EdgeCenter_160088) = [-0.225, 0, -1
Position2(EdgeCenter_178270) = [-0.3, 0, -1.9
Distance = 0.192971085917mm
X Distance = 0.075mm
Y Distance = 0mm
Z Distance = 0.1778mm
Angle(P2O - P1O) = 1.52911257708deg

7 mils

Close

0.9 (mm)

X: -0.3 Y: 0 Z: -1.900428 Absolute

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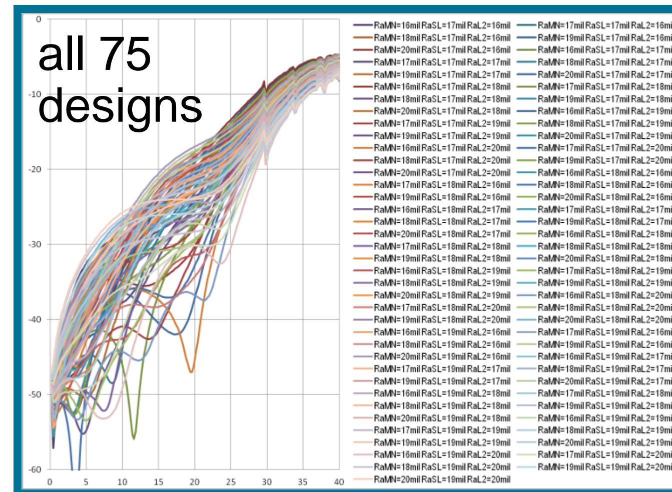
DESIGN CASES FOR OPTIMETRICS RUN NAMED "Pswp_RapadsL2yMAINySL"

Setup Sweep Analysis

Sweep Definitions | Table | General | Calculations | Options

Sync #	Variable	Description
	$AntipadRadius	Linear Step from 16mil to 20mil, step=1mil
	L2GndAntipadRadius	Linear Step from 16mil to 20mil, step=1mil
	$AntipadRadius_SL	Linear Step from 17mil to 19mil, step=1mil



Setup Sweep Analysis

Sweep Definitions | Table | General | Calculations | Options

Sim. Setup	Include
Setup0	☐
Setup1	☐
Setup2	☐
Setup3	☐
Setup40GHz	☐
SetupDCto40GHz	☐
SetupDiscrete	☐
SetupPortsOnly	☐
dSp005_30G	☑

Starting Point:

Design Variable	Override	Value	Units
$NumGNDringVias	☐	7	
$NumGNDtraceVias	☐	2	
$SignalChannelWidth	☐	1.1	mm
$SignalViaRadius	☐	0.125	mm
$SpaceViaPad2Edge	☐	0.555	mm
$Xsize	☐	270	mil
$Ysize	☐	10	mm
$core_Df	☐	0.004	
$core_Dk	☐	3.22	
$neck_length	☐	1.78	mm
$pad_radius	☐	0.35	mm
$prepreg_Df	☐	0.004	

Signal via diameter is fixed at 0.25 mm.

Used 12 Linux computers (8 processor cores each) to analyze all 75 designs; took ~12 hours to run.

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RL (S11) RESULTS FOR FINAL OPTIMIZATION RUN – FIVE BEST DESIGNS

Note:
RaMN=$AntipadRadius in HFSS (layers 4, 6, 8, 10, 12)
RaSL=$AntipadRadius_SL in HFSS (L13 and L15)
RaL2=L2GndAntipadRadius in HFSS

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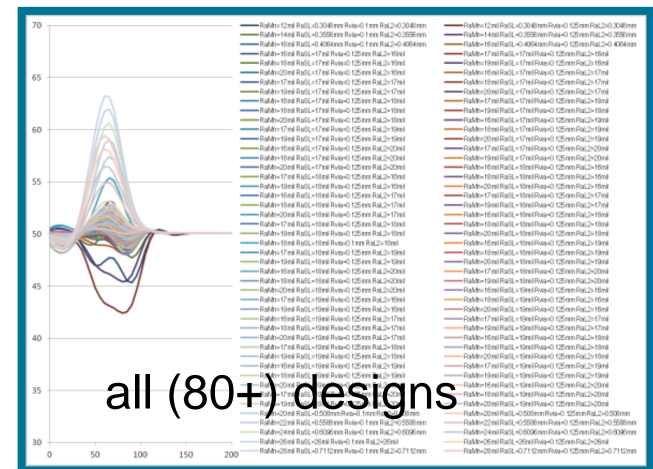
TDR (T11) RESULTS FOR FINAL OPTIMIZATION RUN – FIVE BEST DESIGNS



S.E. Zo (ohms)

51
50.8
50.6
50.4
50.2
50
49.8
49.6
49.4
49.2
49

0 50 100 150 200

Time (psec)

RaMn=17mil RaSL=17mil Rvia=0.125mm RaL2=18mil

RaMn=17mil RaSL=17mil Rvia=0.125mm RaL2=19mil

RaMn=16mil RaSL=17mil Rvia=0.125mm RaL2=20mil

RaMn=17mil RaSL=18mil Rvia=0.125mm RaL2=18mil

RaMn=16mil RaSL=18mil Rvia=0.125mm RaL2=19mil

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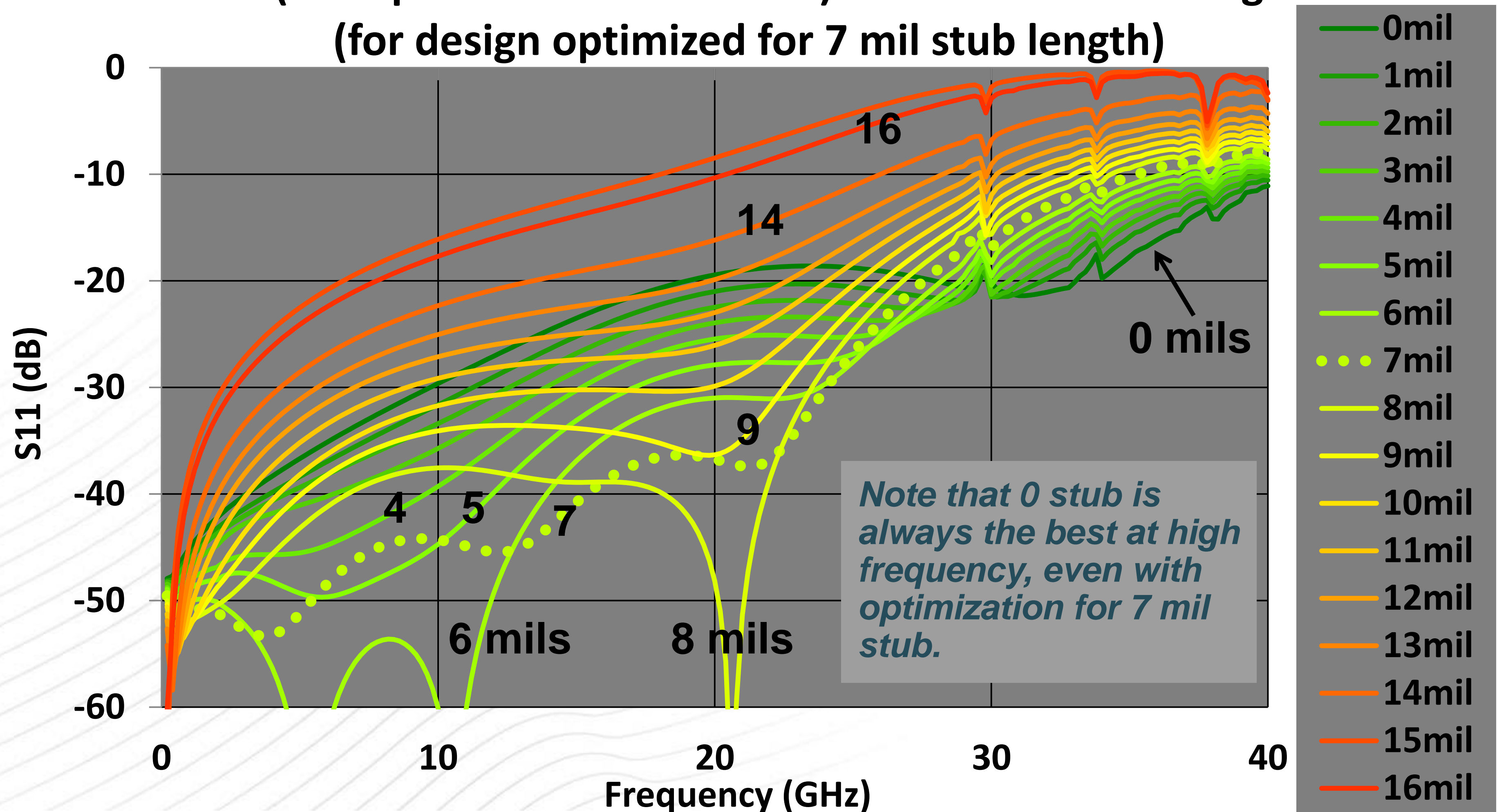
SIMULATED RL (S11) FOR VARYING BACKDRILL STUB LENGTH

Note that design was already optimized assuming backdrill stub length = 7 mils (expected nominal).



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OPTIMIZED CONNECTOR / VIA LAUNCH DIMENSIONS FOR 7 MIL POST-BACKDRILL STUB LENGTH

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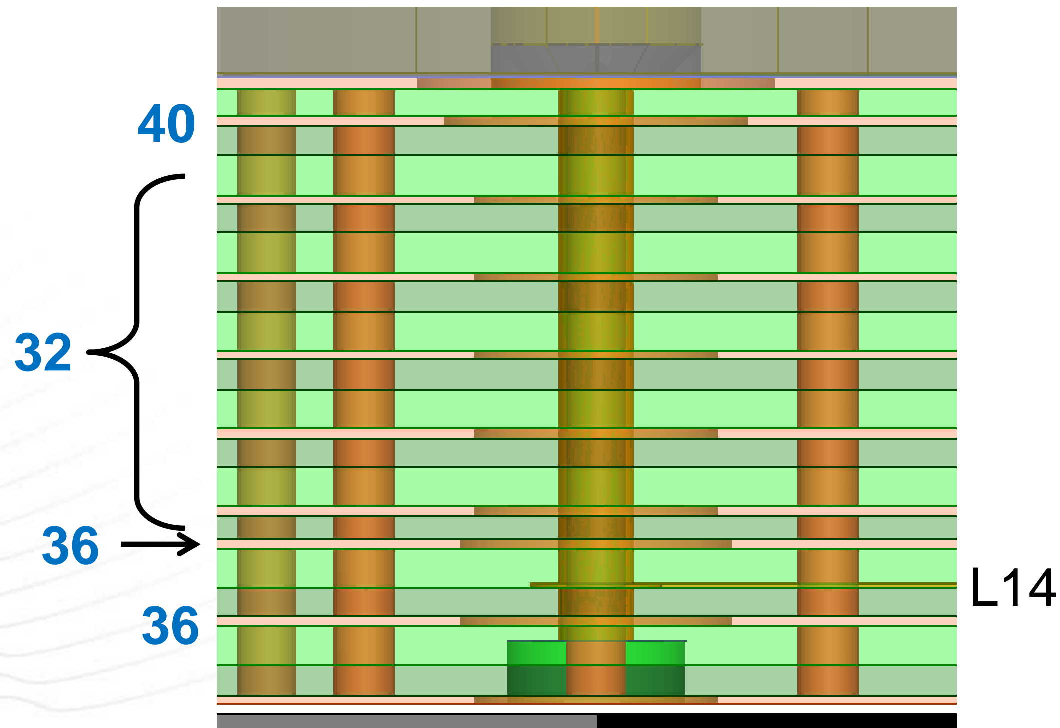
Two different proposals, varying in implementation difficulty:

- **If all antipads are the same: 36 mil diameter.**
- **If they can be different:**
  - **L2 antipad diameter = 40 mils**
  - **L13 and L15 antipad diameter = 36 mils (note: trace on L14)**
  - **All other antipads (layers 4, 6, 8, 10, and 12): 32 mils**

Note: The second approach is probably much better suited to be utilized for other stripline layers (i.e., L16, L18, …).

Just replace L13/L15 with the appropriate layers above and below the stripline layer.



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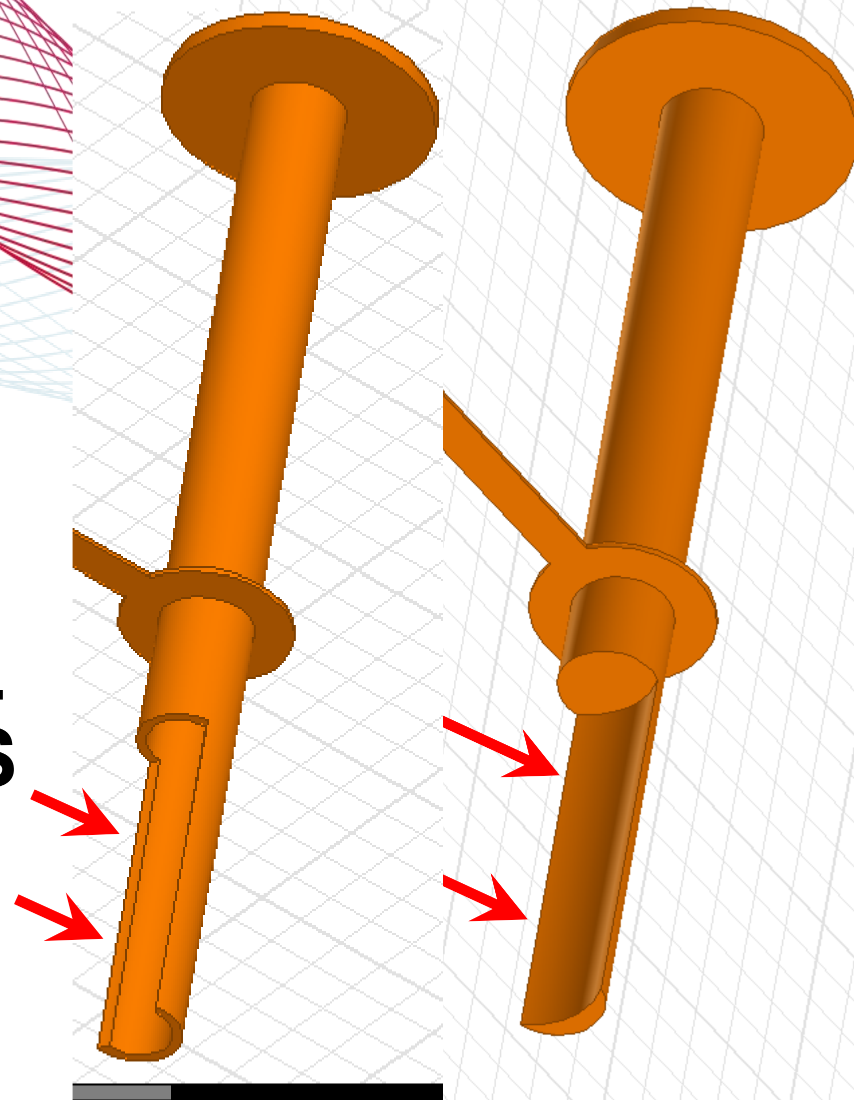
EFFECT OF BACKDRILL OFFSET WHICH LEAVES PART OF THE VIA



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OFFSET BACKDRILL EXAMPLES WHERE A PORTION OF THE VIA CYLINDER REMAINS

Seen on only certain PCBs in a fab lot/run.

- **Examples from a lot of “Tomahawk” PCBs, 200-127325-0010v0.**

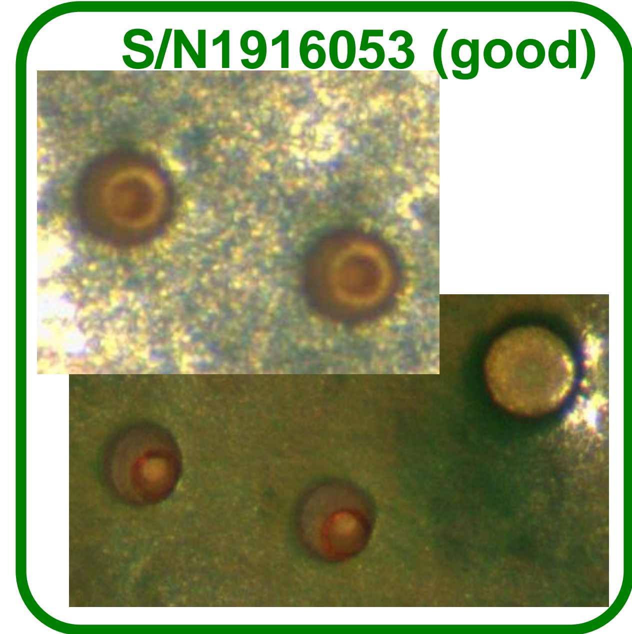
(S/N 1916051)

TTM 1SAM76-0 94V-0
4614 -1
200-127325-0010_01
1 OF 2

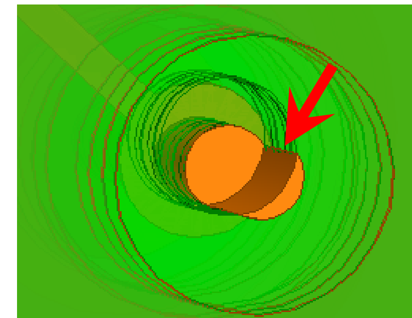
PCB at an angle relative to camera

PCB at an angle relative to camera

S/N1916053 (good)



HFSS model drawn to mimic issue



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CROSS-SECTION PHOTOS OF GOOD AND BAD BACKDRILL OFFSETS

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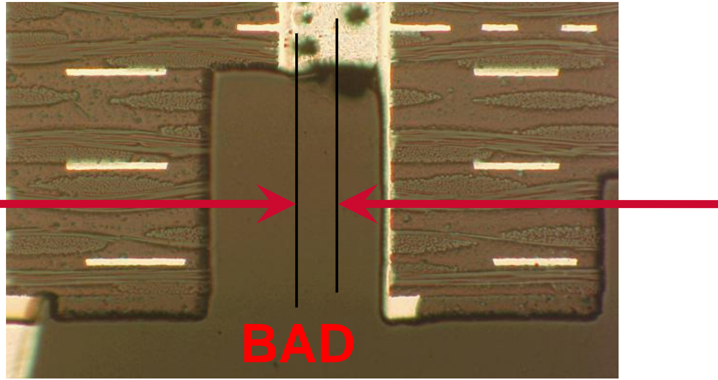
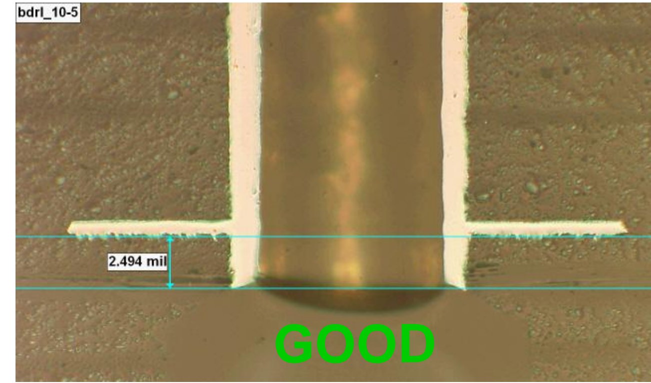
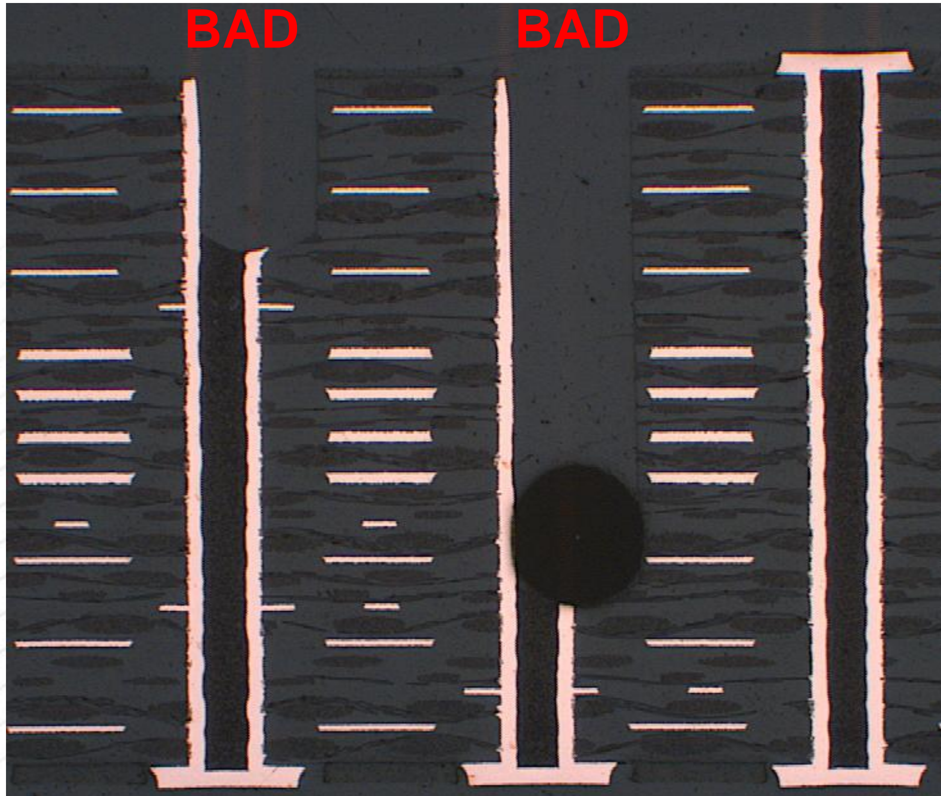
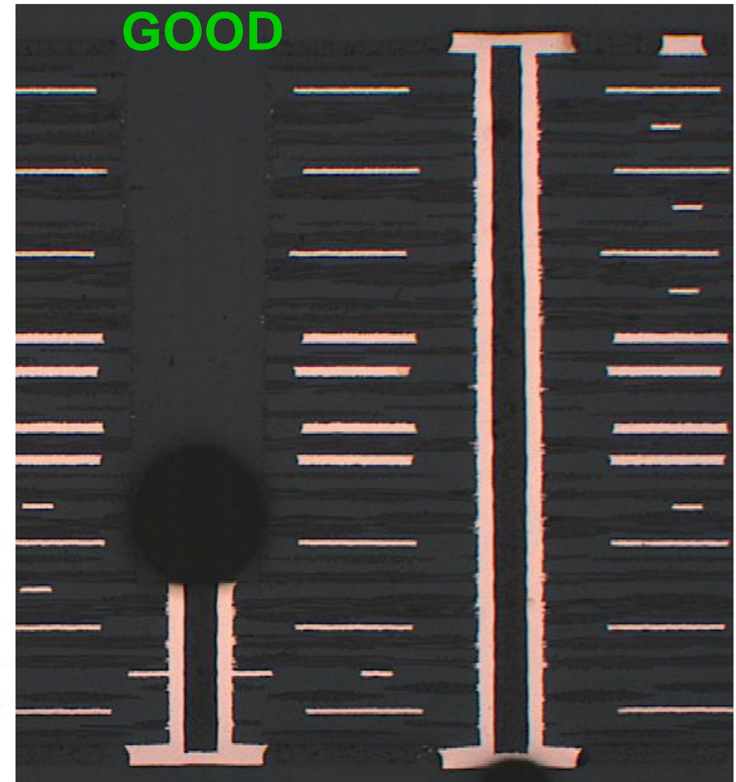
OFFSET









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IMPEDANCE DISCONTINUITIES MORE PRONOUNCED ON PCB WITH OFFSET BACKDRILLING (PARTIAL STUBS)

TDR Measurements of Cal Traces of ProductA DVT boards - S/Ns 1916051 and 1916053

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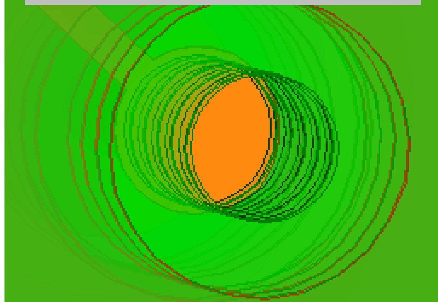
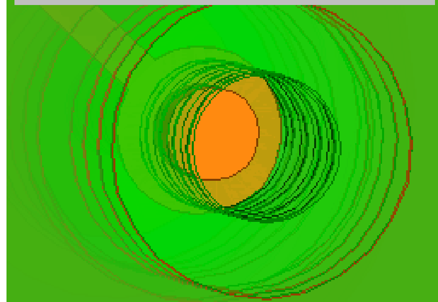
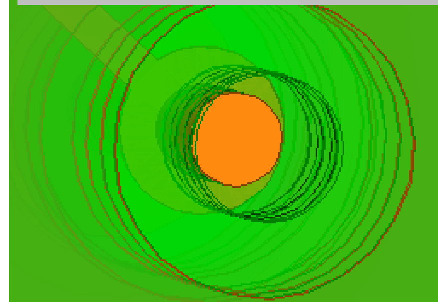
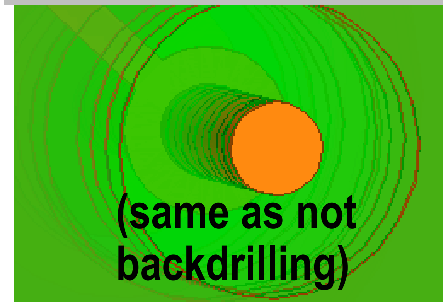
JUST A SLIGHT X/Y OFFSET CAN LEAVE A PORTION OF THE VIA

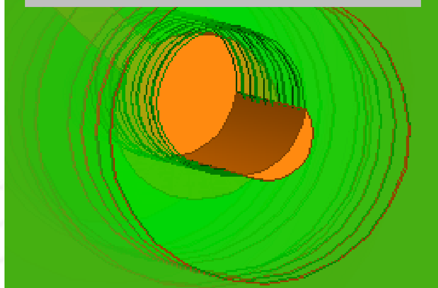
HFSS model was designed so stub length and backdrill offset are varied and simulated.

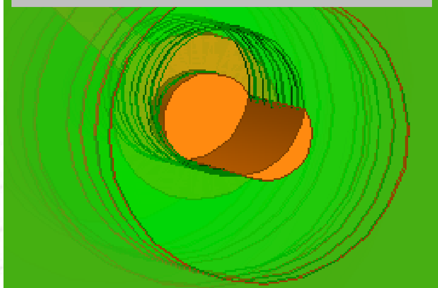


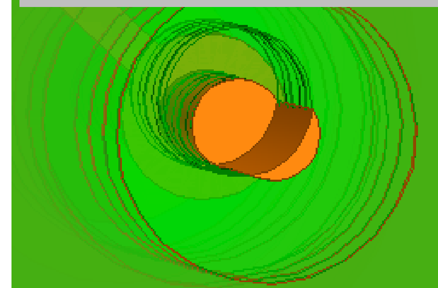


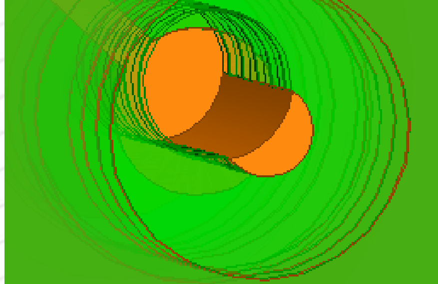


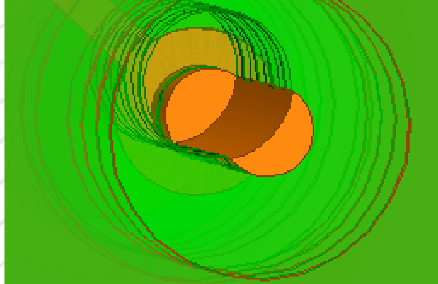


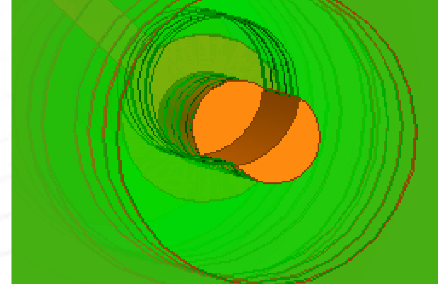


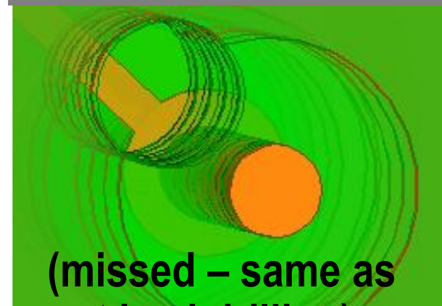












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LEAVING ANY PORTION OF VIA BARREL IS AS ABOUT AS BAD AS COMPLETELY FAILING TO BACKDRILL

Return Loss (S11) vs. frequency for various backdrill offsets and stub lengths

RL (S11), dB

0
-5
-10
-15
-20
-25
-30
-35
-40

0
10
20
30
40

Frequency (GHz)

DESIRED AVOIDANCE REGION

25
15
10
0
5

reflection cancellation; only helpful for narrowband data

Note: Design was already optimized assuming backdrill stub length = 7 mils (expected nominal).

- offset=0mil stub=0mil
- offset=0mil stub=5mil
- offset=0mil stub=10mil
- offset=0mil stub=15mil
- offset=0mil stub=25mil
- offset=0mil stub=51.6mil
- offset=5mil stub=0mil
- offset=5mil stub=5mil
- offset=5mil stub=10mil
- offset=5mil stub=15mil
- offset=5mil stub=25mil
- offset=5mil stub=51.6mil
- offset=15mil stub=0mil
- offset=15mil stub=5mil
- offset=15mil stub=10mil
- offset=15mil stub=15mil
- offset=15mil stub=25mil
- offset=15mil stub=51.6mil

via entirely missed

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THERE IS NO SUCH THING AS A GOOD PARTIALLY BACKDRILLED VIA

Zo discontinuity is very similar, regardless of drill depth, when a backdrill offset causes part of the via to remain.

XY Plot 3_1 MXPx2

TDRZt(TrcSL1_T1)

54.00 52.00 50.00 48.00 46.00 44.00 42.00 40.00 38.00 36.00

0.00 50.00 100.00 150.00 200.00

Time [ps]

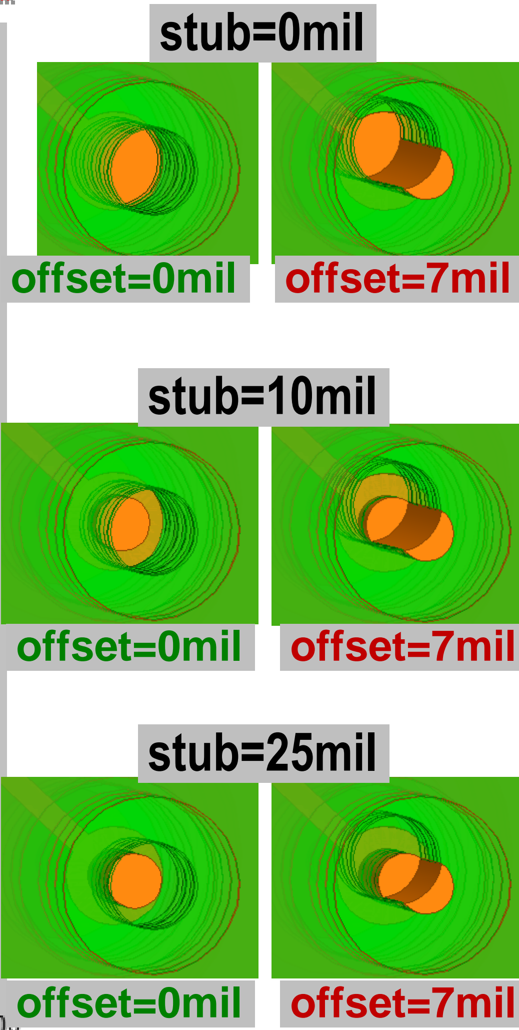
0
5
10
15
25

stubs= {0, 5, 10, 15, 25}
w/ offset=7mil

51.6

Curve Info

- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='0mil' $BackdrillStub='0mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='0mil' $BackdrillStub='5mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='0mil' $BackdrillStub='10mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='0mil' $BackdrillStub='15mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='0mil' $BackdrillStub='25mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='0mil' $BackdrillStub='51.6mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='7mil' $BackdrillStub='0mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='7mil' $BackdrillStub='5mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='7mil' $BackdrillStub='10mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='7mil' $BackdrillStub='15mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='7mil' $BackdrillStub='25mil'
- TDRZt(TrcSL1_T1) dSp005_40G : Int0p2to40G $Backdrill_Xoffset='7mil' $BackdrillStub='51.6mil'



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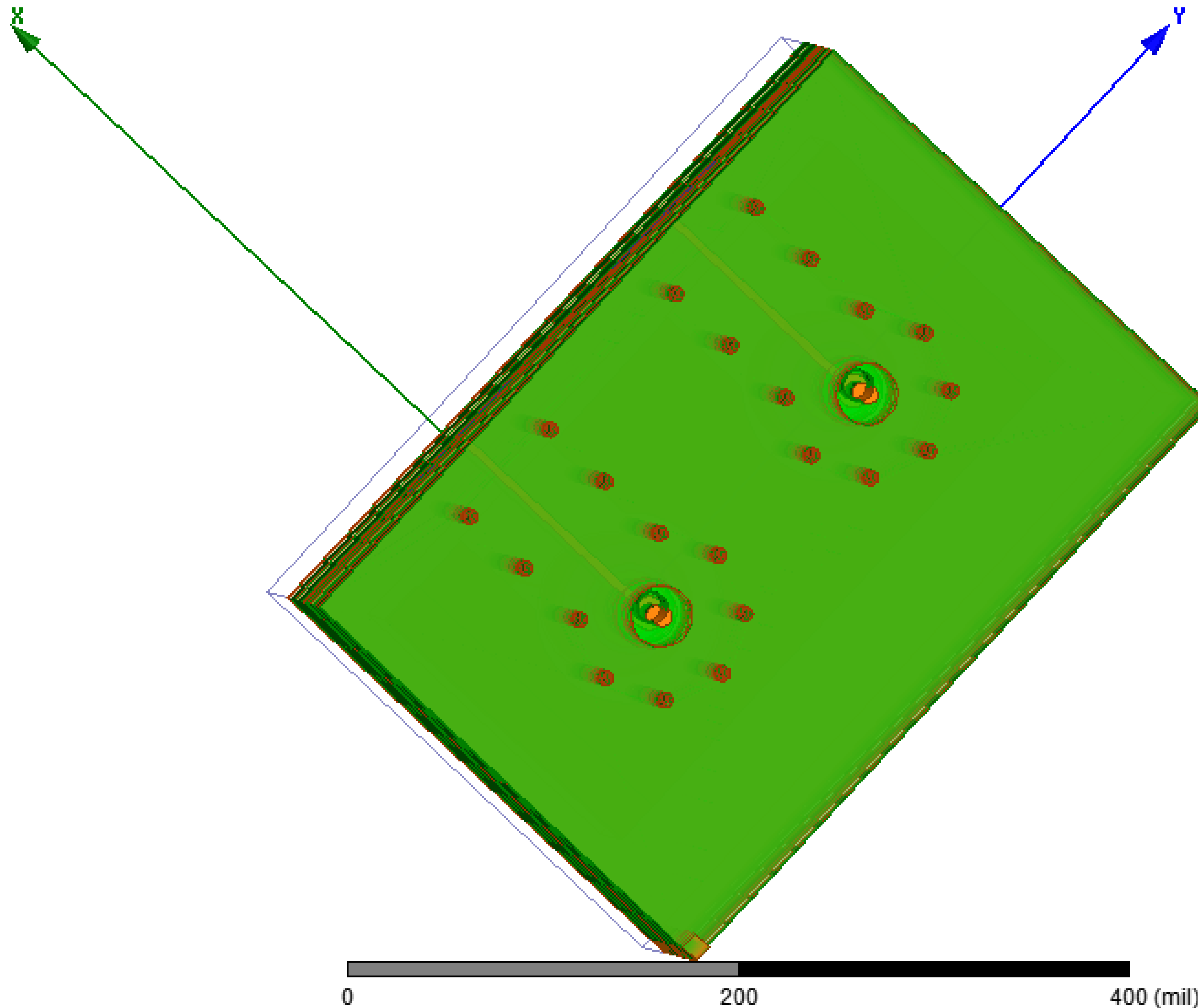
This is just to give a reference for the view orientation.



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30 different design variants, total.

Setup Sweep Analysis

Sweep Definitions | Table | General | Calculations | Options

Sync #	Variable	
	$Backdrill_Xoffset	Single Value at 0mil
		Single Value at 5mil
		Single Value at 7mil
		Single Value at 10mil
		Single Value at 15mil
	$BackdrillStub	Single Value at 0mil
		Single Value at 5mil
		Single Value at 10mil
		Single Value at 15mil
		Single Value at 25mil
		Single Value at 51.6mil

Setup Sweep Analysis

Sweep Definitions | Table | General | Calculations | Options

*	$BackdrillStub	$Backdrill_Xoffset
1	0mil	0mil
2	5mil	0mil
3	10mil	0mil
4	15mil	0mil
5	25mil	0mil
6	51.6mil	0mil
7	0mil	5mil
8	5mil	5mil
9	10mil	5mil
10	15mil	5mil
11	25mil	5mil
12	51.6mil	5mil
13	0mil	7mil
14	5mil	7mil
15	10mil	7mil
16	15mil	7mil
17	25mil	7mil
18	51.6mil	7mil
19	0mil	10mil
20	5mil	10mil
21	10mil	10mil
22	15mil	10mil
23	25mil	10mil
24	51.6mil	10mil
25	0mil	15mil
26	5mil	15mil
27	10mil	15mil
28	15mil	15mil
29	25mil	15mil
30	51.6mil	15mil

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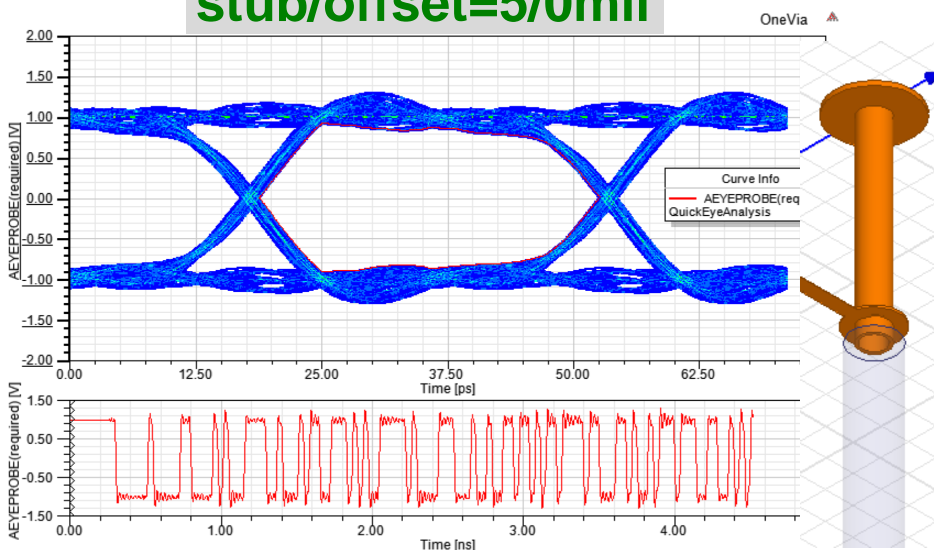
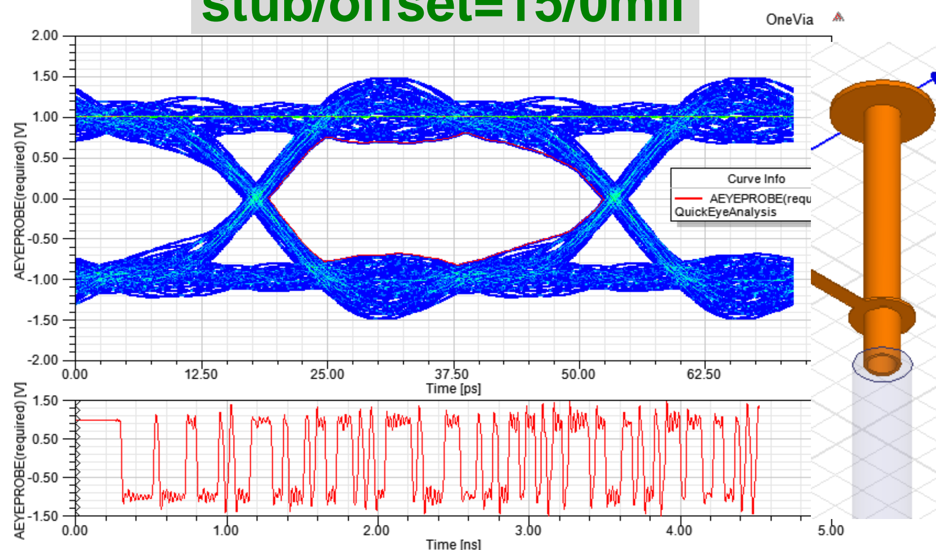
28.125 Gbps EYE DIAGRAM RESULTS FOR ONE (1) VIA IN THE PATH, VARIOUS STUB/OFFSET CASES

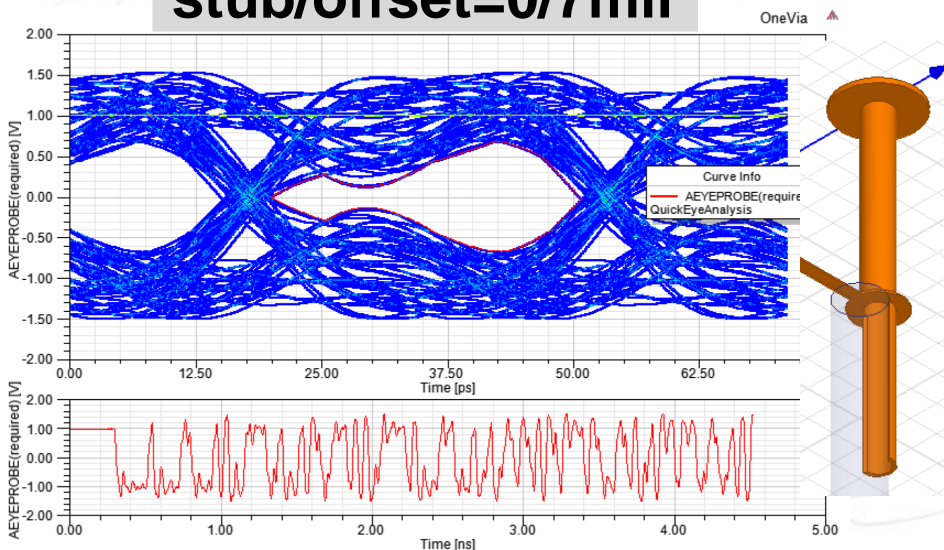
stub/offset=5/0mil



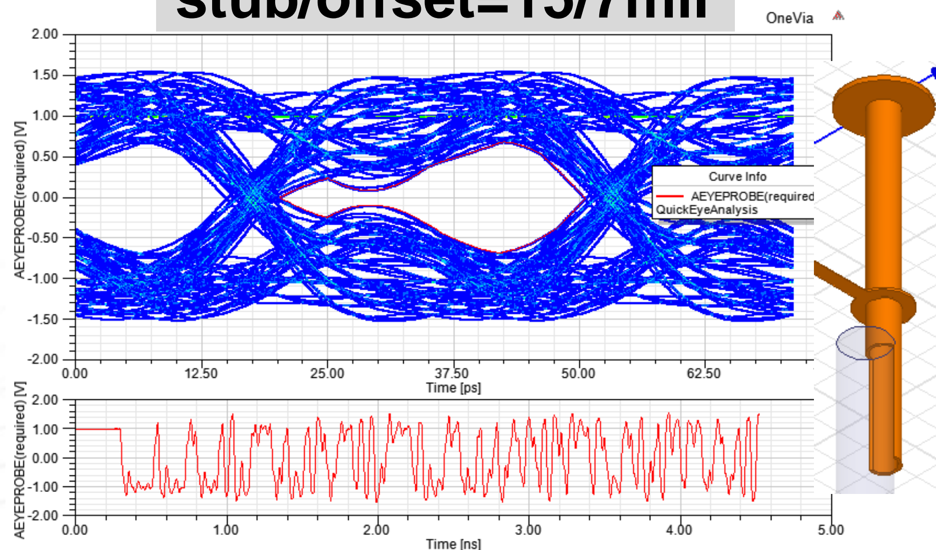
stub/offset=15/0mil



stub/offset=0/7mil



stub/offset=15/7mil



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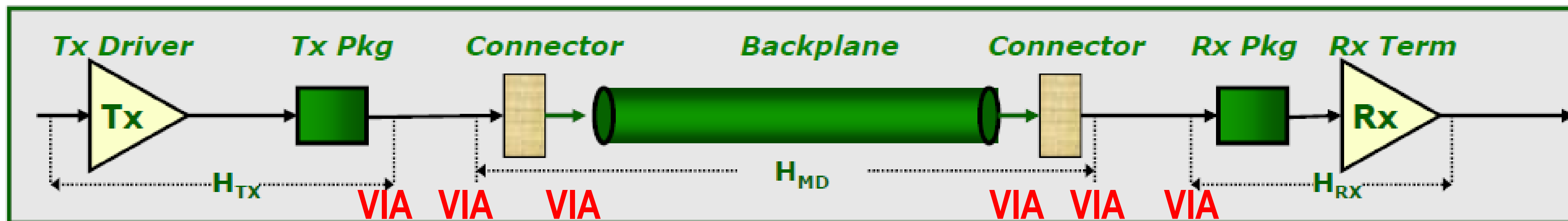
A TYPICAL BACKPLANE SYSTEM HAS AT LEAST SIX VIAS IN THE PATH

Backdrilled vias are in the following locations:

1. Chip ball (dogbone aka “offset via” or Via-In-Pad) to PCB stripline layer
2. Linecard (“daughtercard”, “blade”, etc.) connector via
3. Backplane connector via
4. Backplane connector via near far-end linecard
5. Line or other card connector via
6. PCB to chip ball (dogbone or VIP)



- Even with advanced receiver architectures (i.e., “DFE”), only the discontinuities closest to the receiver get attention (usually, at best, compensates for reflections related to the closest PCB via, the chip package, on-chip ESD structure).

Diagram courtesy of Vivek Telang, Broadcom

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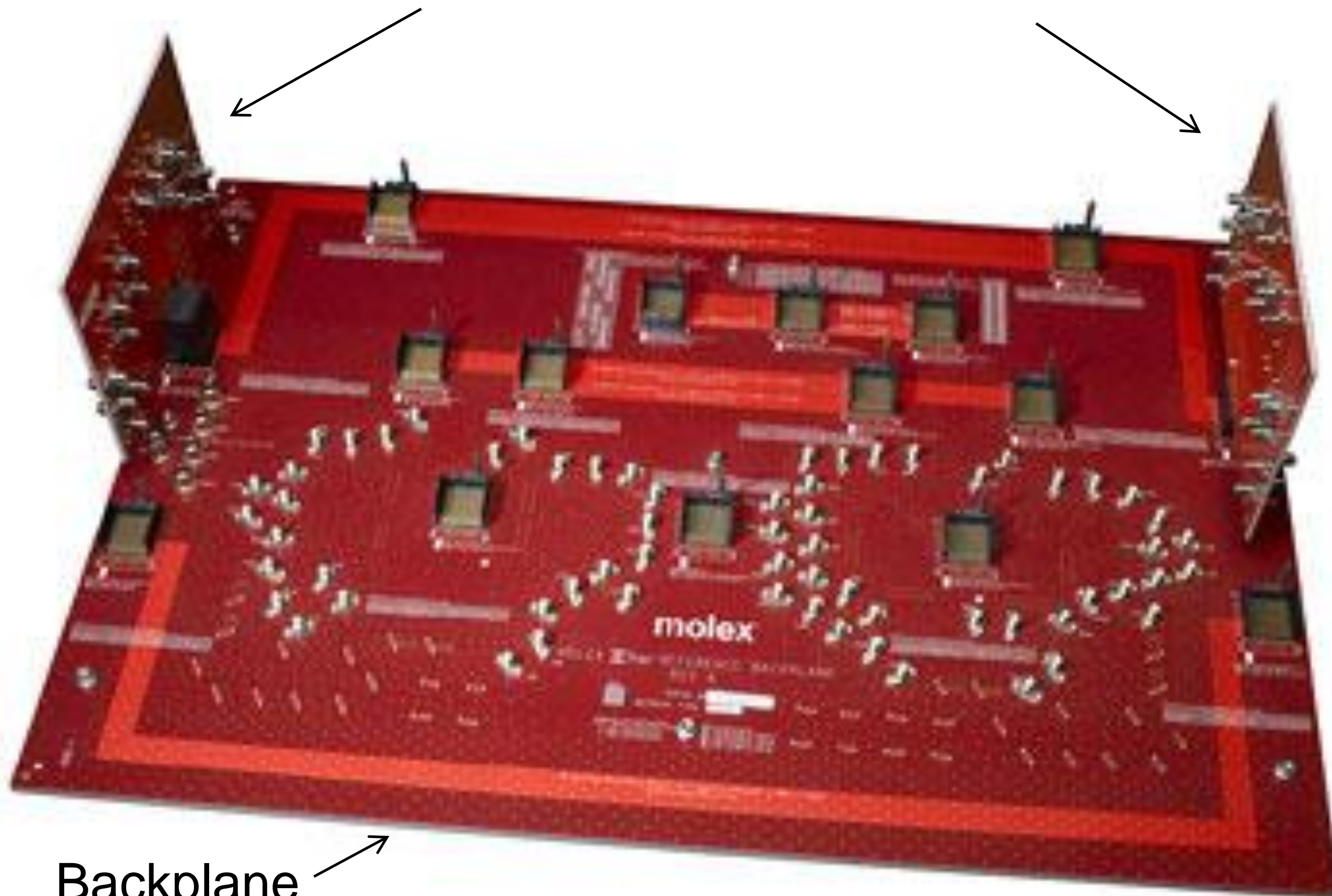
EXAMPLE BACKPLANE EVALUATION SETUP

Tier 1 backplane connector manufacturers often design and build their own demonstration vehicles.

Linecards, aka daughtercards



Backplane
(multiple paths available to choose from for evaluation purposes)

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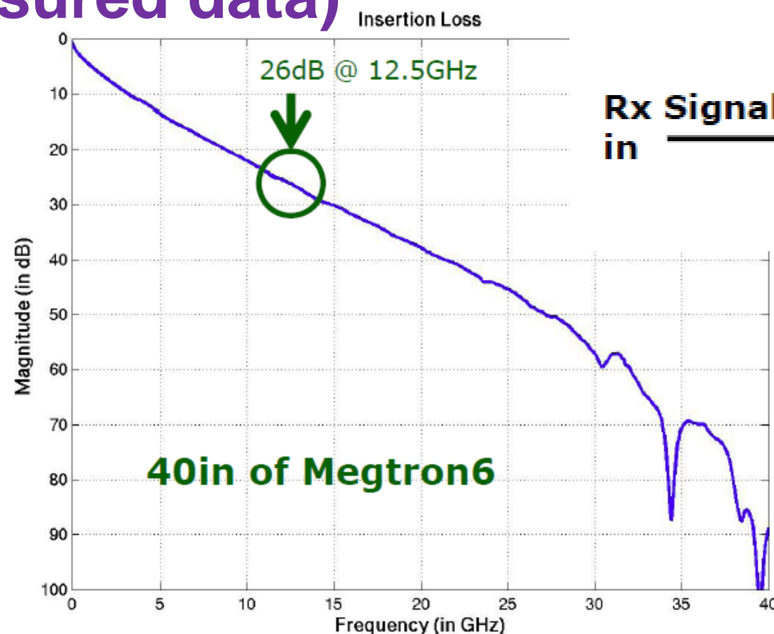
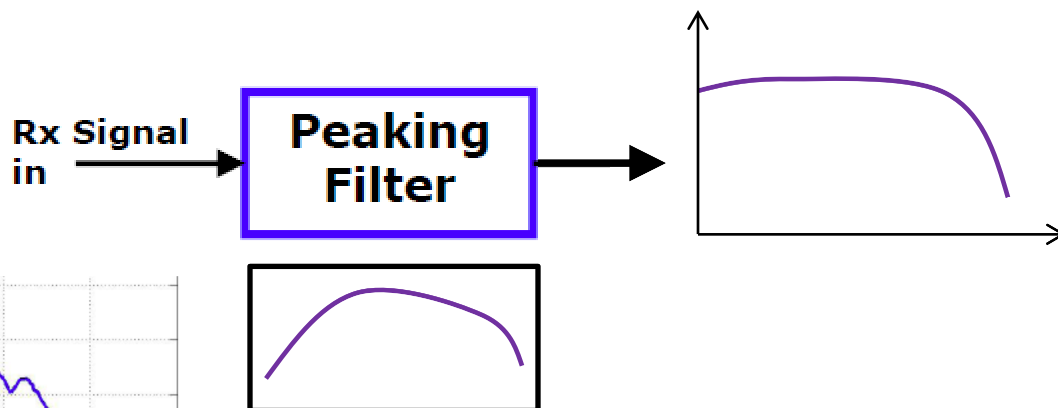
CHANNEL LOSS COMPENSATION BY "CTLE"

The attenuation vs. frequency in a typical PCB can be compensated for by filtering and amplifying appropriately with electronic circuits on-chip ("Continuous Time Linear Equalizer")





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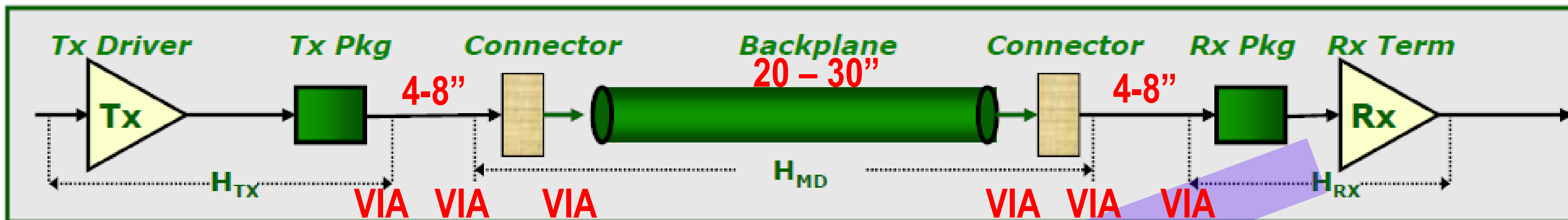
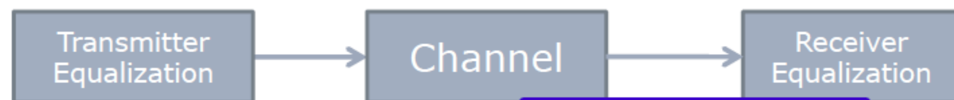
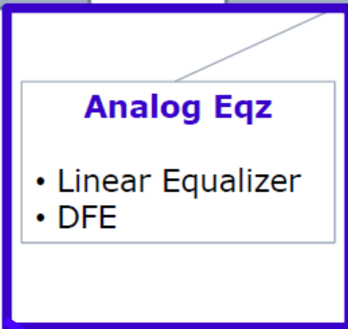
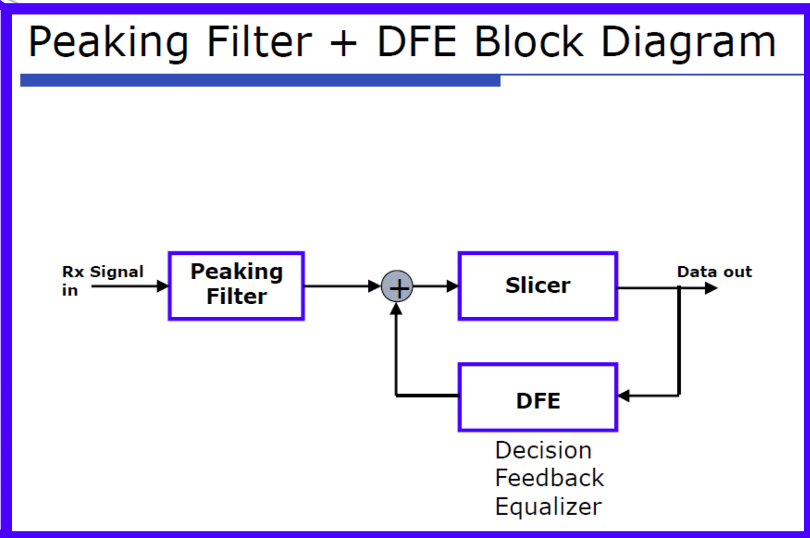
DFE ENABLES COMPENSATION OF EFFECTS LIKE DISPERSION, ISI, AND REFLECTION

Reflections, especially multiple ones, cannot be fully compensated, nor at excessive distance (delay).









Diagrams courtesy of Vivek Telang, Broadcom

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4 OF 6 TYPICAL VIAS CANNOT BE COMPENSATED DUE TO DISTANCE (DELAY) BEYOND # OF DFE TAPS

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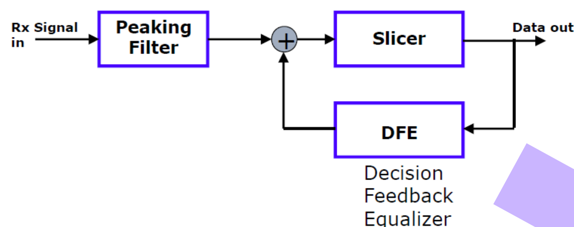
Number of taps required for reflection compensation = delay/period.
Becomes too complex (too much power and area cost) if # of taps is high.

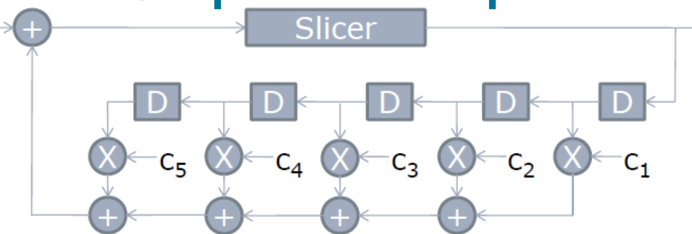
Peaking Filter + DFE Block Diagram



Decision Feedback Equalizer

- Cancels post-cursor ISI
  - Equalization without noise enhancement
  - Implementation is challenging at high speeds
  - Error propagation can be an issue
- Coefficients are adapted using LMS

5 tap DFE example

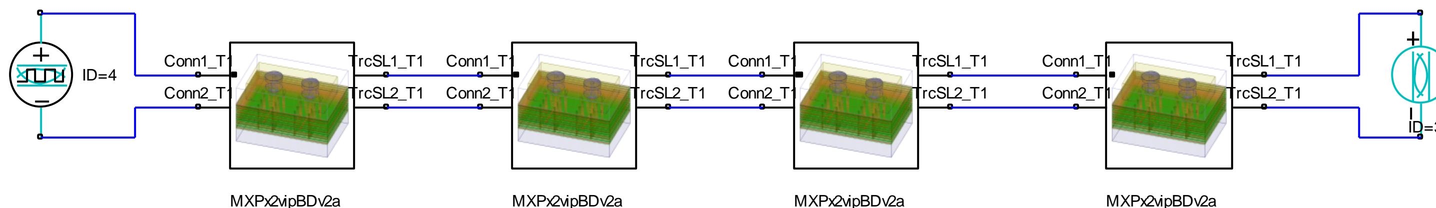


Vivek Telang Equalization for High-Speed Serdes 29 of 67

DFE makes a bit decision based upon “weighted” bit decisions for N previous bits.

Diagrams above courtesy of Vivek Telang, Broadcom

Final model of 4 series vias for eye diagrams on next page



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28.125 Gbps EYE DIAGRAM RESULTS FOR FOUR (4) VIAS IN THE PATH, VARIOUS STUB/OFFSET CASES

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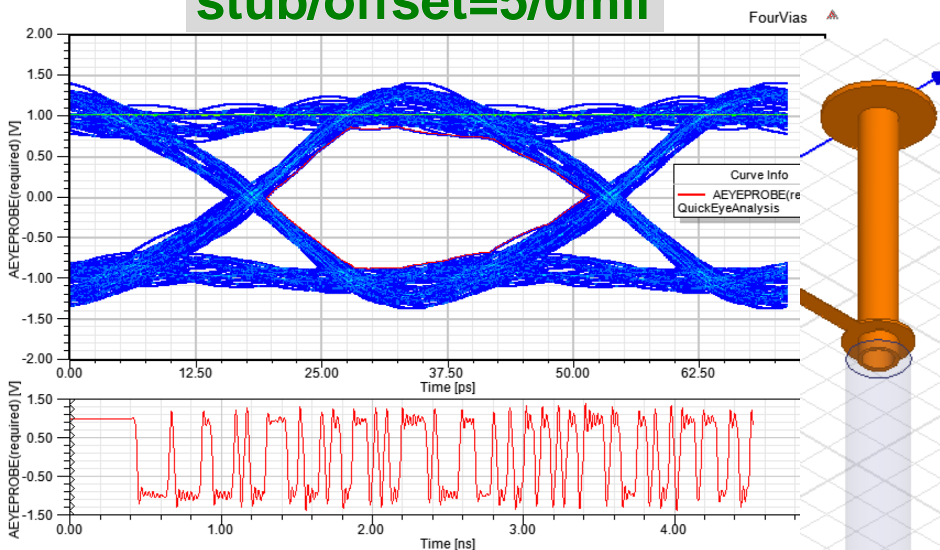
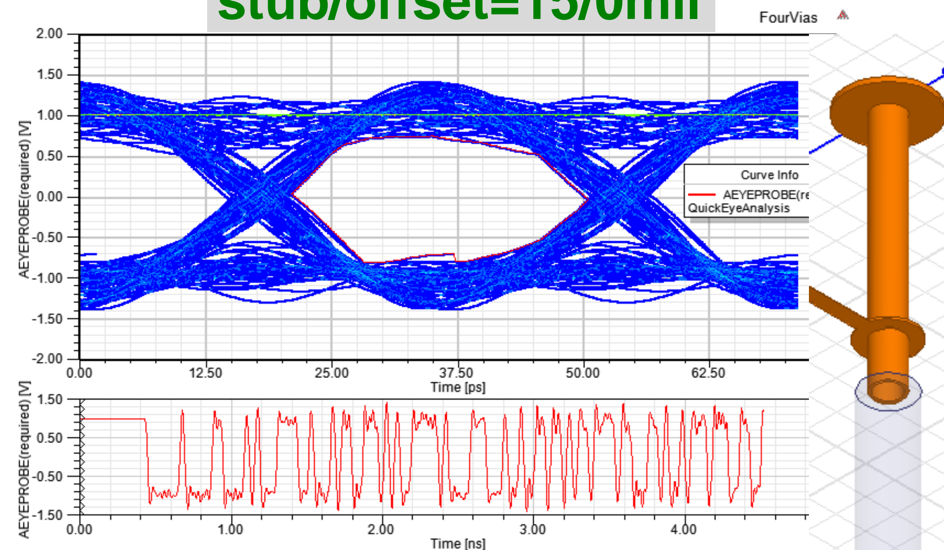
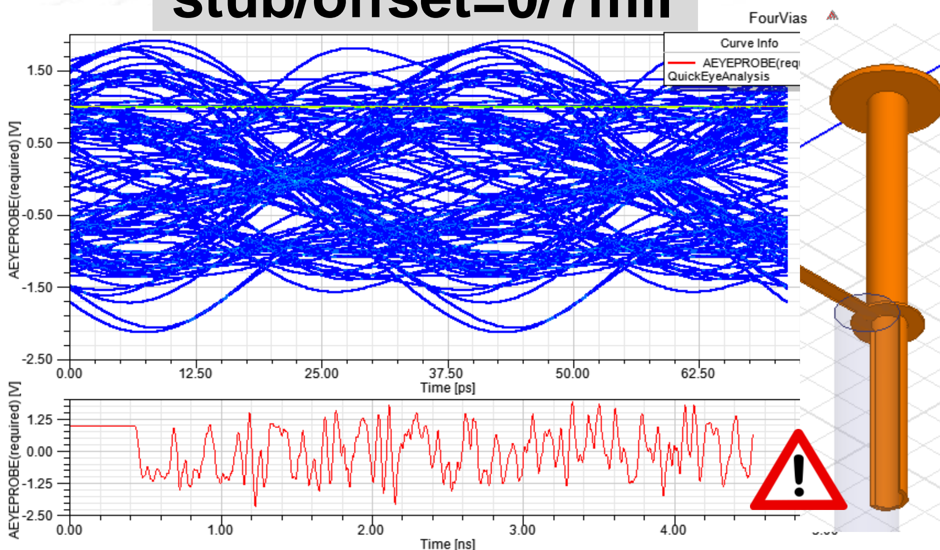
stub/offset=5/0mil



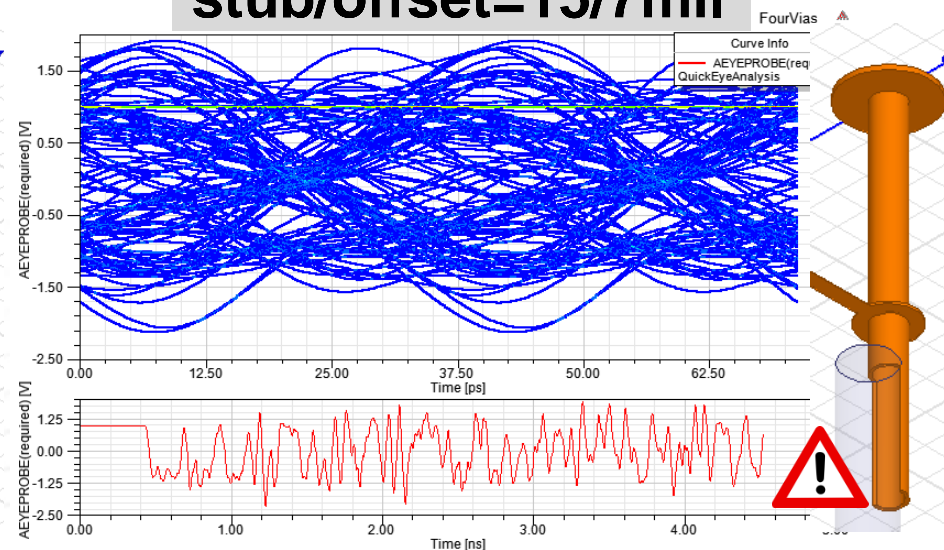
stub/offset=15/0mil



stub/offset=0/7mil



stub/offset=15/7mil



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COMPARISON OF DATA PATTERN FOR PARTIAL BARREL DUE TO OFFSET BACKDRILL VS. NOT

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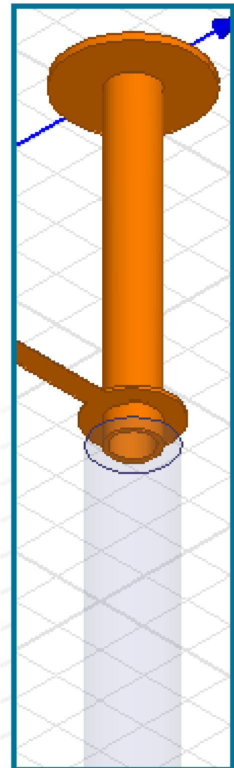
The severity of combined reflections is so severe, it is doubtful that even advanced chip circuitry can correct it.



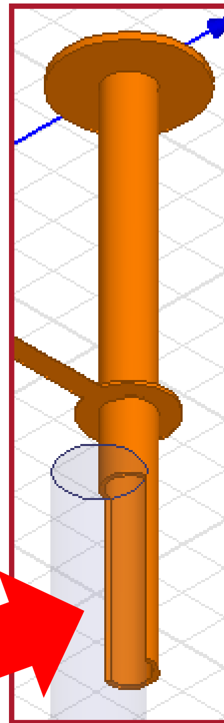
Sample signal at RX (after "perfect" loss compensation) with various stub & backdrill offset

stub=5mils, offset=0mils, 4vias

stub=15mils, offset=7mils, 4vias

Signal level (Volts): 2.5, 2, 1.5, 1, 0.5, 0, -0.5, -1, -1.5, -2, -2.5

Time (nsec): 2.5, 2.7, 2.9, 3.1, 3.3, 3.5, 3.7, 3.9



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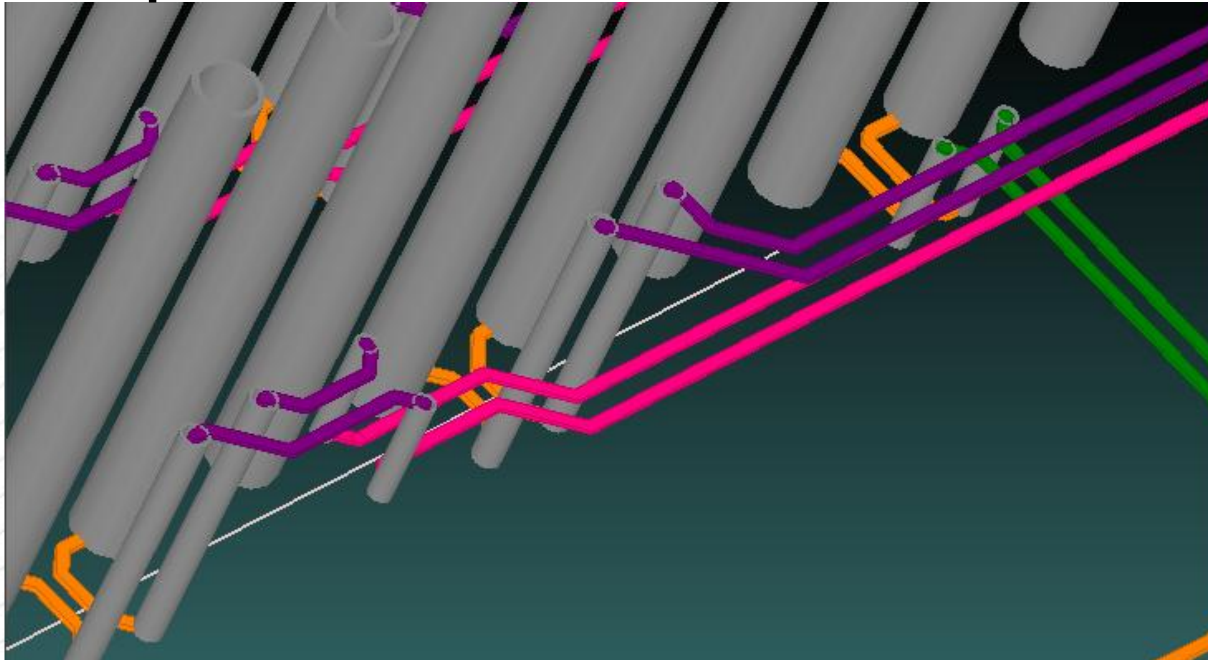
ALTERNATIVES TO SINGLE-LAM BACKDRILLED PCBS

- **Multiple lamination/sequential stackup:**
  - More costly than single-lam.
  - More difficult for very large and high-layer count PCBs:
    - Modern high-density switch platforms use 25 to > 50 PCB layers.

Example multi-lam PCB: BCM99006J47/116792.



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CONCLUSION

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The traditional PCBA remains the preferred solution for most short-reach, high-density chip-to-chip and chip-to-module links.

- Traditional single-lam cycle backdrilled system PCBAs still suffice for 28 Gbps NRZ signaling and similar links (i.e., BRCM 56 Gbps PAM-4 signaling), when IC's SerDes I/O circuit designs feature appropriate loss, dispersion, and reflection compensation.
- These links can be established successfully for path lengths up to 1 meter, using appropriate (low-loss) materials and fabrication.
- These links can successfully include high-quality connectors and vias, such that board-to-board transmission is feasible.
- Via stub length variations that are common in current-day processes (i.e., up to ~15 mils) can be tolerated in these systems.
- Misaligned backdrilling, which results in partial stub, is nearly the same as not backdrilling at all, and results in reflections that are probably too severe for links to be reliable.

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