Reduce EMI and Improve Power Delivery with Embedded Capacitance

Types of **EMBEDDED** capacitance

1.

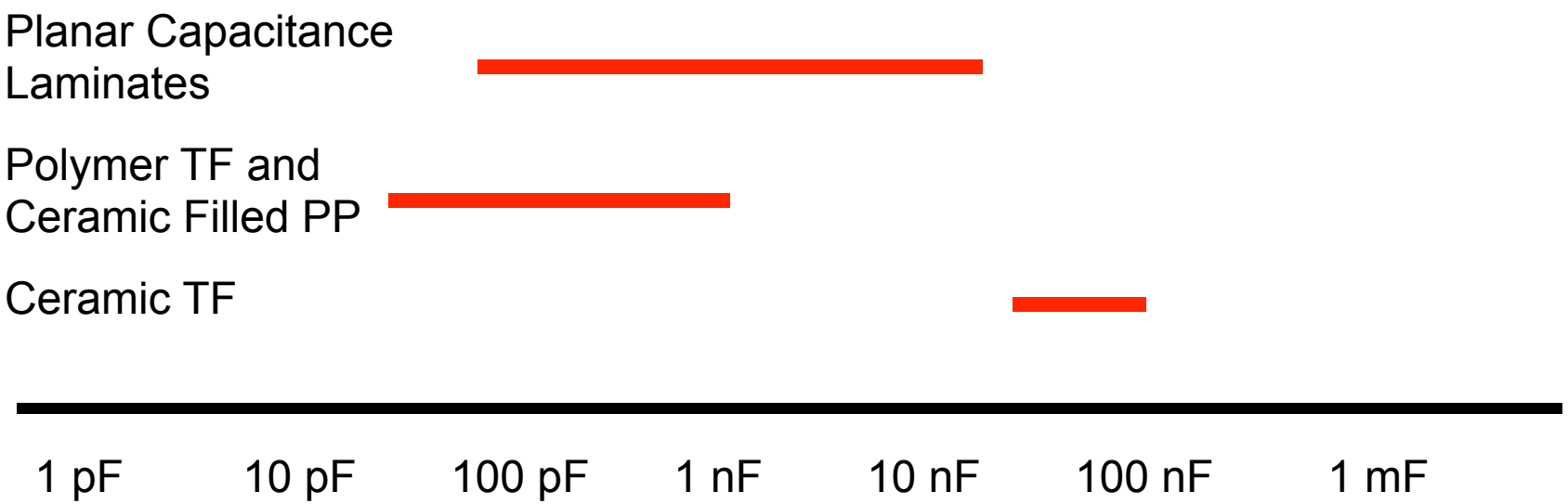
- Planar
  - Shared
  - Discrete

2.

- Discrete
  - Polymer Thick Film
  - Ceramic Thick Film
  - Ceramic Filled Photopolymer

3.

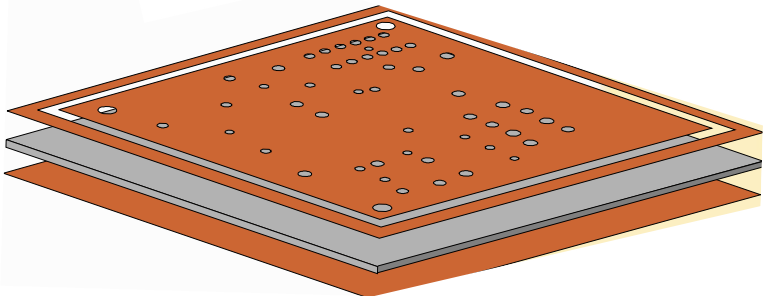
- Discrete in Cavity



Courtesy of Gary Ferrari, FTG

Types of **EMBEDDED** capacitance

Planar Layers in PCB



Use this is an existing stack up of layers in the PCB

Plus
- Easy
- Addresses many issues with PCB design and power delivery
- Same or lower cost
- More reliable

Minus
- Limited capacitance currently available

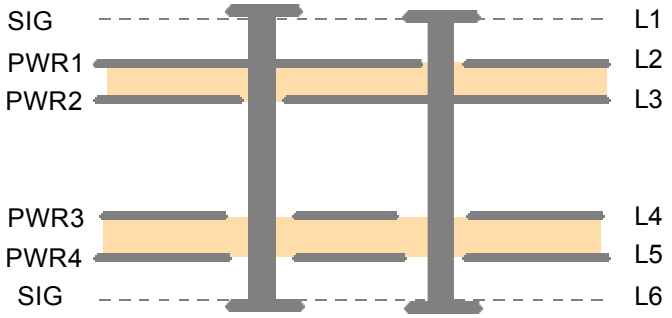
Discrete in PCB cavity

Leave a cavity open in the PCB and then place the capacitor and solder in place and then fill the cavity

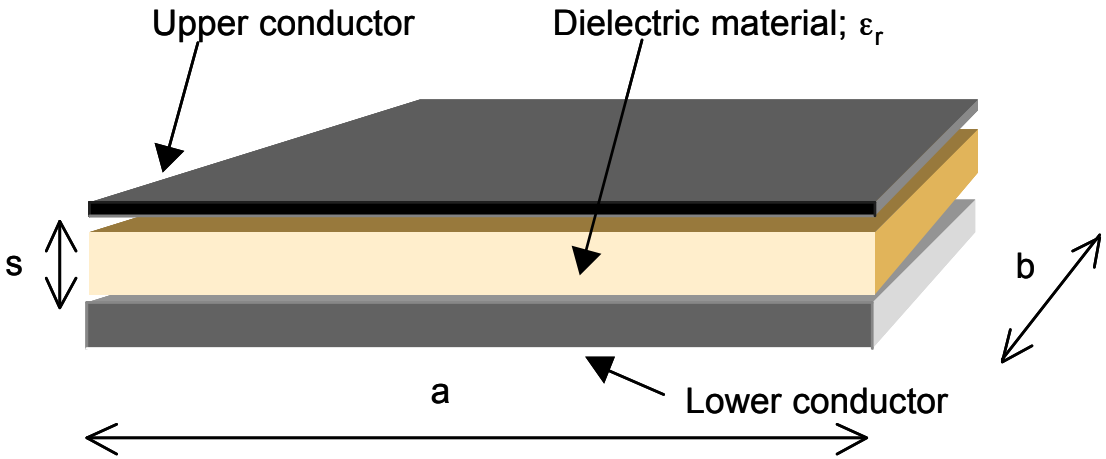
Plus
- Full values of capacitance available

Minus
- Manufacturing and design difficult
- Costly
- Less reliable

What is a Planar Capacitor?



Conductive plane pair with dielectric separation:



The current planar ultra-thin material sets:

1. Polymer film such as polyimide (**Dupont**)
2. Polymer film and resin combination (**Dupont and Oak-Mitsui**)
3. Unsupported resin filled with higk Dk or other types of particles (**3M and Oak-Mitsui**)

2014 Survey by IPC

1. Of the companies in the survey 30% of their PCB's are using Embedded Capacitance
2. In 2015 and beyond the expectation are that this will more than double

Why Embedded Capacitance and Why Thin Dielectrics?

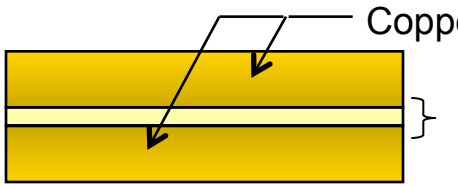
- Better PDN
- Lower profile
- More design space
- Low inductance
- Low impedance
- Reduced noise
- Space…
- Thickness reduction…
- Weight reduction
- Higher reliability
- In some designs better thermal transfer
- Etc.

Solution

High speed computing boards
Servers, Routers, Super computers

Power distribution improvement

Uitra-Thin substrate
for use as embedded capacitor

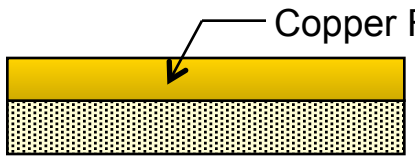


8～24 **micron Polymer Dielectric**

Module boards
Cell phones, PDA, Note book computers

Miniaturization / HDI

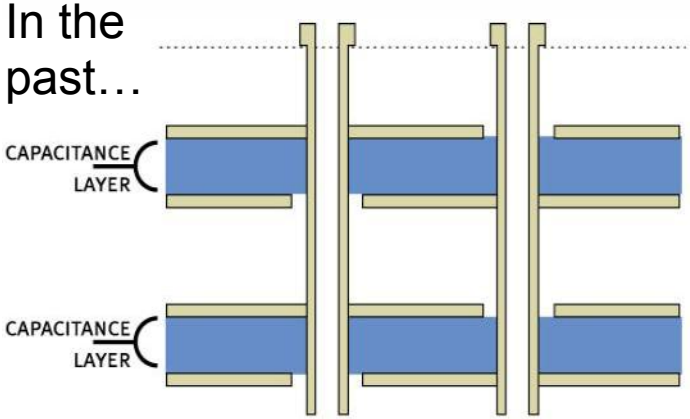
Hi-Dk RCF
for used as embedded capacitor



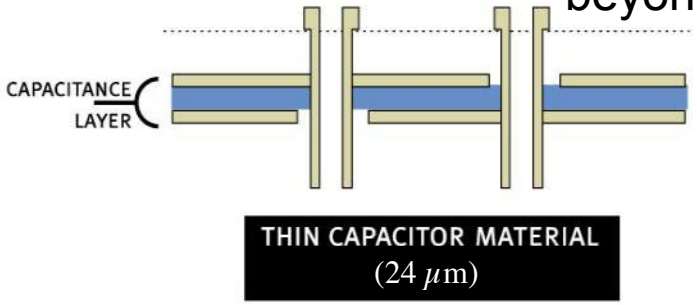
16 **micron Polymer Dielectric with Hi-Dk Filler**

Need for thinner (<25micron) Embedded Capacitance Materials

In the past…

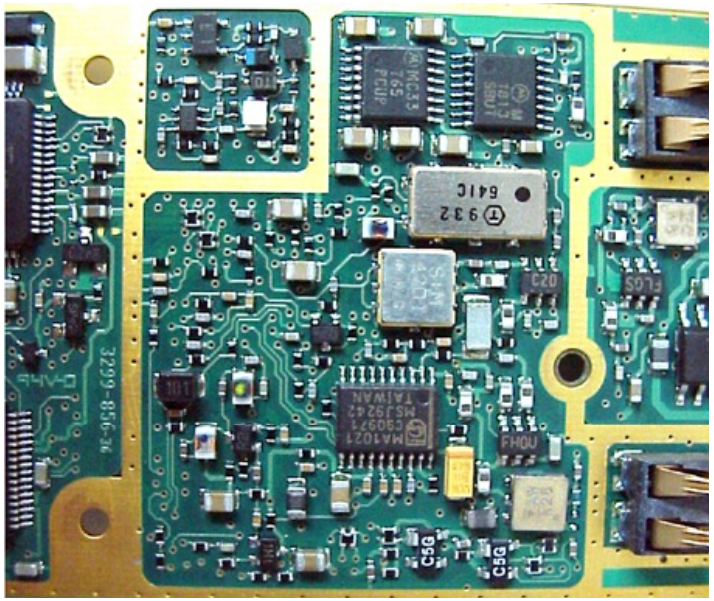


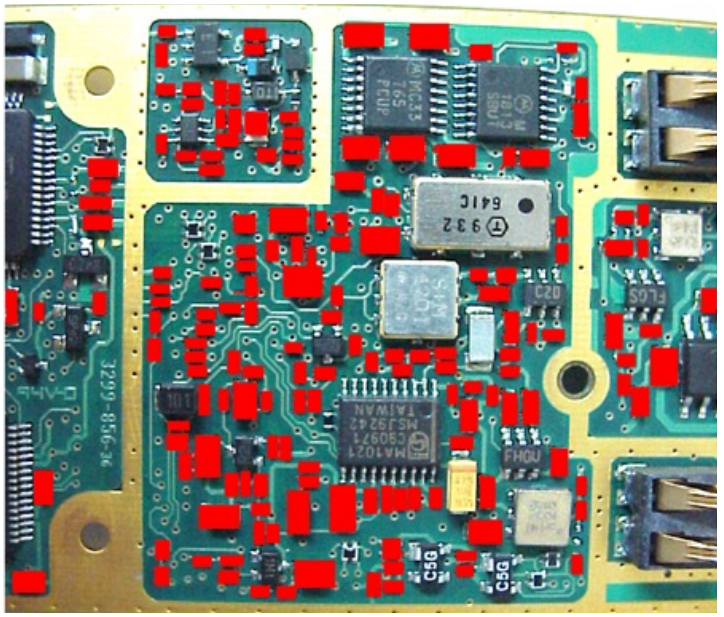
Today and beyond…



Expectation by using thin planar capacitance material
- Improved electrical performance
- Reduce system cost
- Reduce board thickness
- Reduce prototype revisions

Component density is reaching its limit





Passive components

Source: Richard Ulrich University of Arkansas

High capacitance and capacitance uniformity are key

8 Layer HDI Design

With Decoupling Caps

Without Decoupling Caps

With shared planar embedded capacitance

Courtesy of Gary Ferrari, FTG

14 Layer Design

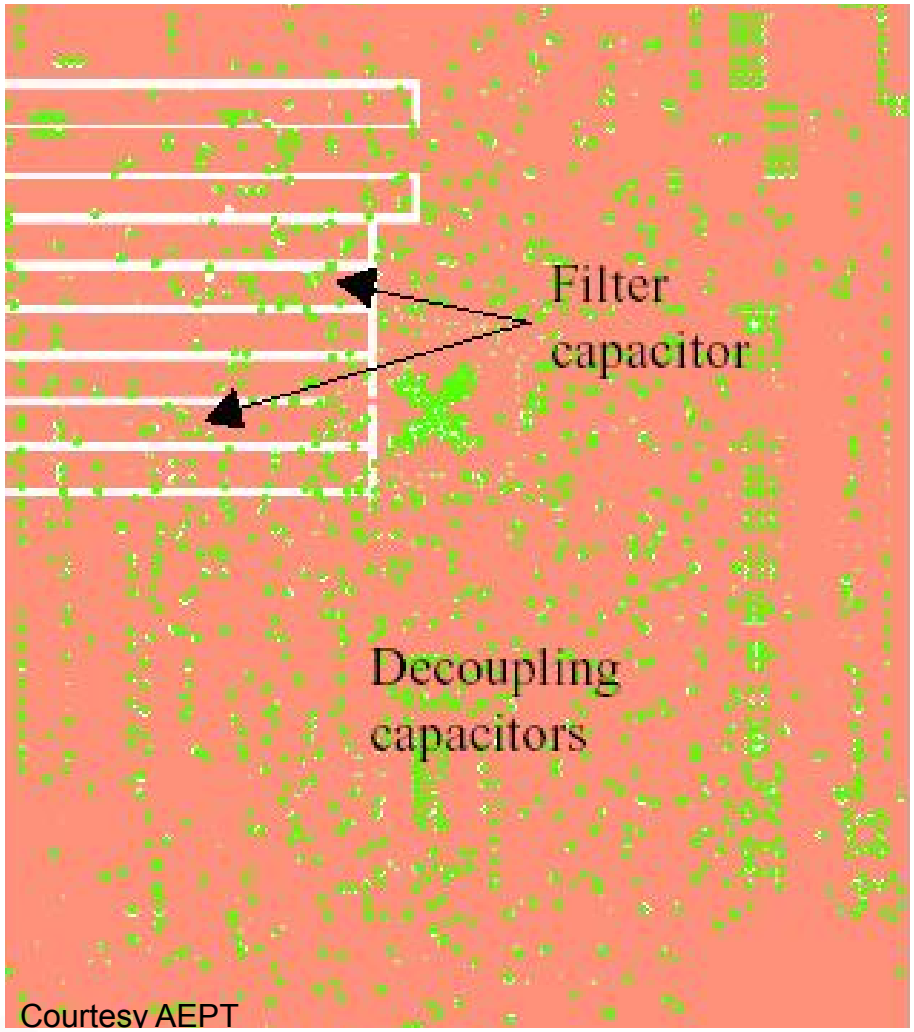
With Decoupling Caps

Without Decoupling Caps

Courtesy of Gary Ferrari, FTG

With shared planar embedded capacitance

Discrete Capacitors designed into a Distributed Capacitor Plane



Courtesy AEPT

Courtesy of Gary Ferrari, FTG

Two Approaches to Embedded Capacitance

Solution

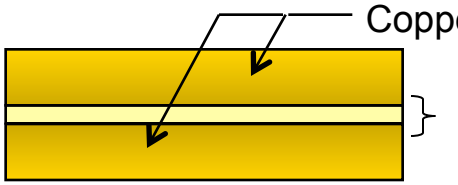
High speed computing boards
Servers, Routers, Super computers

Power distribution improvement

Module boards
Cell phones, PDA, Note book computers

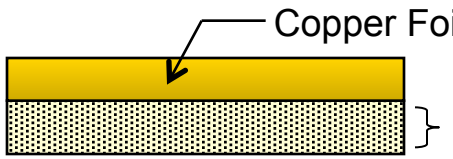
Miniaturization / HDI

Uitra-Thin substrate
for use as embedded capacitor



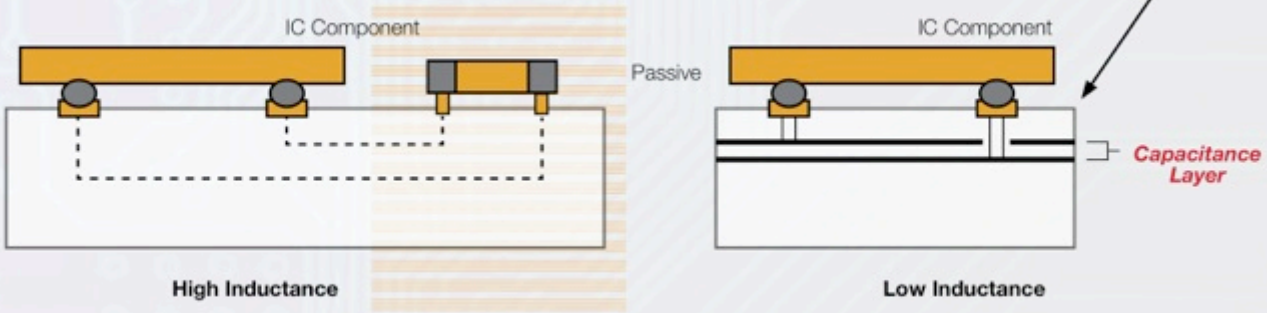
8～24 **micron Polymer Dielectric**

Hi-Dk RCF
for used as embedded capacitor



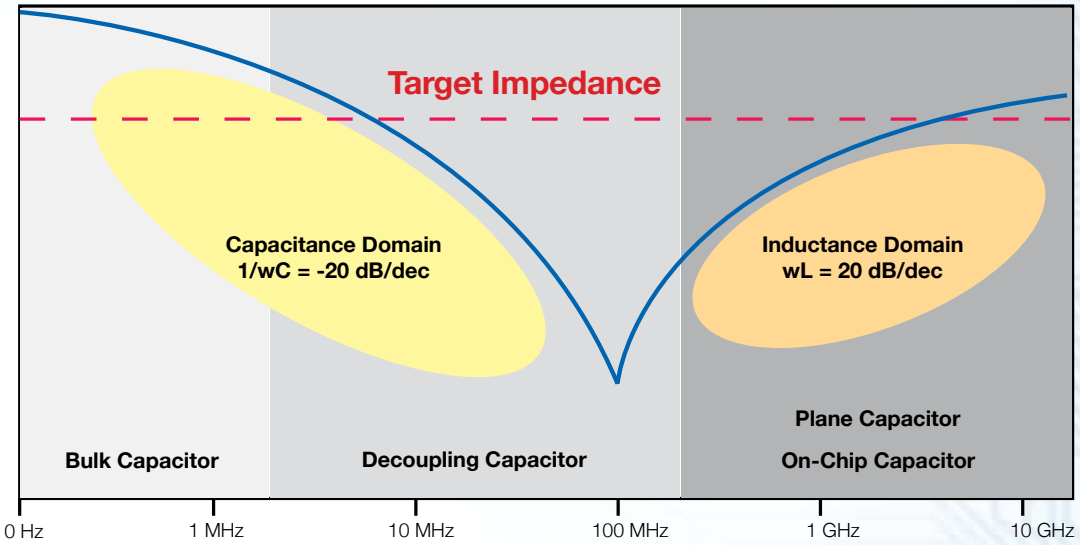
16 **micron Polymer Dielectric with Hi-Dk Filler**

FaradFlex® greatly reduces power buss noise and eliminates the need for many decoupling capacitors

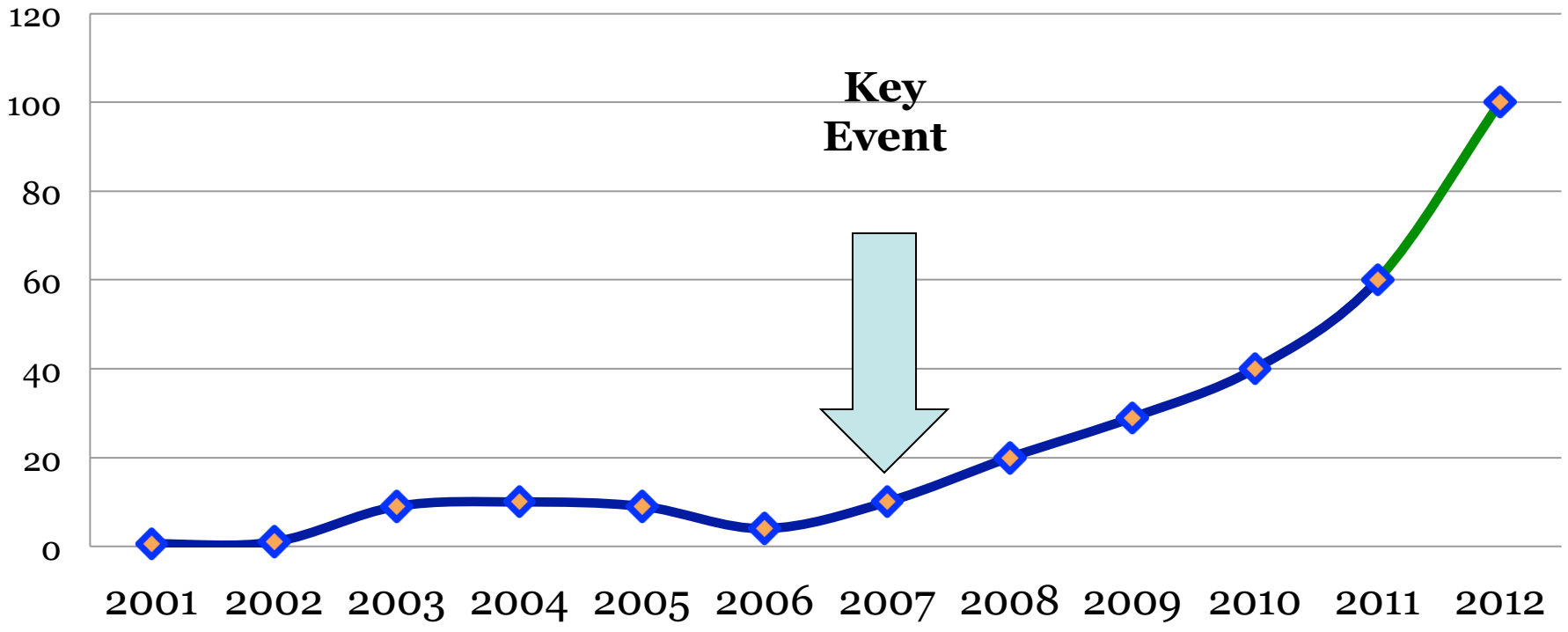


FaradFlex® compared to traditional material

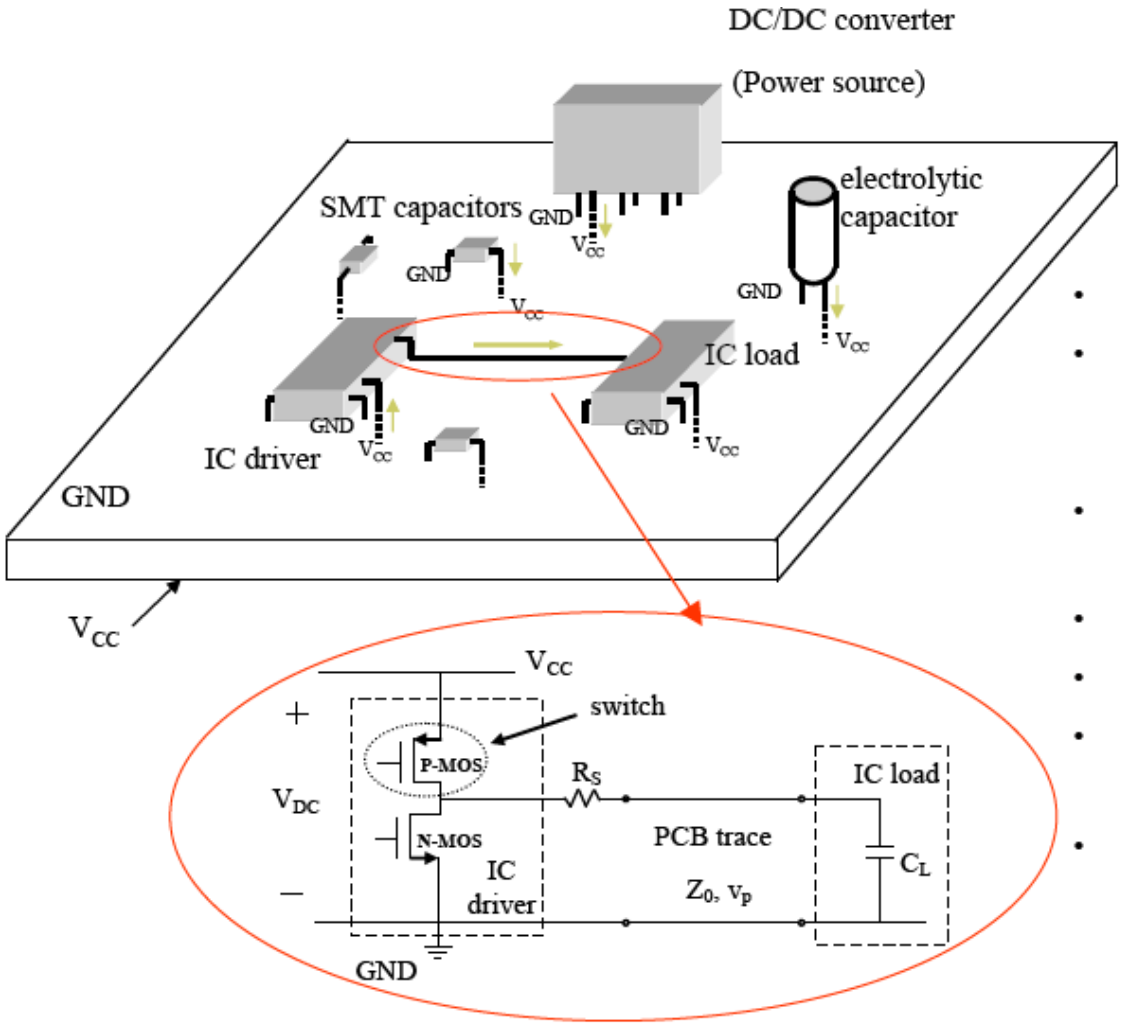
- *FaradFlex*® is 1/2 to 1/6 the thickness compared to the typical “thinnest” laminate using glass cloth reinforcement.
- *FaradFlex*® increases thermal transfer from the PCB due to the ultra thin power-ground substrate.
- Dielectic withstanding voltage is typically 10 times better with *FaradFlex*® than the traditional FR-4 laminates and similar materials.



Background / Motivation



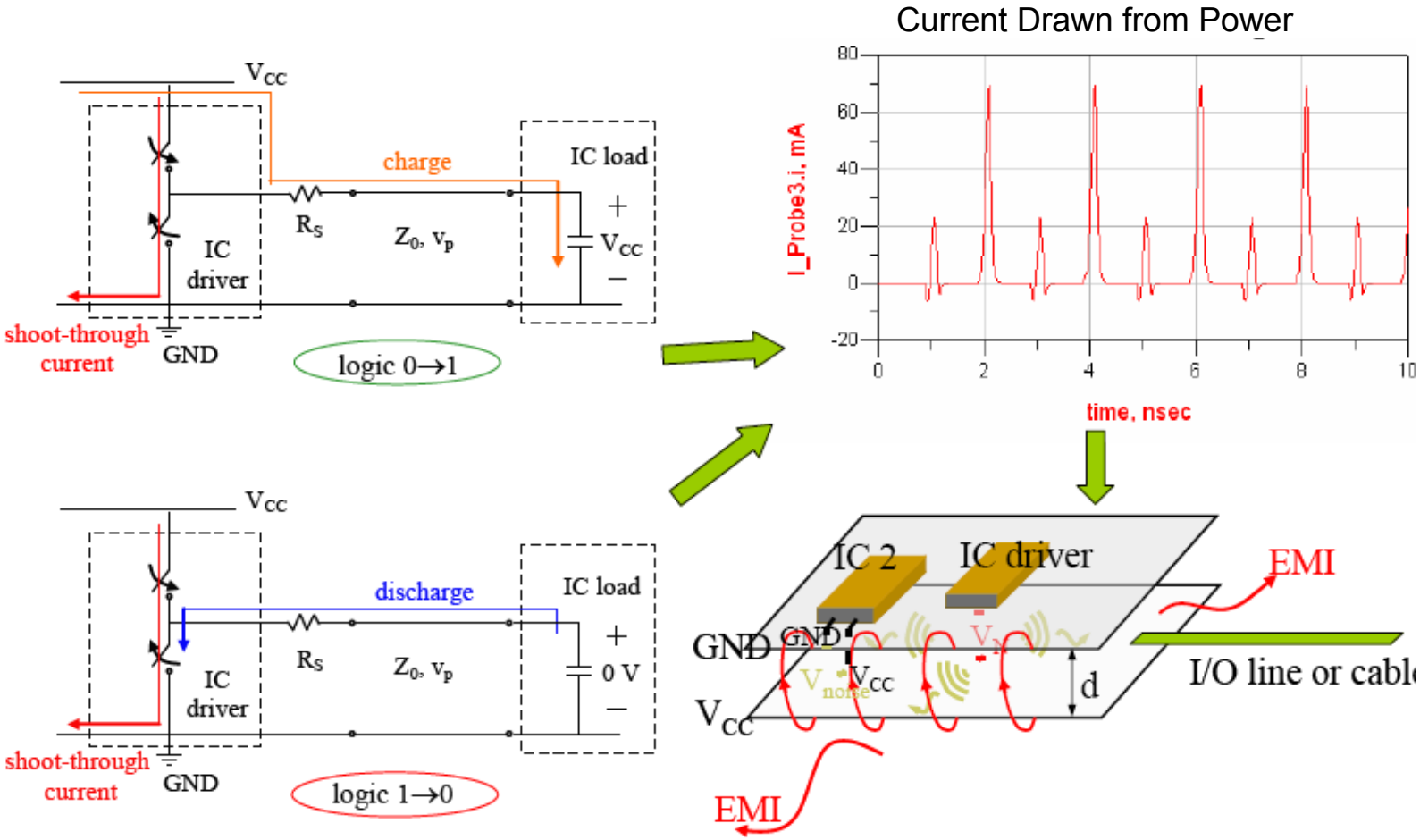
TYPICAL/ TRADITIONAL POWER DISTRIBUTION NETWORK



- Capacitor interconnects;
- Individual capacitor values and packaging forms;
- Number of capacitors needed;
- Capacitor placement;
- PCB stack-up;
- Power/ground plane pair geometry;
- Segmentation and isolation

Courtesy of Dr. Jun Fan

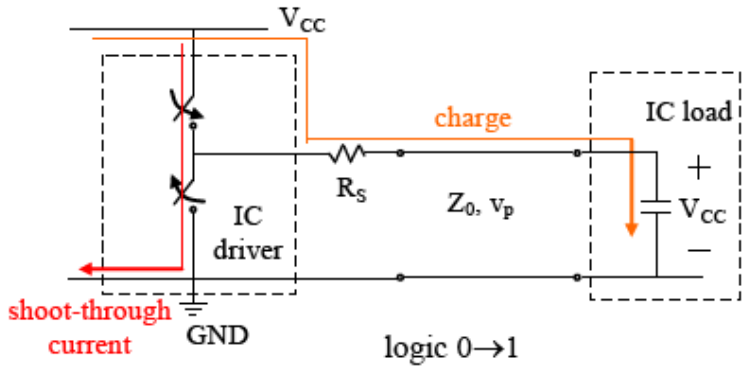
Device Switching And Noise Current

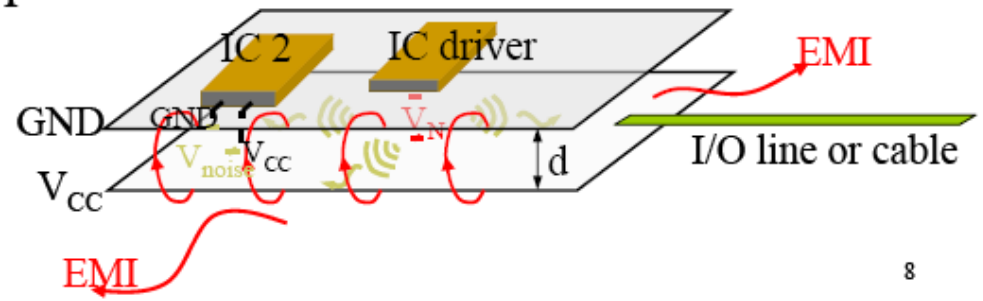


J. L Knighten, B. Archambeault, J. Fan, et. al., "PDN Design Strategies: IV. Sources of PDN Noise," *IEEE EMC Society Newsletter*, Winter 2007, Issue No. 212, pp. 66-76.

PDN Design Objectives

1. Ensure charge supply for logic transitions
   - Enough capacitance to store charge
   - Enough charge readily available for short transitions
2. Minimize noise voltage distribution on the V_{CC}/GND plane pair
   - Low power bus impedance over frequency
   - Noise decoupling
   - Noise isolation





Courtesy of Dr. Jun Fan

STANDARD Dk PRODUCT

Properties	Test Method	MC24M	MC12M	MC8M	MC25L
Dielectric Thickness, µm	IPC or others	22	12	8	25
Cp @1 MHz, nF/in^2(pF/cm^2)	Nominal	**1.2 (180)**	**1.9 (300)**	**3.1 (480)**	**1.0 (130)**
Dk (Dielectric Constant) @ 1 MHz/ 1 GHz	IPC TM-650 2.5.5.2	4.4/ 3.5	4.4/ 3.5	4.4/ 3.5	3.9/ 3.8
Df (Loss Tangent) @1 MHz/ 1 GHz	IPC TM-650 2.5.5.2	0.015/ 0.016	0.015/ 0.020	0.016/ 0.021	**0.004/ 0.005**
Peel Strength, lbs/ linear in.	IPC TM-650 2.5.5.2	8	8	5	8
Dielectric Strength, kV/mil	IPC TM-650 2.4.9	>7	>7	>5	>7
Tensile Strength, MPa (kpsi)	ASTM D-882A	219 (31.8)	194 (28.2)	126 (18.3)	227 (32.9)
Elongation, %	ASTM D-882A	36.0	13.5	8.5	47.0
CTE, ppm/°C, x-y (40-200°C), TMA	TMA	24	23	32	30
Dielectric Withstanding Voltage (Hi-Pot test)	IPC TM-650 2.5.7.2	PASS (500V)	PASS (500V)	PASS (500V)	PASS (500V)
Thermal Stress (20Sec Float @288C), Times	-	>10	>10	>10	>10
THB, 85°C/85%RH/ dc bias	1000hr	PASS	PASS	PASS	PASS
Flammability/Temp Rating	UL	V0 130°C	V0 130°C	V0 125°C	V0 130°C
PWB Processing	-	Both sides	Both sides	Both sides	Both sides

Note: This chart provides the typical values for FaradFlex product.

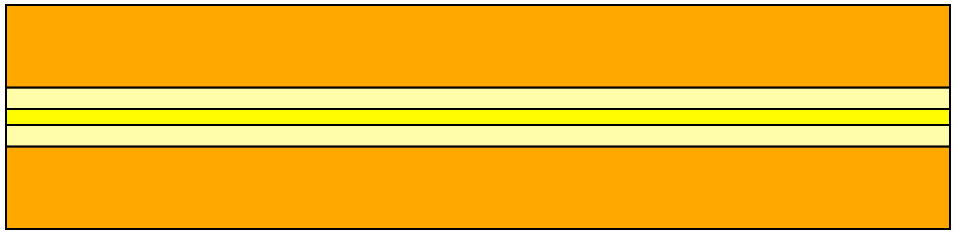
HIGH Dk PRODUCT

Properties	Test Method	MC12TM	MC8TM	MC16T	MC25ST	MC25LD
Dielectric Thickness, µm	IPC or others	12	8	16	25	25
Cp @1 MHz, nF/in^2(pF/cm^2)	Nominal	**4.2 (650)**	**7.1 (1100)**	**11 (1700)**	**4.3 (660)**	**2.1 (320)**
Dk (Dielectric Constant) @ 1 MHz/ 1 GHz	IPC TM-650 2.5.5.2	10.0/ 9.5	10.5/ 10.0	30.0/ 25,0	18.5/ 18.0	8.3/ 7.8
Df (Loss Tangent) @ 1 MHz/ 1 GHz	IPC TM-650 2.5.5.2	0.015/ 0.020	0.020/ 0.021	0.034/ 0.036	**0.004/ 0.008**	**0.0027/ 0.0032**
Peel Strength, lbs/ linear in.	IPC TM-650 2.5.5.2	5	5	5	4	4
Dielectric Strength, kV/mil	IPC TM-650 2.4.9	5	4	2	2	2
Tensile Strength, MPa (kpsi)	ASTM D-882A	153 (22.2)	127 (18.4)	NA	NA	NA
Elongation, %	ASTM D-882A	31.4	14.0	NA	NA	NA
CTE, ppm/°C, x-y (40-200°C), TMA	TMA	28	22	17(α1) 42(α2)	32(α1) 97(α2)	55
Dielectric Withstanding Voltage (Hi-Pot test)	IPC TM-650 2.5.7.2	PASS (500V)	PASS (250V)	PASS (100V)	PASS (100V)	PASS (100V)
Thermal Stress (20 Sec Float @288C), Times	-	>10	>10	>10	>10	>10
THB, 85°C/85%RH/ dc bias	1000hr	PASS	PASS	PASS	PASS	PASS
Flammability/Temp Rating	UL	V0 130°C	V0 130 °C	V0 130°C	Pending	Pending
PWB Processing	-	Both sides	Both sides	Sequential	Sequential	Sequential

Note: This chart provides the typical values for FaradFlex product.

Embedded Capacitance Materials

First Type of Embedded Capacitance Laminate

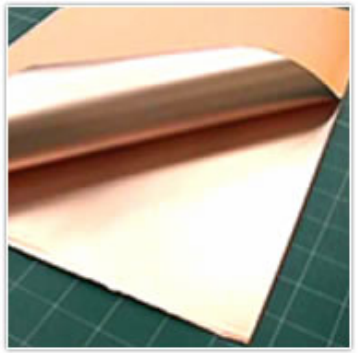


Laminate constructed with:

- **Copper**
- **Epoxy or other type resin bonded to a high performance polymer film**

Includes These:

MC24M, MC12M, MC8M, MC25L



CHARACTERISTICS

Most cost effective.

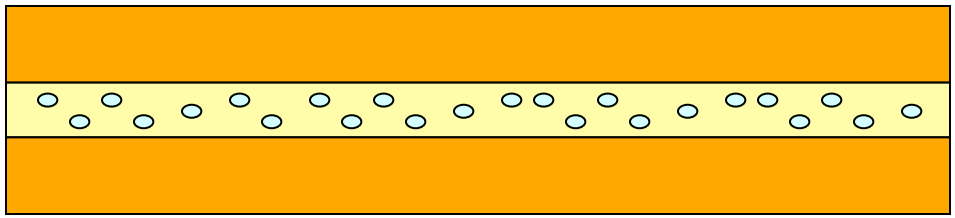
Best processabilty

Longest in history

Highest reliability

Embedded Capacitance Materials

Second Type of Embedded Capacitance Laminate

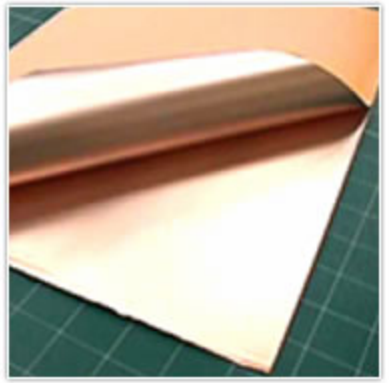


Laminate constructed with:

- Copper
- **Unsupported epoxy resin** with barium titanate or other particles dispersed in the resin

Includes These:

MC16T, MC25ST, MC25LD



CHARACTERISTICS

Most costly laminate

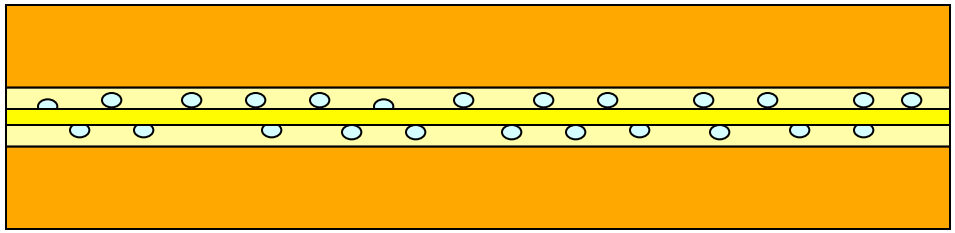
Least processabilty

Highest Dk, Highest capacitance

Lowest reliability

Embedded Capacitance Materials

Third Type of Embedded Capacitance Laminate

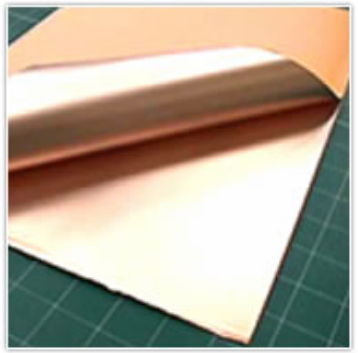


Laminate constructed with:

- Copper
- **Supported epoxy resin and polymer film composite,** barium titanate particles or other material dispersed

Includes These:

MC12TM, MC8TM



CHARACTERISTICS

Mid to more costly laminate

High level of processabilty

Very High Dk, Very High capacitance

High reliability, High withstanding voltage

TYPICAL PCB DESIGN AND STACK UP

Replace the Existing Power Ground Layer with FaradFlex

for use as power distribution layer

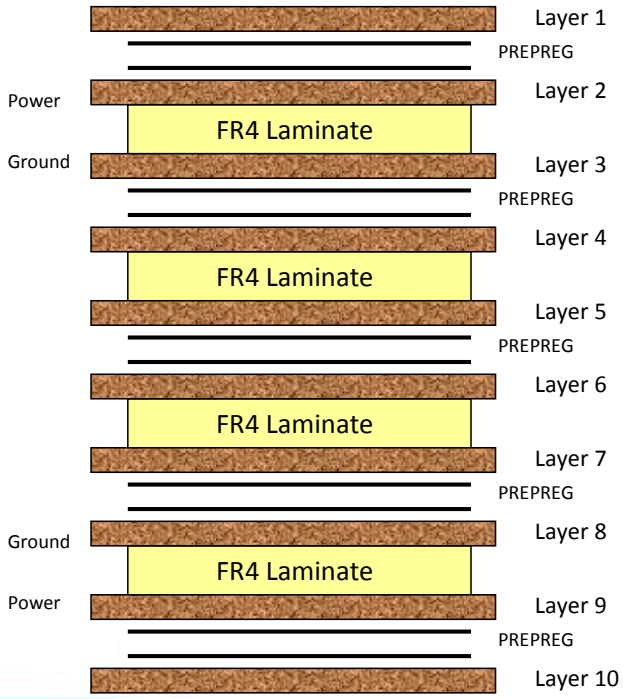
EXAMPLE 1

10 LAYER PCB STACK-UP

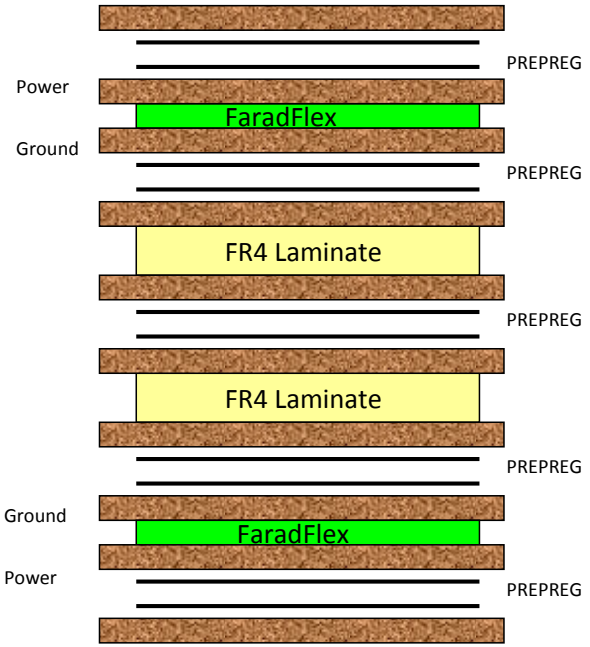
With **2** Power-Ground layers at **L2/L3** and **L8/L9**

(using FaradFlex in the Power-Ground allows for buried capacitance)

With FR4 Power-Ground

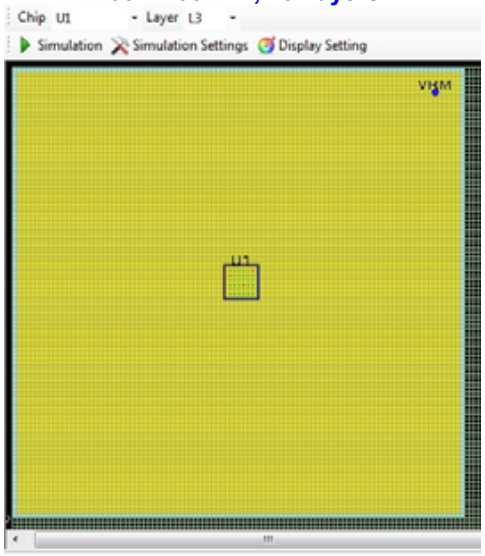


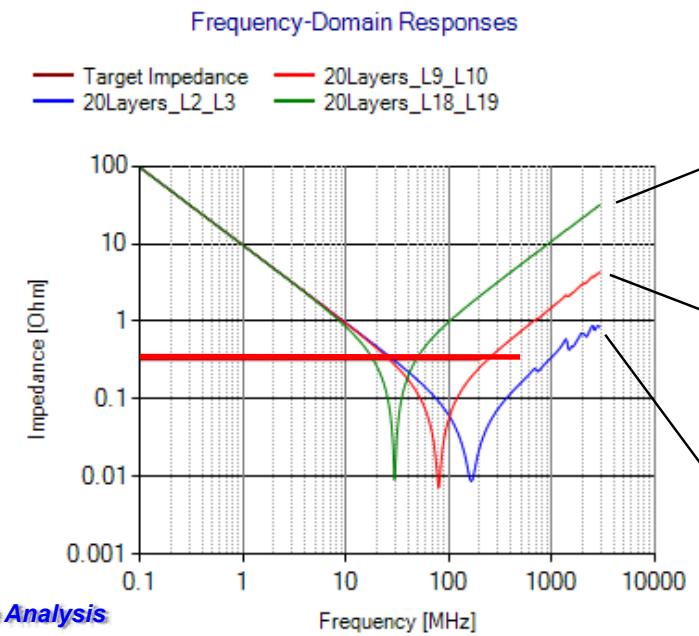
With IMC24M Power-Ground

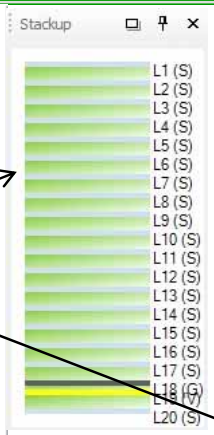


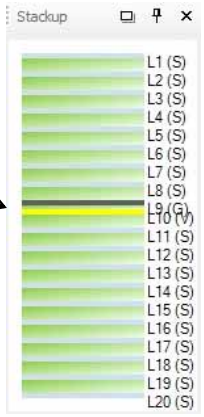
Where to place FaradFlex?

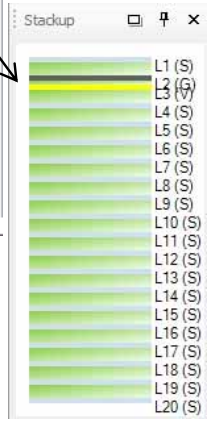
100 x 100 mm, 20 Layers

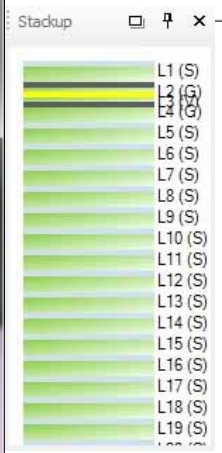




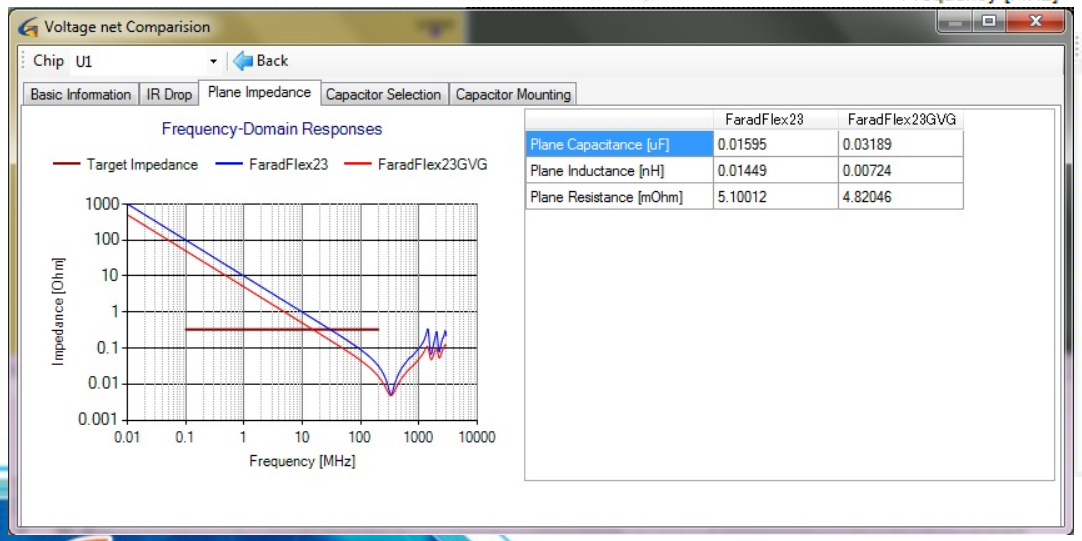








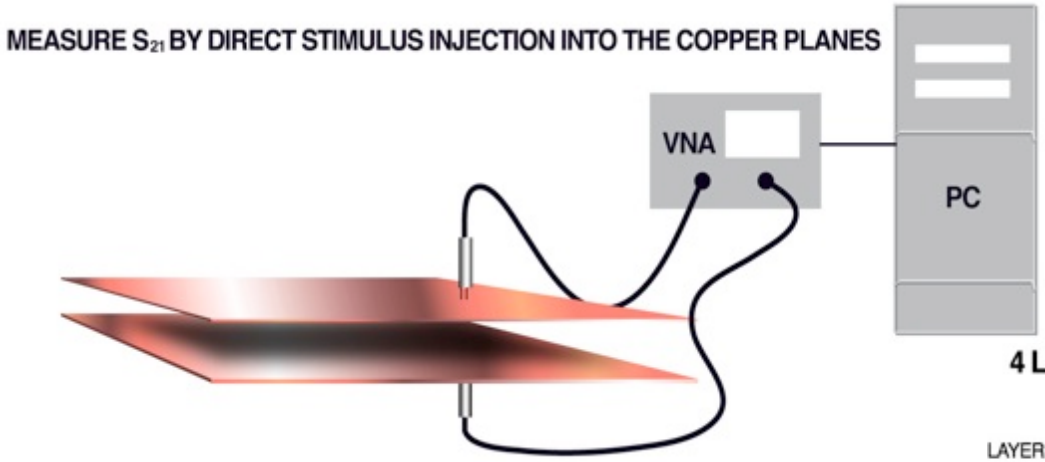
G-V-G Structure Analysis

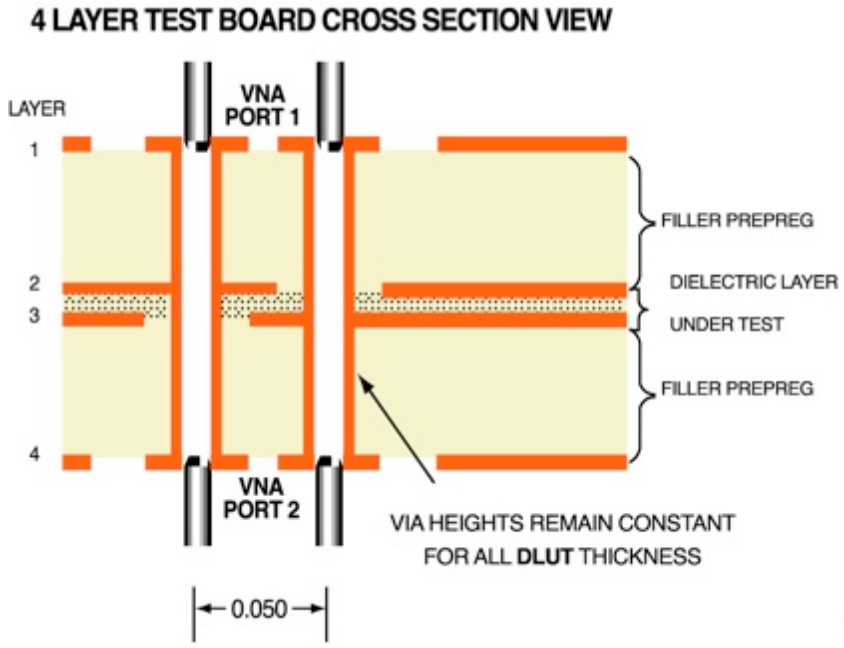


	FaradFlex23	FaradFlex23GVG
Plane Capacitance [uF]	0.01595	0.03189
Plane Inductance [nH]	0.01449	0.00724
Plane Resistance [mOhm]	5.10012	4.82046

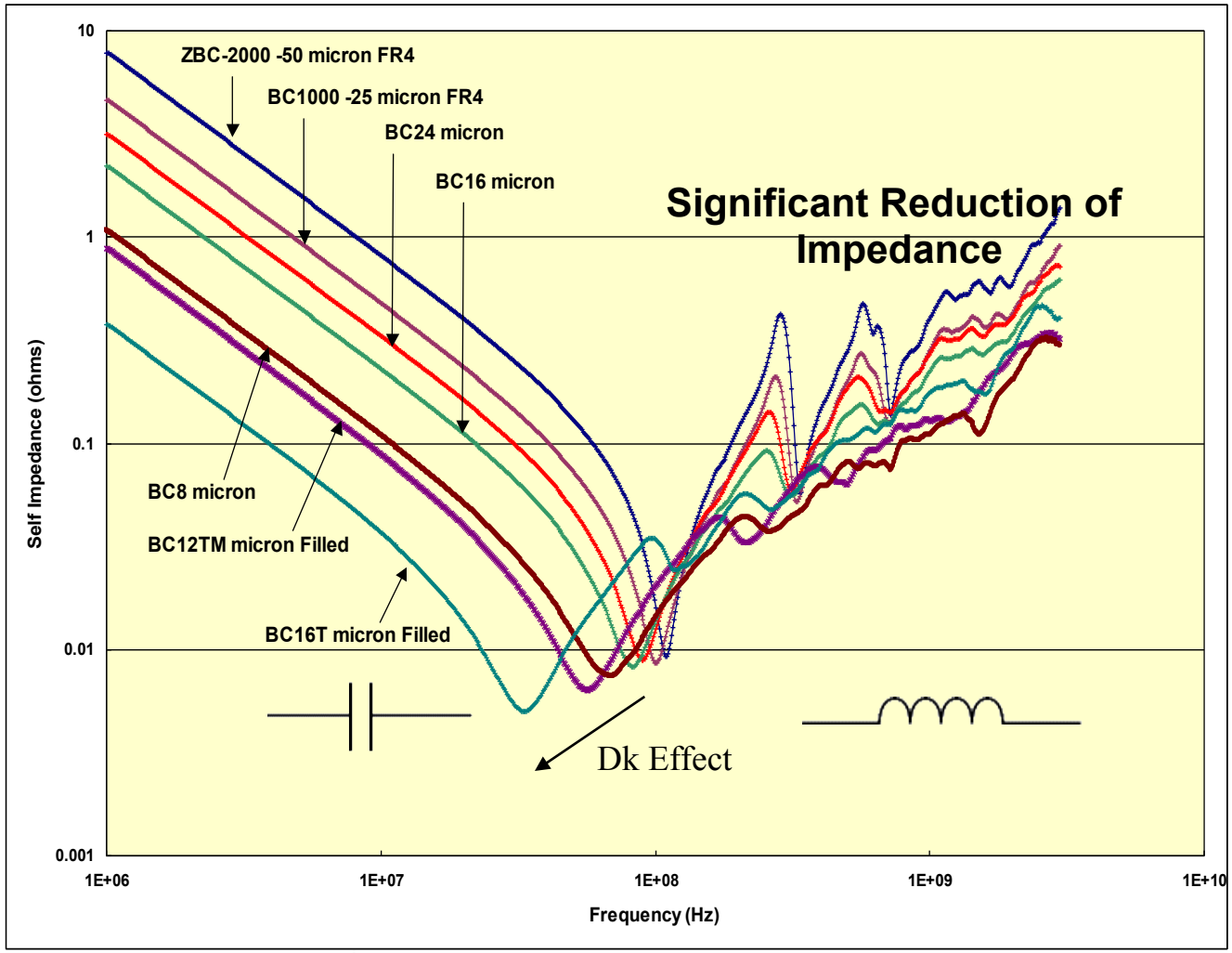
IMPROVED IMPEDENCE/ INDUCTANCE

PCB Electrical Performance





PCB Electrical Performance

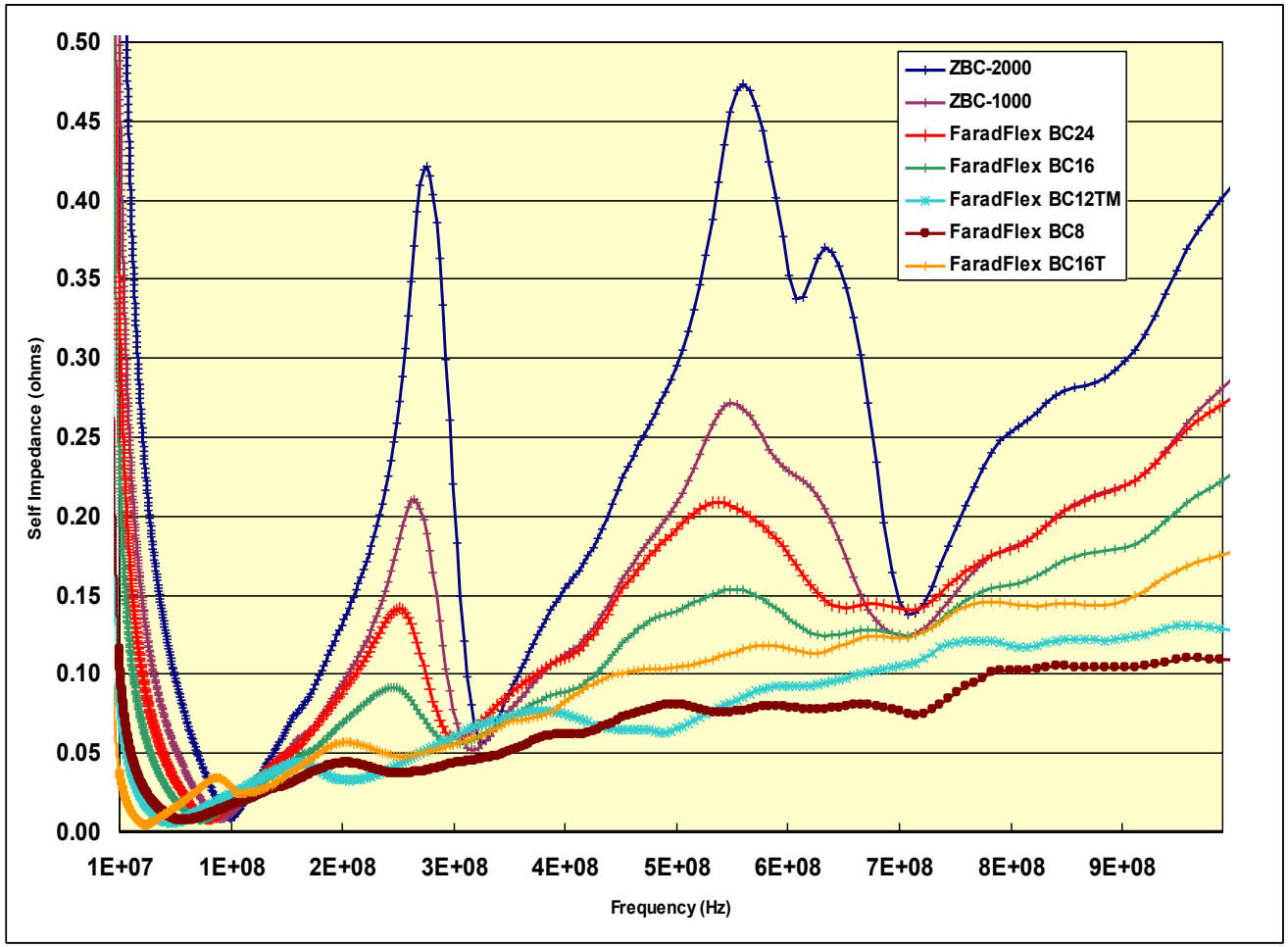


Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

Discrete capacitors of 0.1µF have a resonance frequency of about 15 MHz
Discrete capacitors of 0.01µF have a resonance frequency of about 40 MHz.

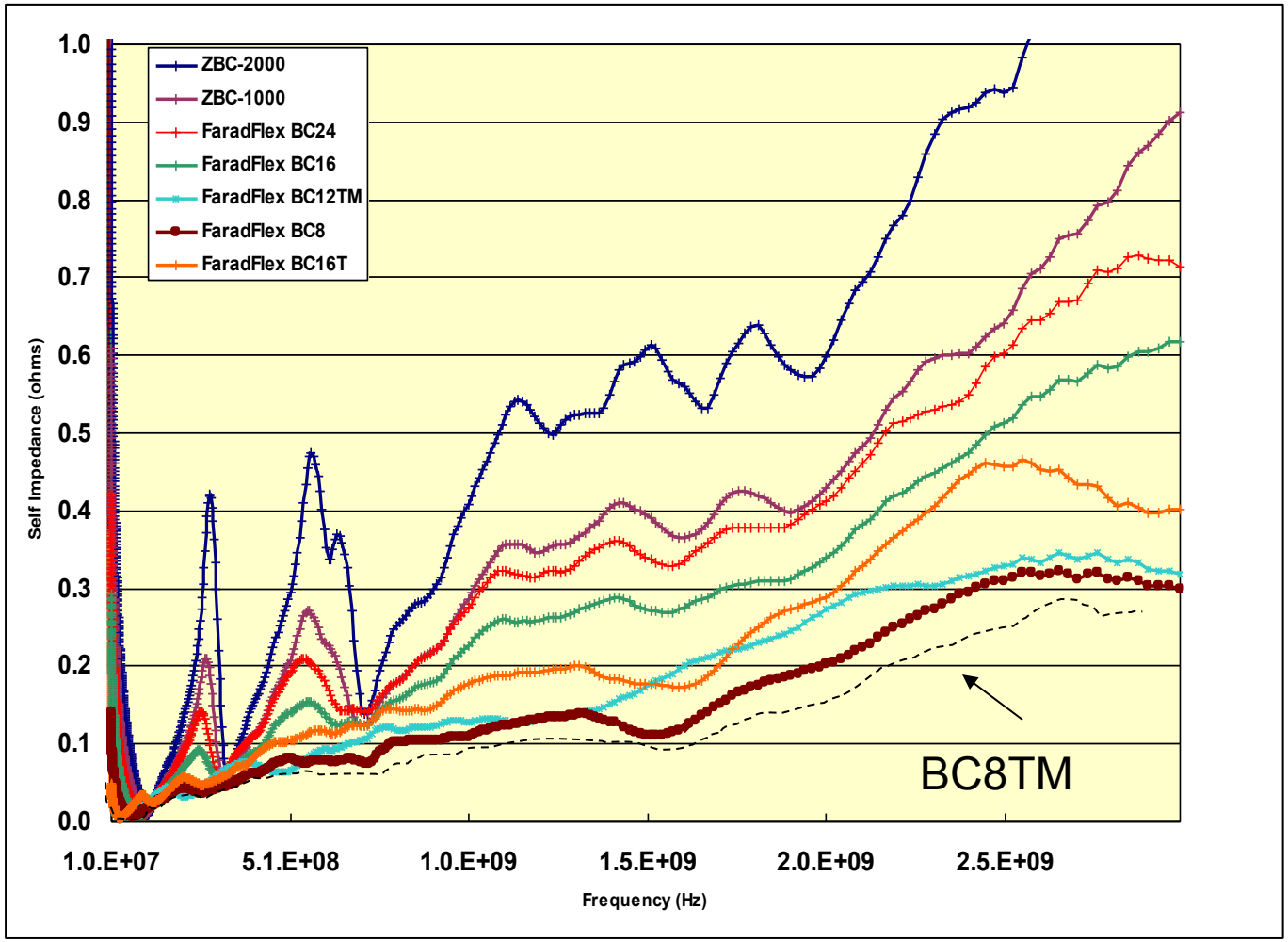
PCB Electrical Performance (Up to 1 GHz)



Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

PCB Electrical Performance (Up to 3 GHz)



Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
MC24M	40
MC16M	64
MC12M	76
MC8M	124
MC12TM	180
MC16T	440

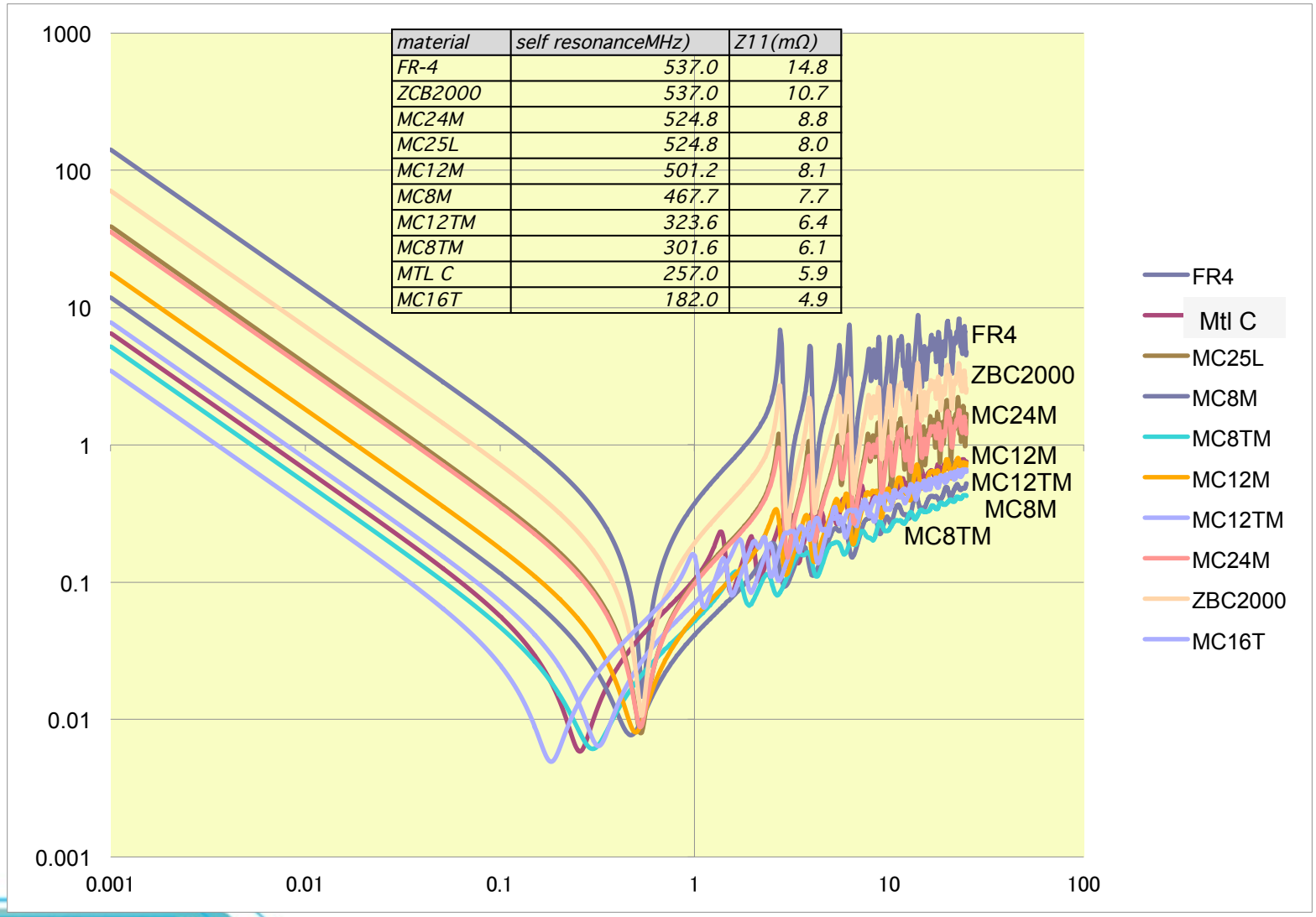
PCB Electrical Performance

Studies Up to 25 GHz

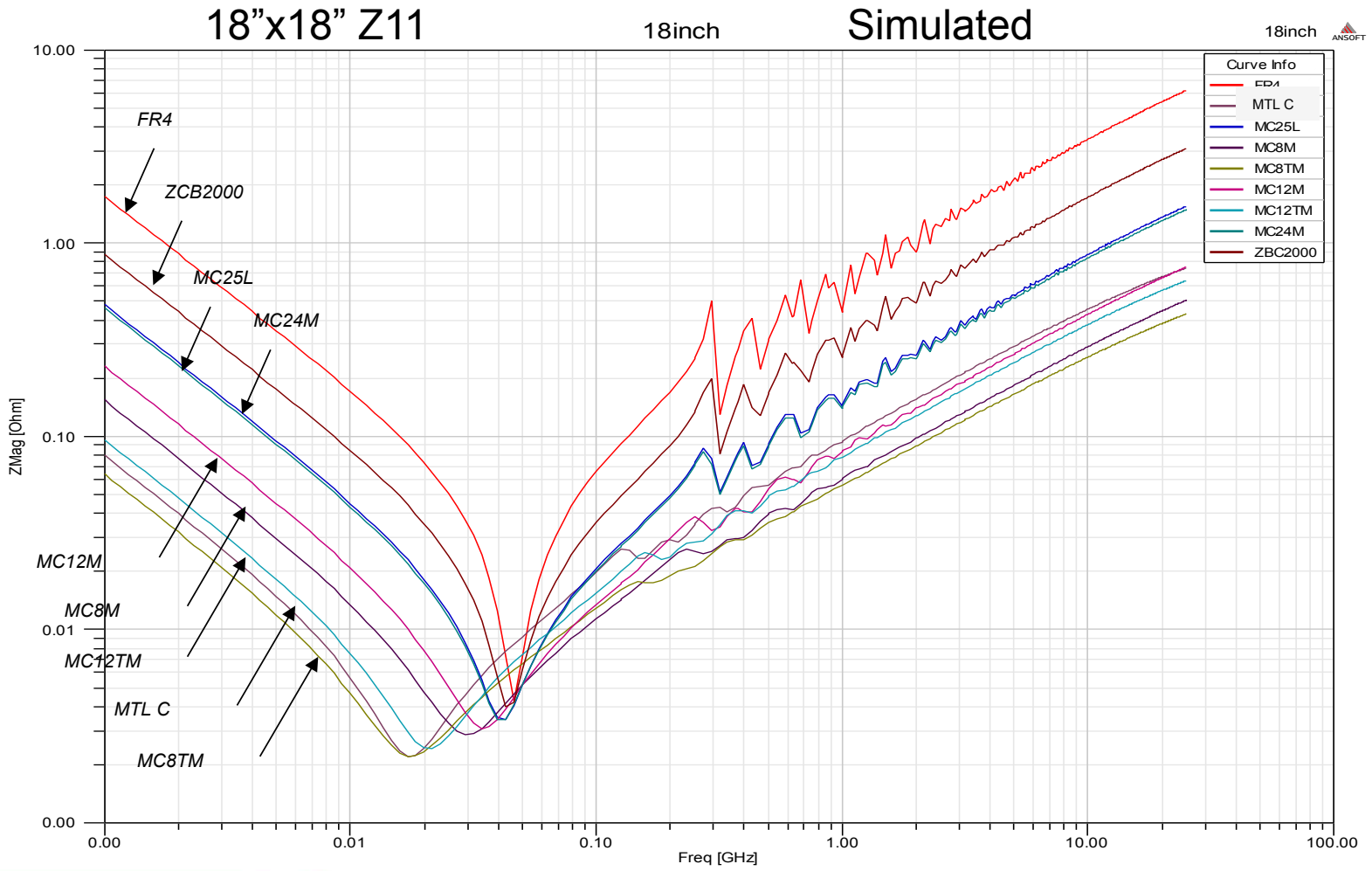
PCB Electrical Performance (Data up to 25 GHz)

2”x2” PCB Simulation

material	self resonanceMHz)	Z11(mΩ)
FR-4	537.0	14.8
ZCB2000	537.0	10.7
MC24M	524.8	8.8
MC25L	524.8	8.0
MC12M	501.2	8.1
MC8M	467.7	7.7
MC12TM	323.6	6.4
MC8TM	301.6	6.1
MTL C	257.0	5.9
MC16T	182.0	4.9



PCB Electrical Performance Data Up to 25 GHz)



RELIABILITY

Reliability Tests

Description	
6x Through Hole Solder Shock	**PASS**
6x Blind Via Solder Shock	**PASS**
Dielectric Thickness per Cross Section within +/-10%	**PASS**
T-288(>20min)	**PASS**
IST Testing (500 cycles)	**PASS**
Core Level Hi-Pot Testing 100Cores(100V/sec; 500Vmax)	**PASS**
Finished Circuit Level Hi-Pot 50 circuits (100V/sec; 500Vmax)	**PASS**

Courtesy of Sanmina-SCI

PCB FABRICATION/ PROCESSING

Processing guideline

Pre-clean
- Standard process

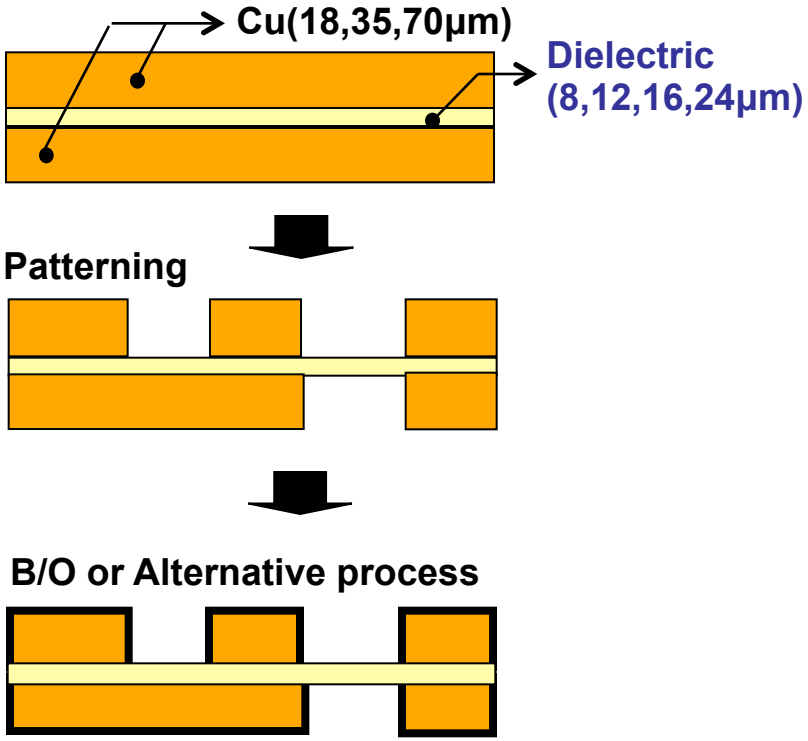
Dry Film lamination
- Standard process

Expose Image
- Standard process

Important

Pattern etching
- Thin core compatible line recommended
  Ex) Thin core Schmid etching line
- Use leader board if not confident
- Careful Handling required

Black oxidizing or alternative oxides
- Thin core compatible line recommended
- Use leader board if not confident
- Horizontal line preferred
- Careful Handling required



Power/Ground Plane Simulation

- Utilize EMI Stream
  - Developed by NEC
  - Based on SPICE Model
- Input PCB Layout in Design Format (.dsn file)
  - Output provide by standard design tools (Mentor Graphics, Cadence, etc.)
- Select thickness, Dk and Cu thickness of P/G planes
- Select frequency range
- Can add/subtract discrete SMT capacitors

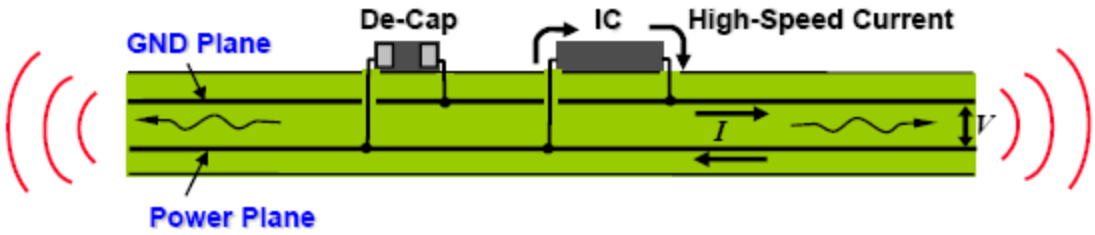
POWER DISTRIBUTIONS NETWORK SIMULATIONS

RESONANCE/ NOISE/ EMI

Why FaradFlex can reduce EMI?

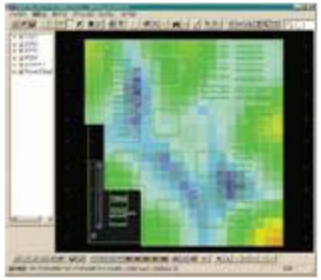
1. Can minimize loop area $(E_r = 1.316 \times 10^{-14} \times I \times f^2 \times S / r)$
2. Can minimize power bus noise
3. Can minimize resonance
4. Can minimize propagation to the edge
   (Related to Transfer Impedance (S21))

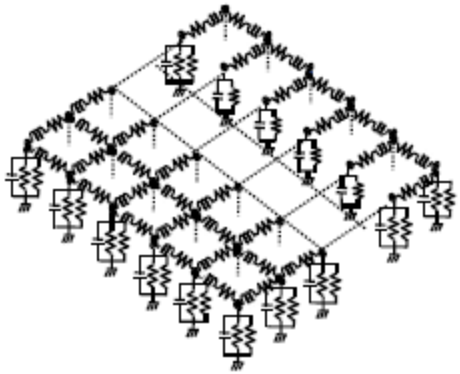
E : Electric Field Strength
I : Normal Mode Current
f : Frequency
S : Loop Area
r : Distance



PI Simulation (EMIStream/PIStream)

- Utilize EMIStream/PIStream
  - Developed by NEC
  - Based on PEEC method with Spice Simulation
- Input PCB Layout in Design File (xxx.dsn)
  - Output provide by standard PCB layout tools (Mentor Graphics, Cadence, Zuken, etc.)
- Select thickness, Dk and Cu thickness of P/G planes
- Select frequency range
- Can add/remove discrete decoupling capacitors

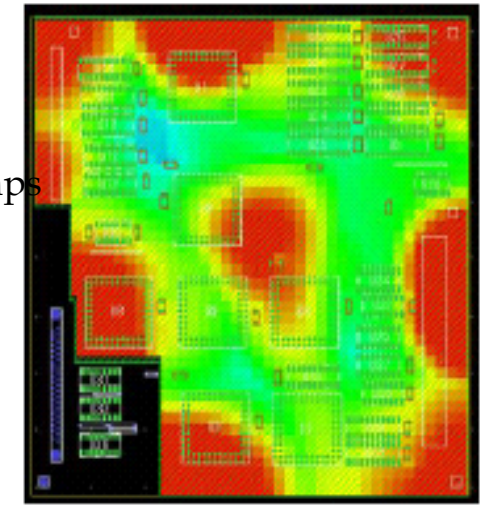




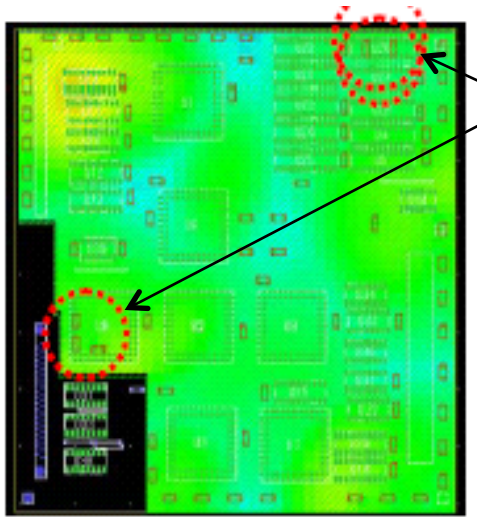
Partial Element Equivalent Circuit Model for Power/GND Plane Pair

Resonance Distribution

35- 0.1 μ F caps
for power
supply



0dB

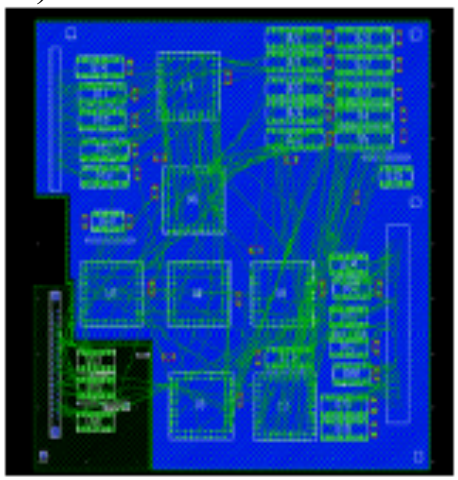


Can not place caps!

35- 0.1 μ F caps
for power supply
+44-0.1 μ F caps
for resonances

0.4mm (16 mil P/G)

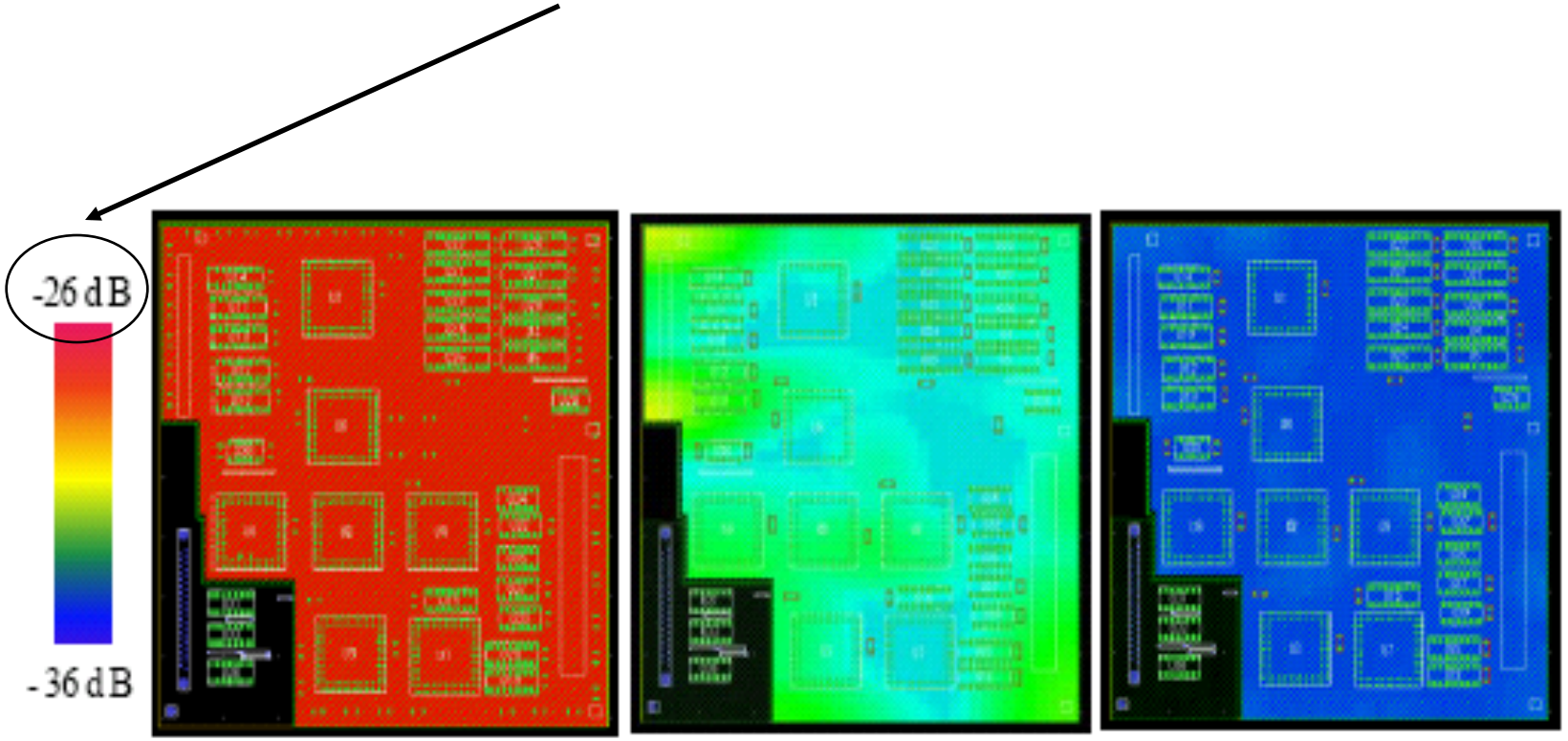
24 μ m P/G
Dk 4.4
No additional
caps



0dB

Simulations provided by
TechDream, Inc.

Resonance Distribution- Lower Noise Threshold

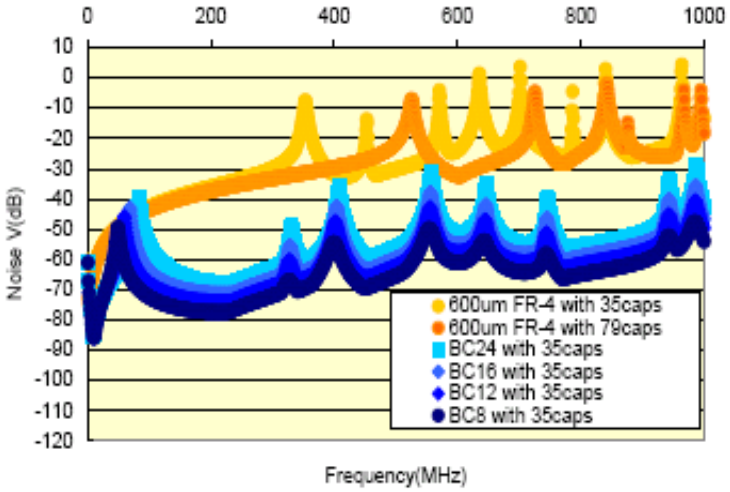


400 μm (16 mil P/G)
79 caps

24 μm P/G
Dk 4.4
35 caps

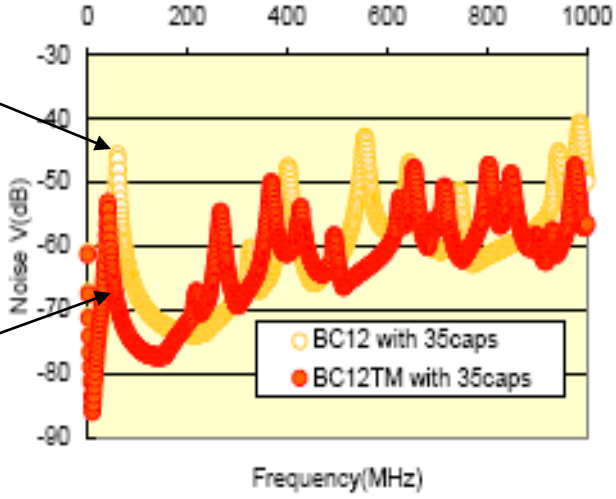
12 μm P/G
Dk 10
35 caps

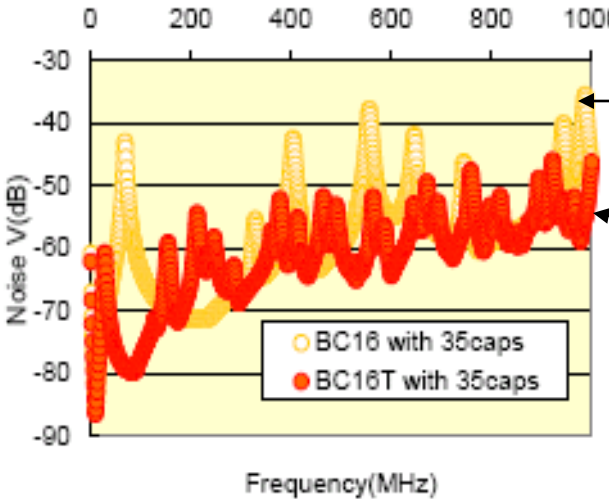
Frequency Response- Effect of Thickness, Dk



Dk-4.4

Dk-10



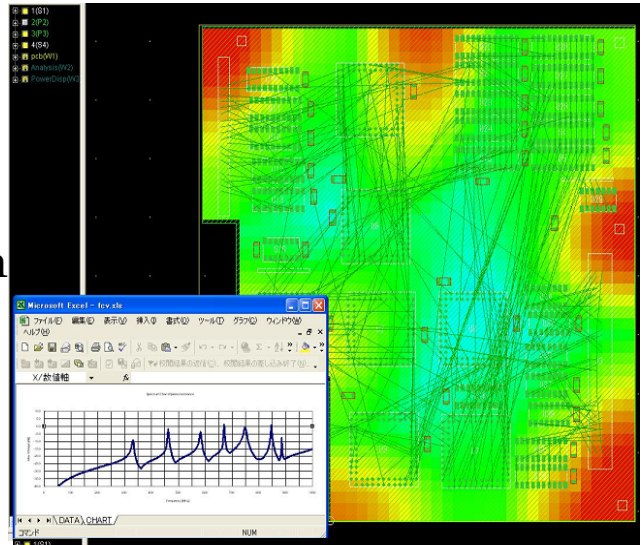


Dk-4.4

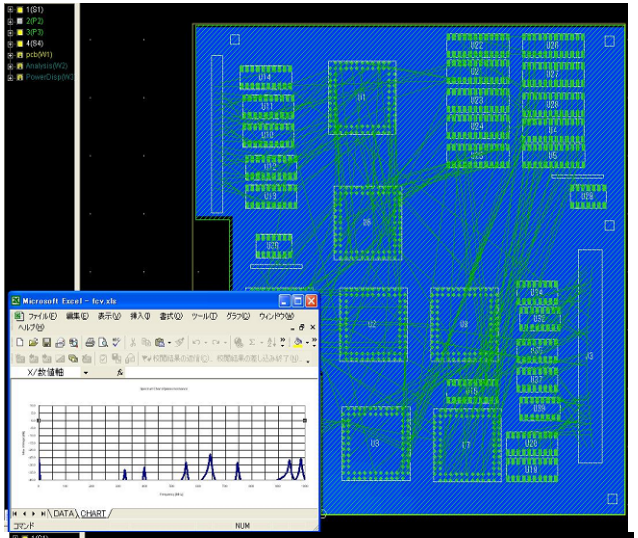
Dk-30

Test Board- Simulation #2

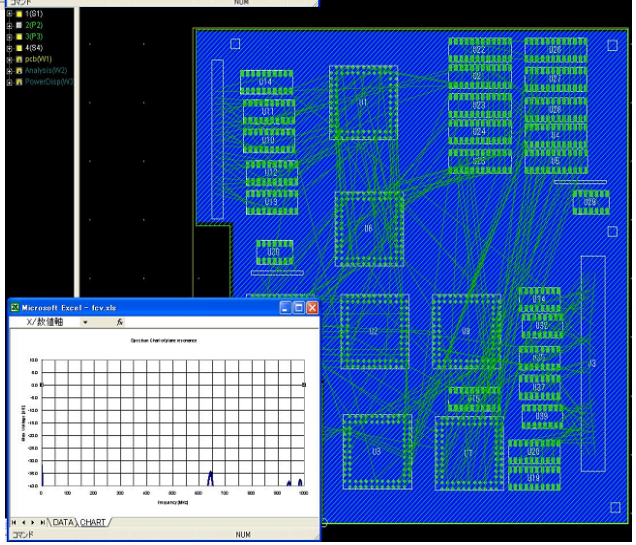
P/G Plane
FR-4 400um
With Caps



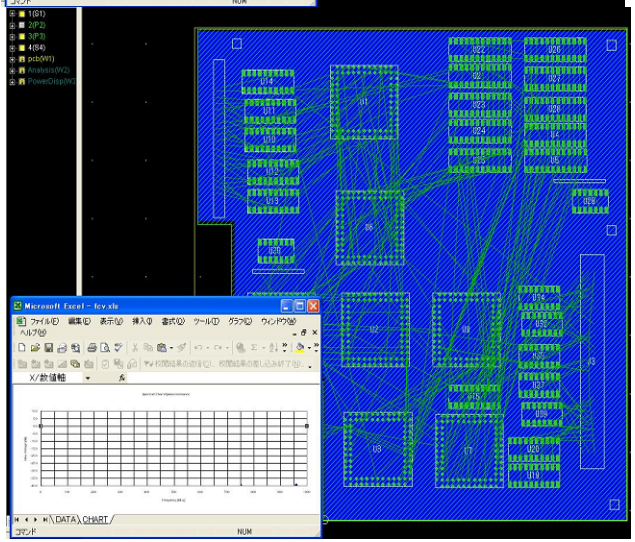
P/G Plane
BC24



P/G Plane
BC12



P/G Plane
BC16T



ELECTRICAL BENEFITS

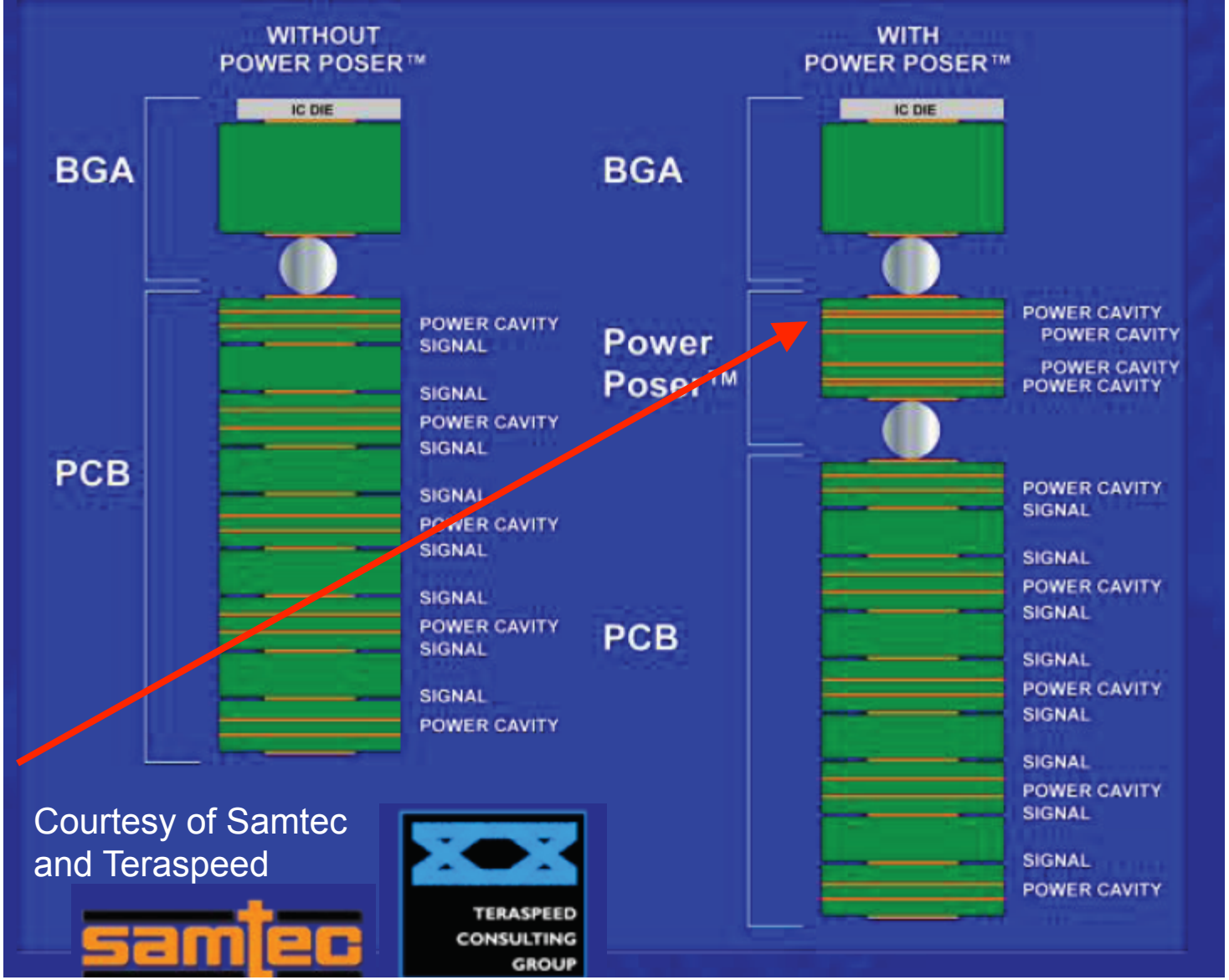
Reduced Jitter/ Improved “Eye”

Using FaradFlex

BC24

BC12TM

or BC8TM



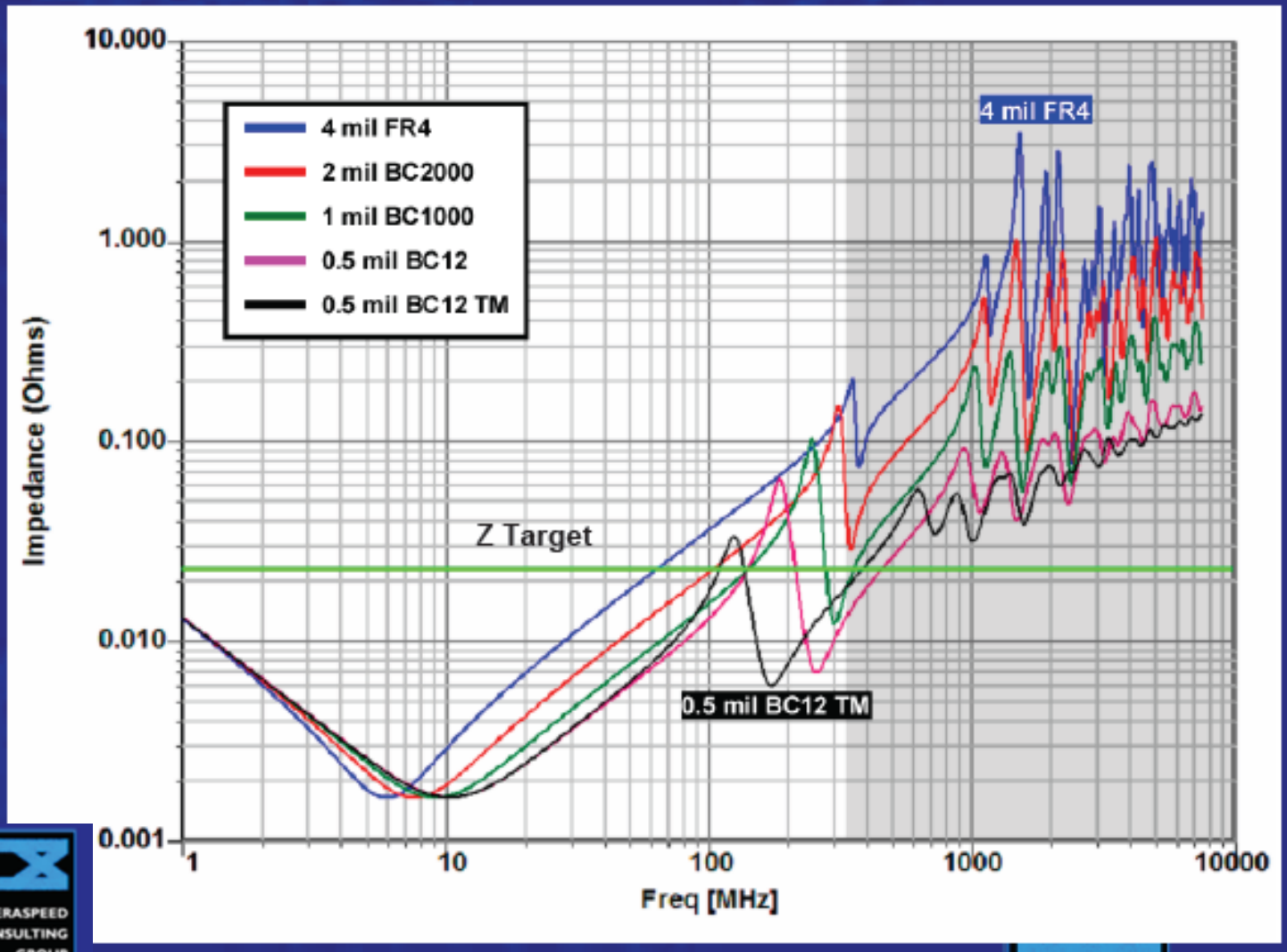
0402 Capacitors with 4 mil Deep Planes Various Plane Thicknesses on 6" x 6" PCB

Reduction in dielectric thickness decrease impedance, but also lowers resonance frequency.

Reduction in dielectric thickness increases magnitude of peaks.

Increase in material Er lowers resonance frequency.

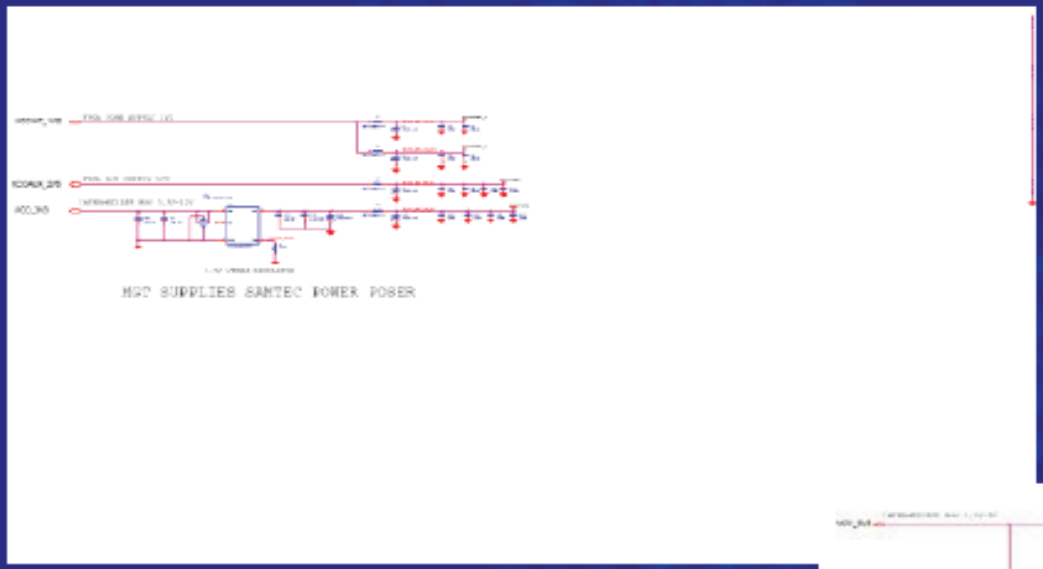
Courtesy of Samtec and Teraspeed



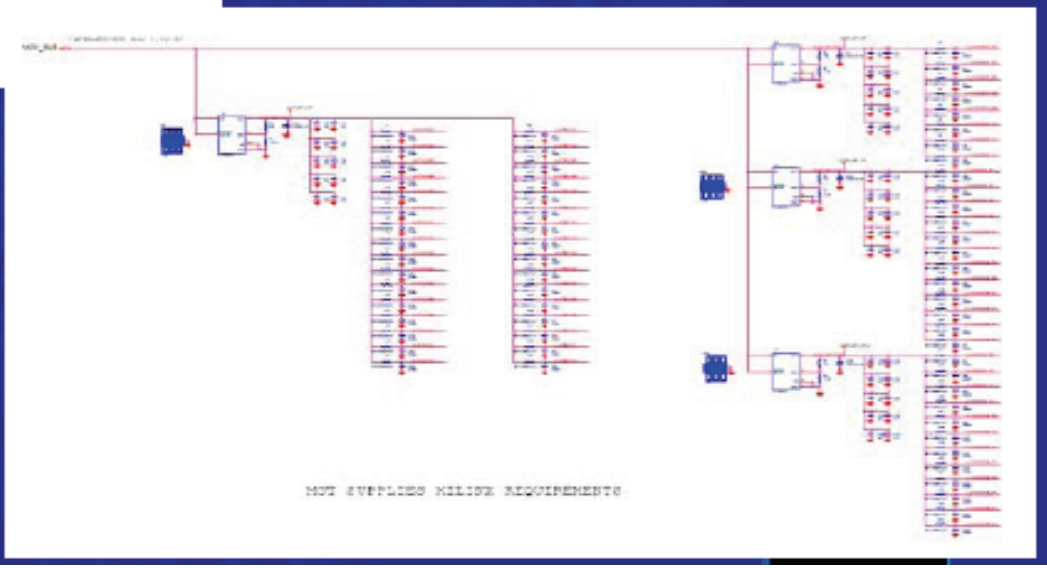
samtec

TERASPEED CONSULTING GROUP

SerDes Filtering Comparison



PowerPoser™ SerDes Filtering



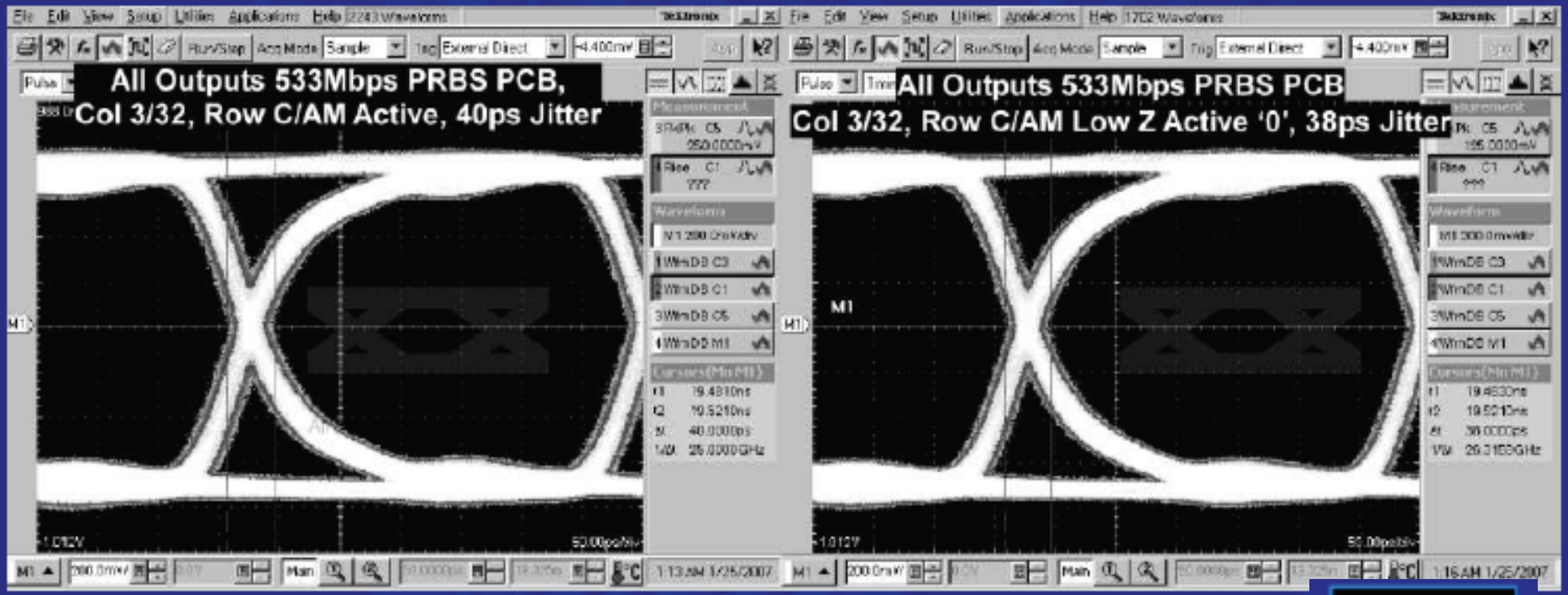
Xilinx SerDes Filtering

Courtesy of Samtec and Teraspeed

samtec

TERASPEED CONSULTING GROUP

Xilinx Guidelines Board SerDes Best Performance @ 3.125 Gbps

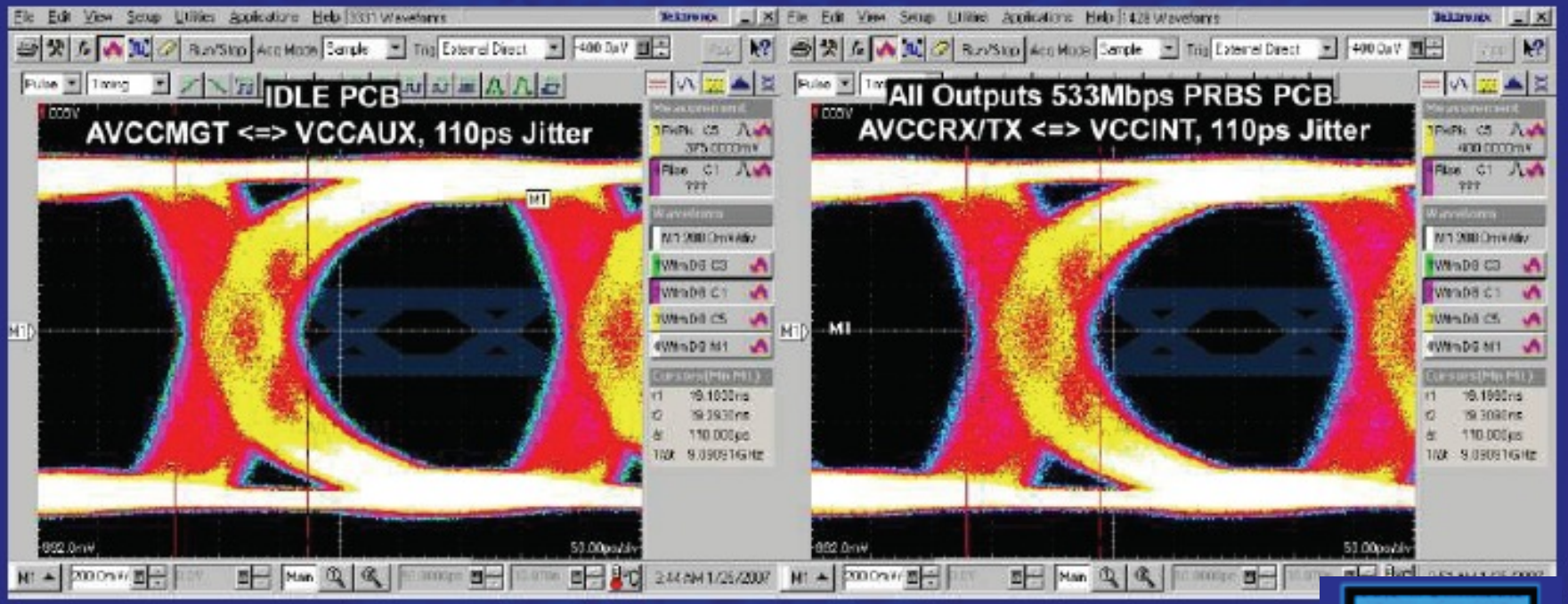


Courtesy of samtec

Design uses all Xilinx mandated linear power supplies and ferrite filter networks for MGT SerDes.

TERASPEED CONSULTING GROUP

Xilinx Filter Network with SMPS Performance @ 3.125 Gbps



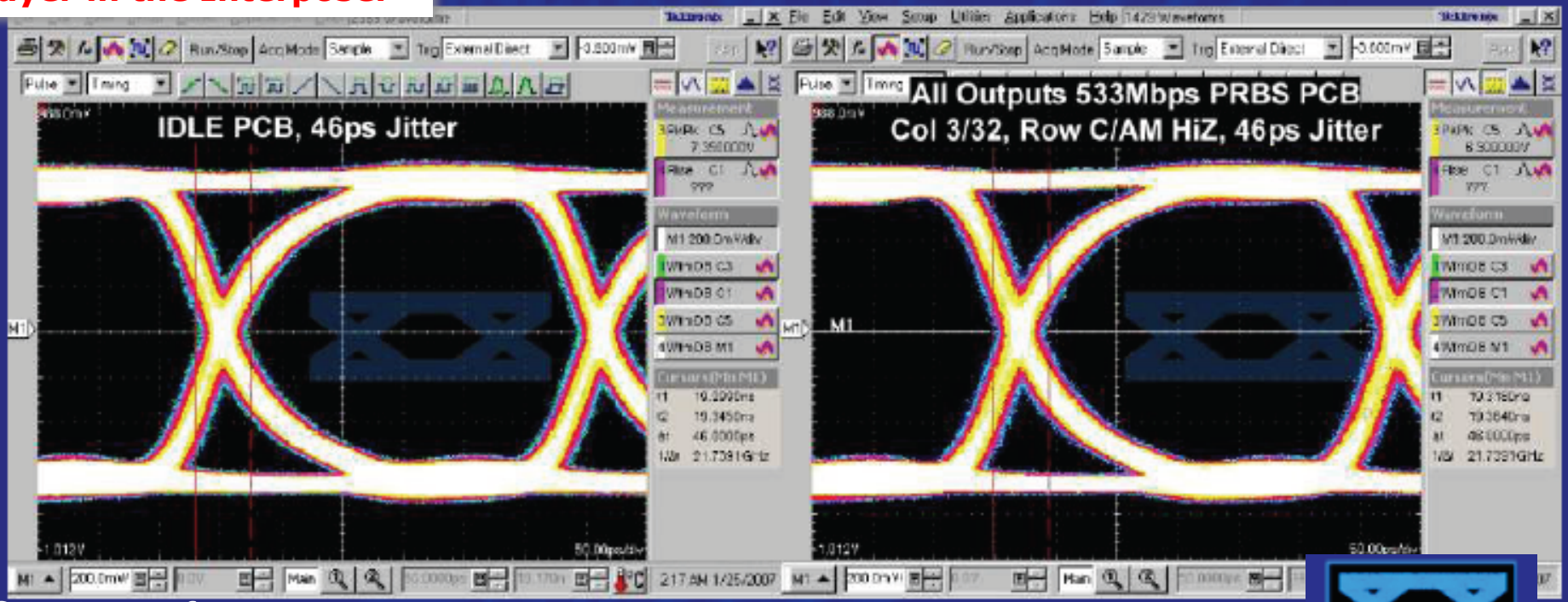
Courtesy of samtec

TERASPEED CONSULTING GROUP

Without Power Poser

PowerPoser™ DirectDrop™ Eval Board Measurements SerDes

Using FaradFlex BC12TM as the key layer in the Interposer

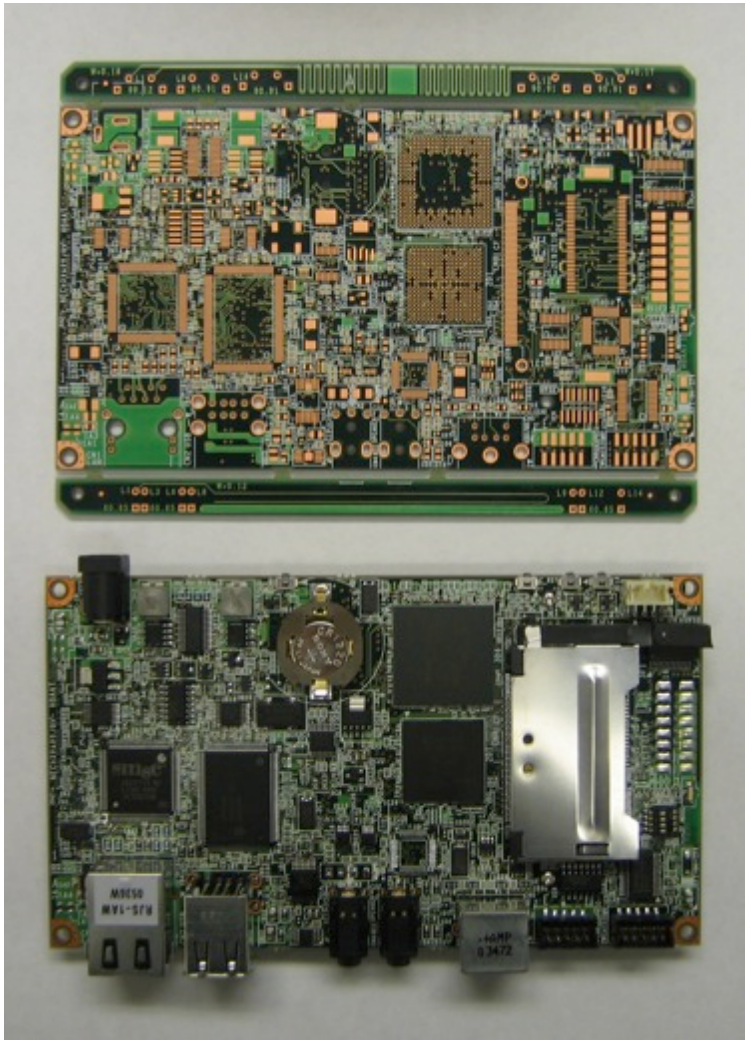


Courtesy of samtec

TERASPEED CONSULTING GROUP

With Power Poser on Xilinx Worst Performance Layout

NEC CASE STUDY



(by courtesy of NEC System Technology, Inc.
& NEC Information Technology, Inc.)

PCB

Construction of Reference Board

No.	Layer		Thickness[mm]	
		resist		
1	Signal		0.057	Include Plating
		prepreg	0.11	
2	Gnd(Plane)		0.032	
		core	0.15	
3	Signal		0.032	
		prepreg	0.17	
4	Gnd(Plane)		0.032	
		prepreg	0.14	
5	Vdd(Plane)		0.032	
		core	0.15	
6	Signal		0.032	
		prepreg	0.14	
7	Gnd(Plane)		0.032	
		core	0.15	
8	Signal		0.032	
		prepreg	0.14	
9	Signal		0.032	
		core	0.15	
10	Vdd(Plane)		0.032	
		prepreg	0.14	
11	Gnd(Plane)		0.032	
		prepreg	0.17	
12	Signal		0.032	
		core	0.15	
13	Gnd(Plane)		0.032	
		prepreg	0.11	
14	Signal		0.057	Include Plating
		resist		

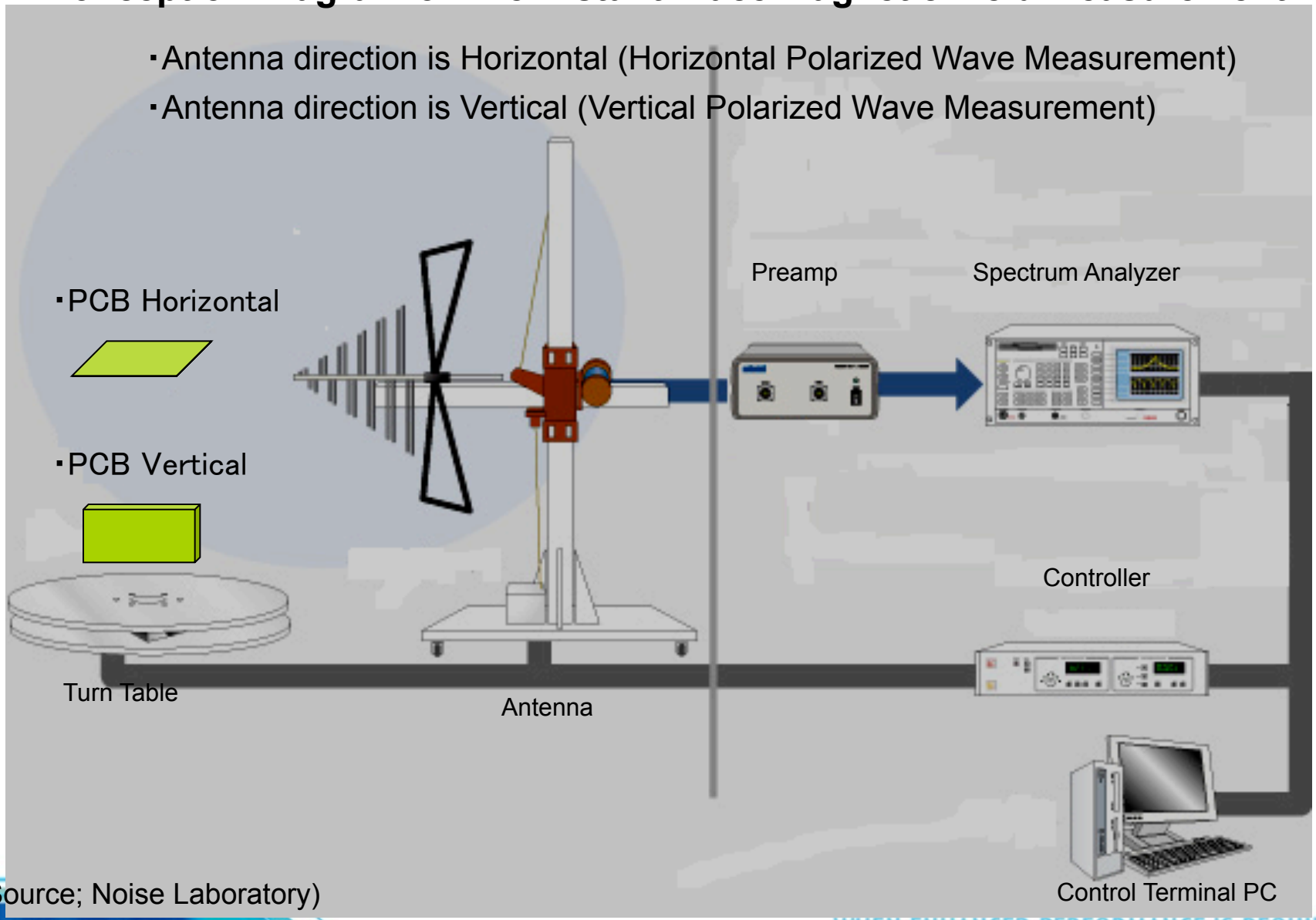
BC24,12,12TM

BC24,12,12TM

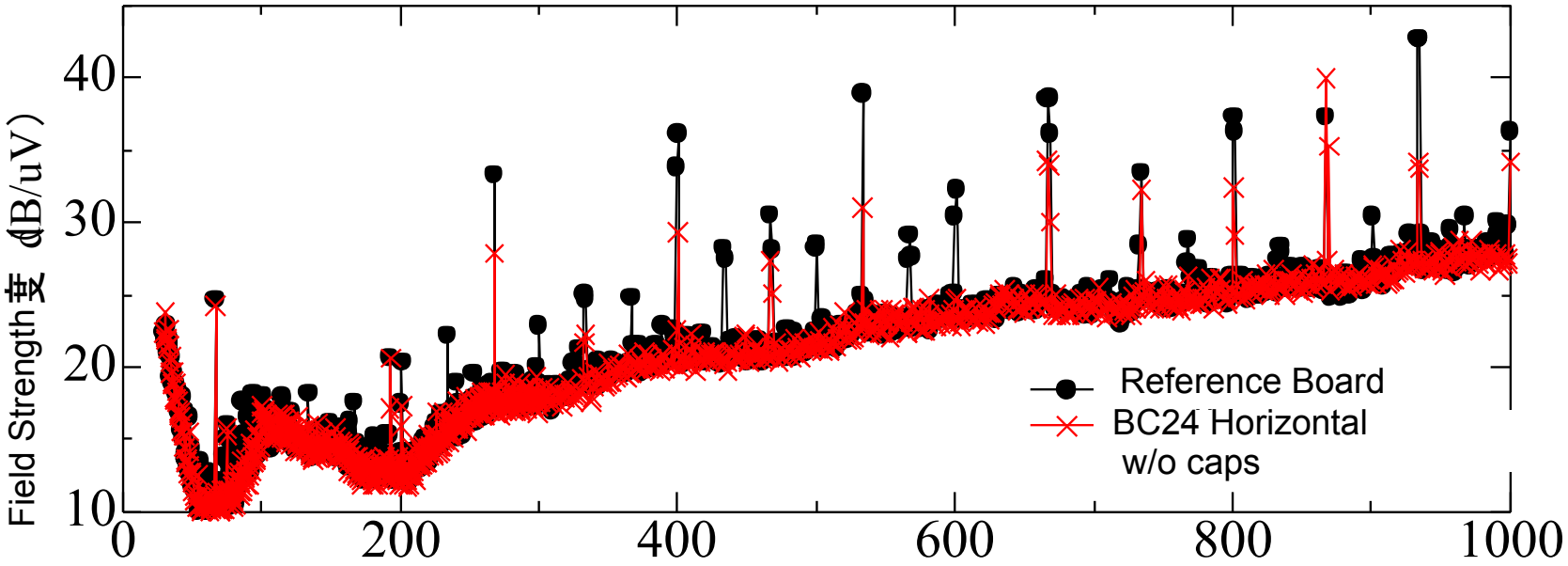
Total 2.368 ±0.2mm

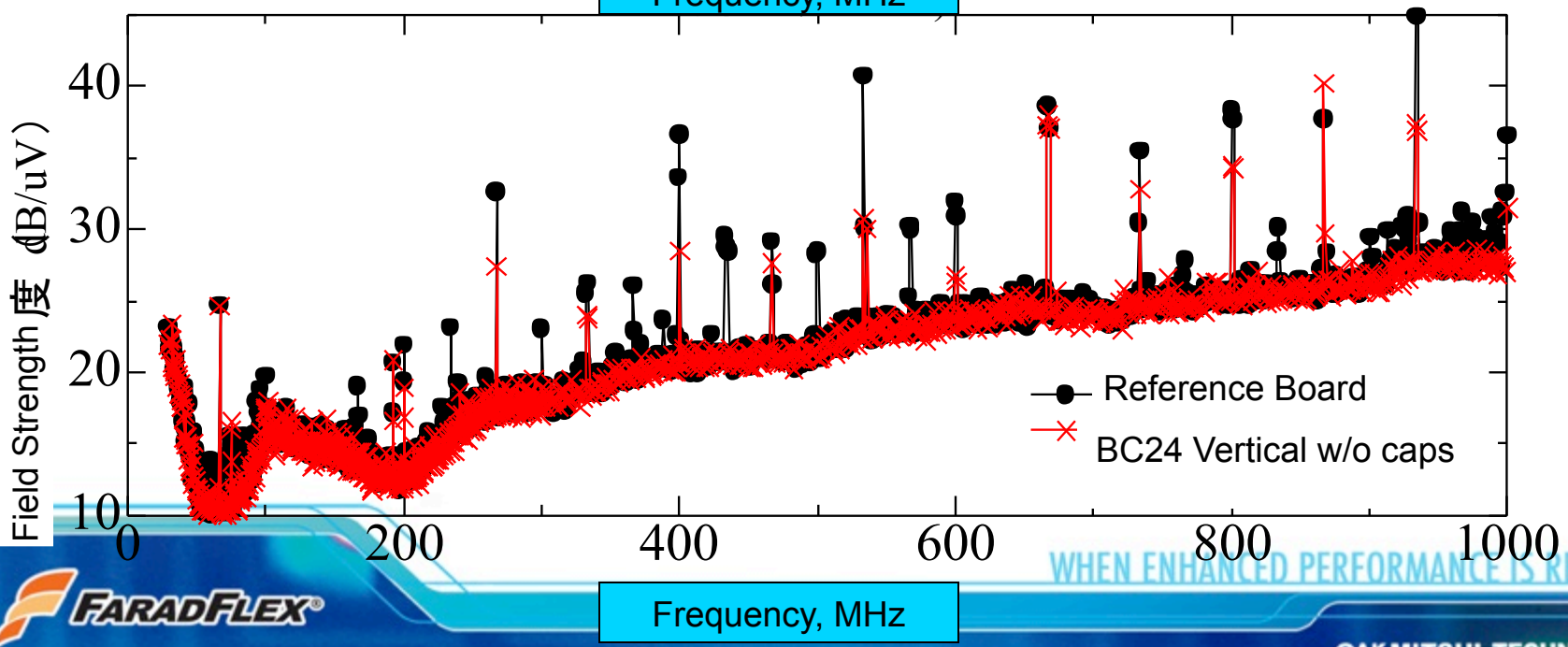
A Conception Diagram of The Distant Place Magnetic Field Measurement

- Antenna direction is Horizontal (Horizontal Polarized Wave Measurement)
- Antenna direction is Vertical (Vertical Polarized Wave Measurement)

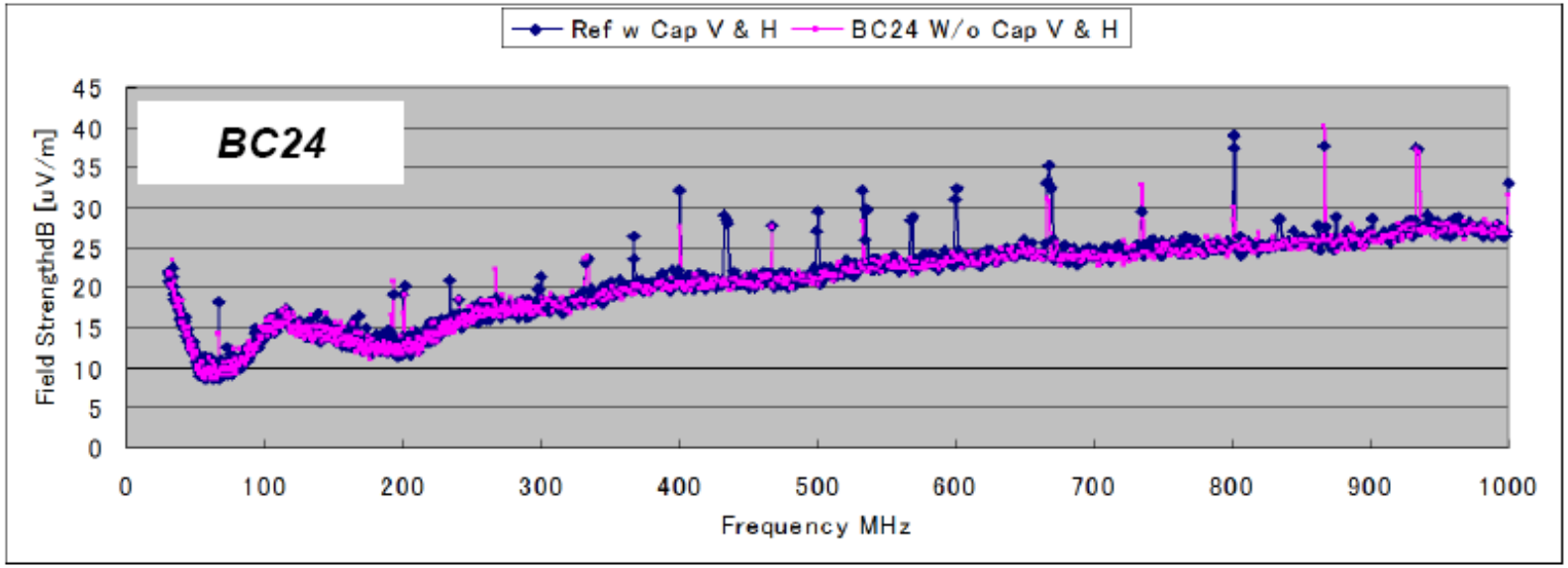


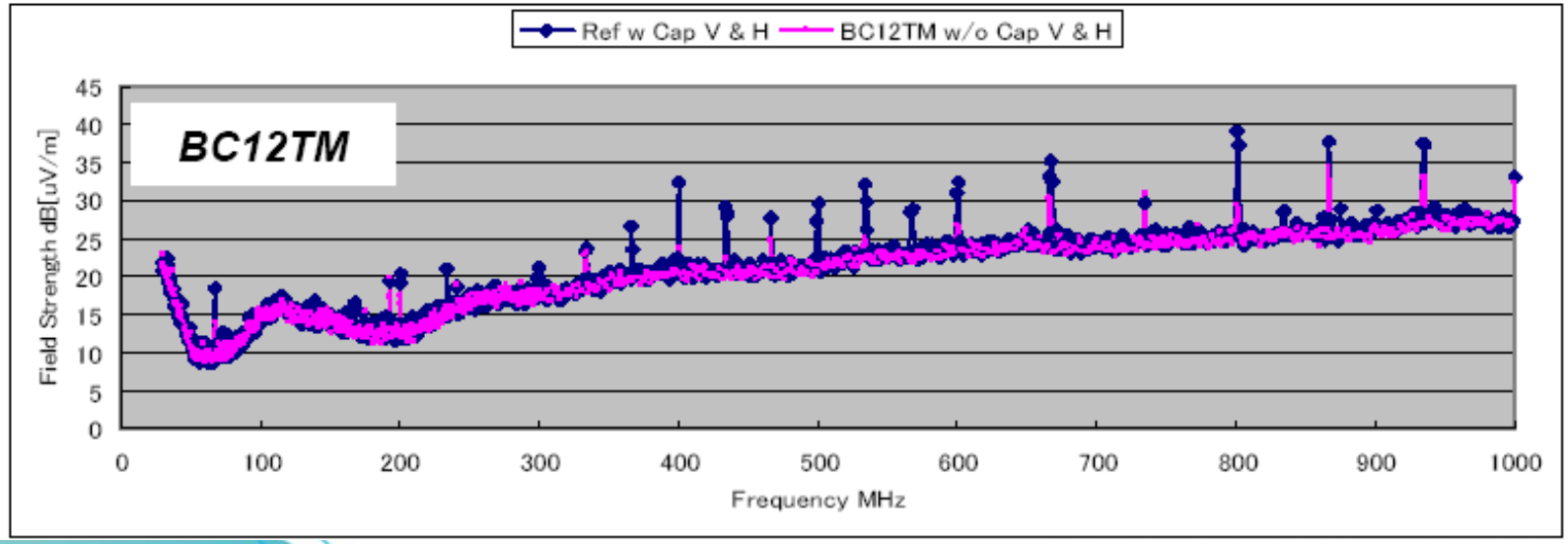
(Source; Noise Laboratory)


Field Strength (dB/uV)
40
30
20
10
0
200
400
600
800
1000
Reference Board
BC24 Horizontal
w/o caps
Frequency, MHz


Field Strength (dB/uV)
40
30
20
10
0
200
400
600
800
1000
Reference Board
BC24 Vertical w/o caps
Frequency, MHz

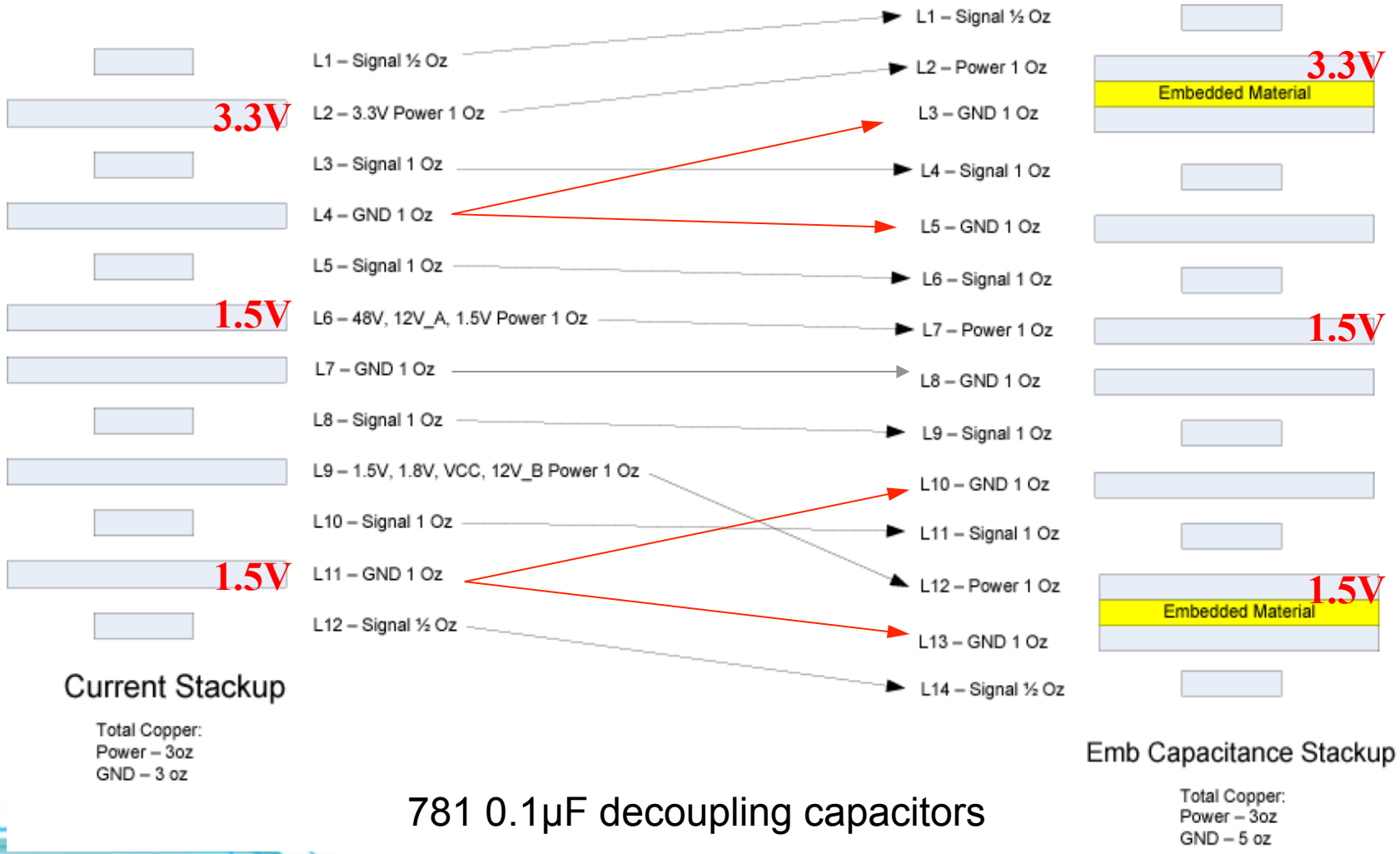
Comparison between reference board with Caps and BC without Caps





NCR-TERADATA CASE STUDY

NCR-TERADATA Study



781 0.1µF decoupling capacitors

Capacitance Measurements

(courtesy of Univ. of Missouri at Rolla)

Plane Pair	FR-4 (nF)	BC24 (nF)	BC12 (nF)	BC12TM (nF)
1.5V/GND	76.1 (75.8)	179.5 (179.0)	286.7 (266)	487 (478)
3.3V/GND	21.2 (21.2)	323.8 (321.3)	551 (541)	1148 (1082)

From LCR Meter

Extracted from VNA

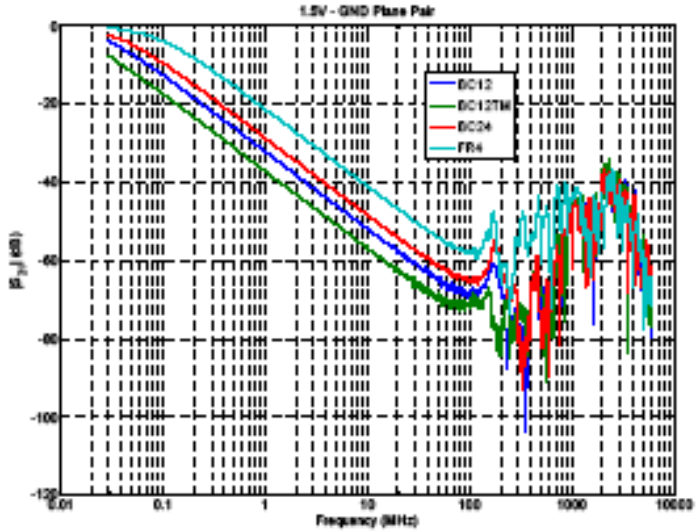
Note: 1.5V plane is split resulting in smaller capacitor area

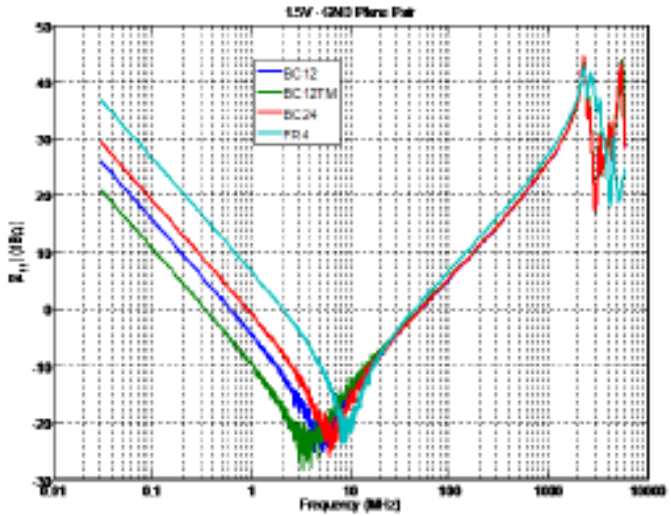
Replaces **78.1 µF** of capacitance on standard board
(781 capacitors of 0.1 µF)

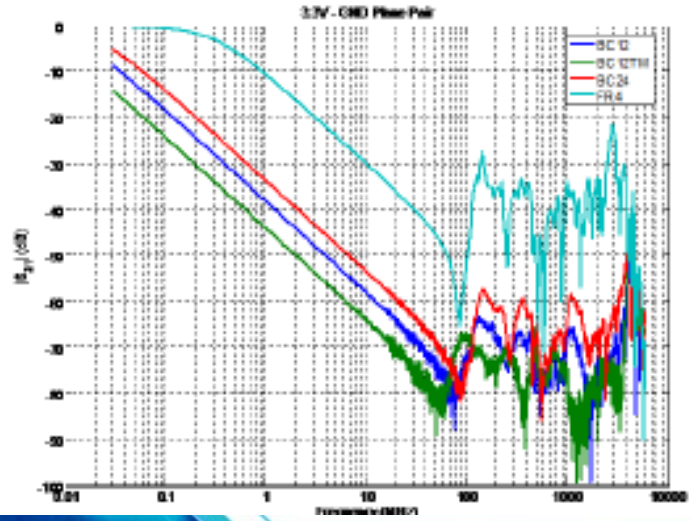
Board Impedance Measurements (S21, Z11)

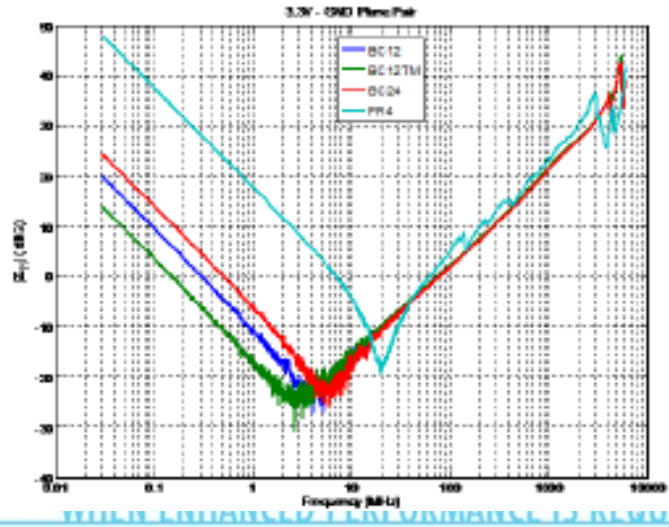
Measurement Equipment : Agilent 8753D (Vector Network Analyzer)

Probe Point : Decoupling Capacitor Pad







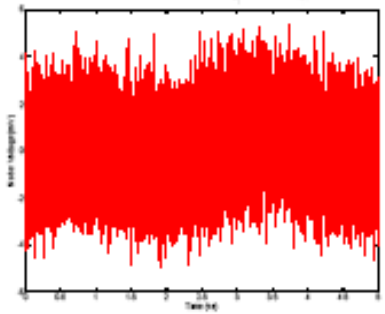


Time Domain Power Bus Noise Measurement

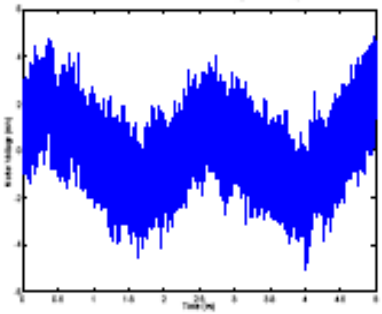
Measurement Equipment : Agilent Infiniium 54855A (Digital Sampling Oscilloscope)

Probe Point : Decoupling Capacitor Pad

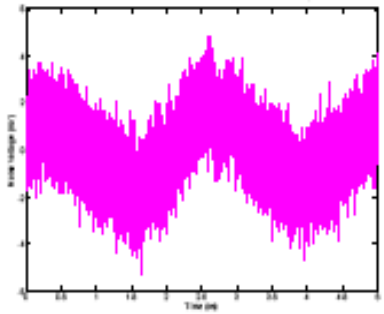
1.5V/GND (FR-4)



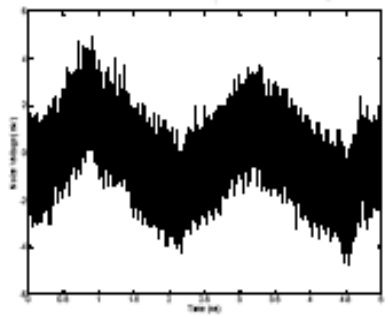
1.5V/GND (B24)



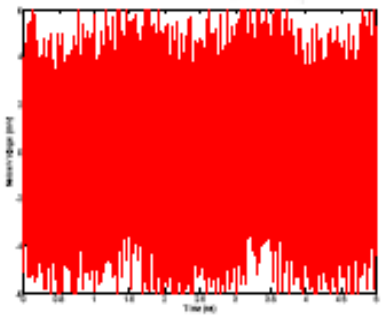
1.5V/GND (BC12)



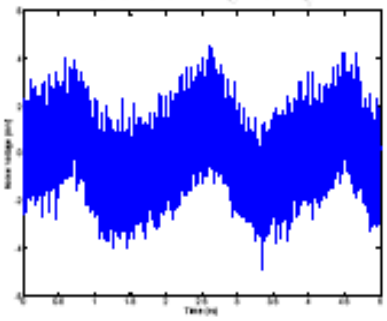
1.5V/GND (BC12TM)



3.3V/GND (FR-4)



3.3V/GND (BC24)



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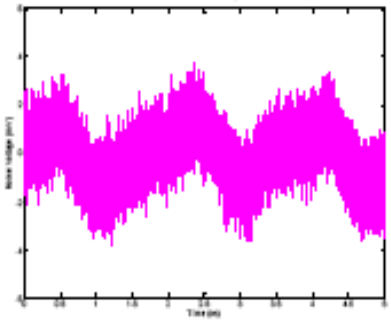
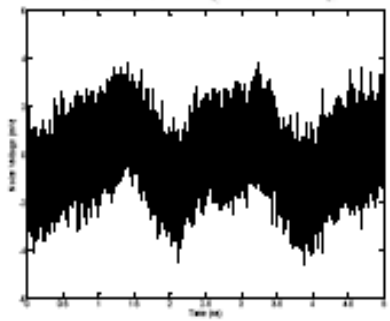


3.3V/GND (BC12TM)



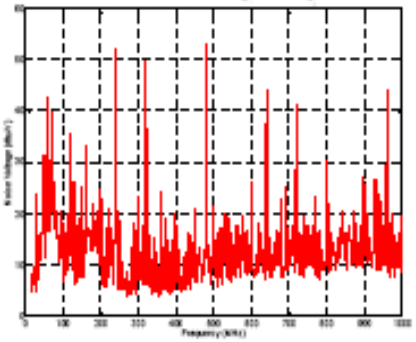
Frequency Domain Power Bus Noise Measurement

Measurement Equipment : Agilent E7404A (Spectrum Analyzer)

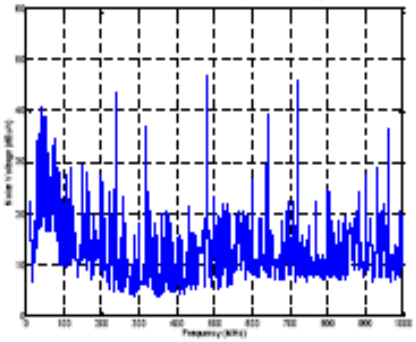
Probe Point : Decoupling Capacitor Pad

Tested to 1 GHz

1.5V/GND (FR-4)



1.5V/GND (BC24)



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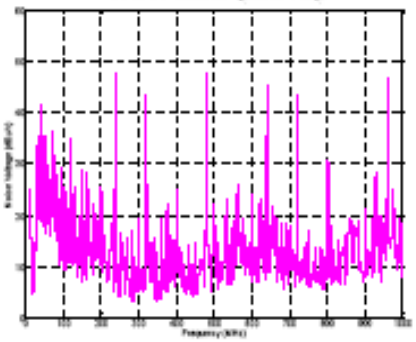
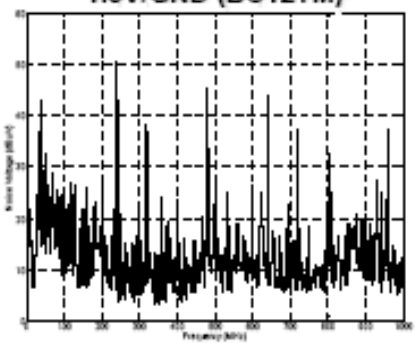
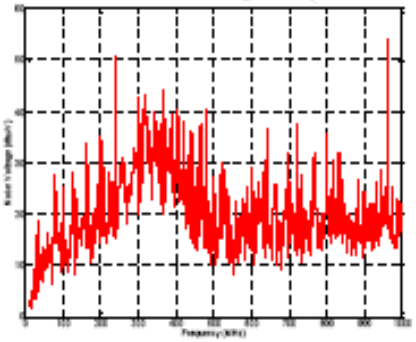


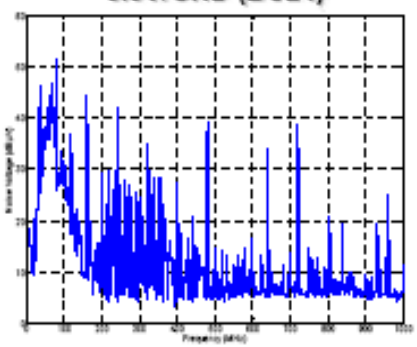
1.5V/GND (BC12TM)



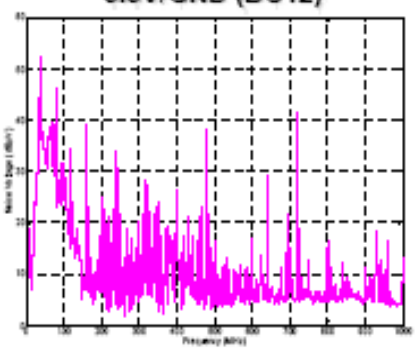
3.3V/GND (FR-4)



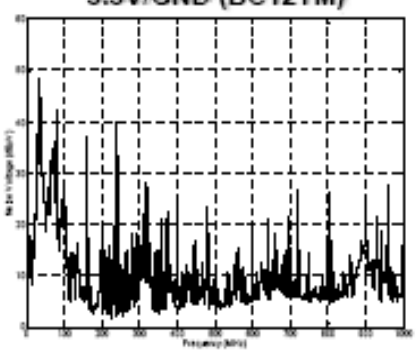
3.3V/GND (BC24)



3.3V/GND (BC12)



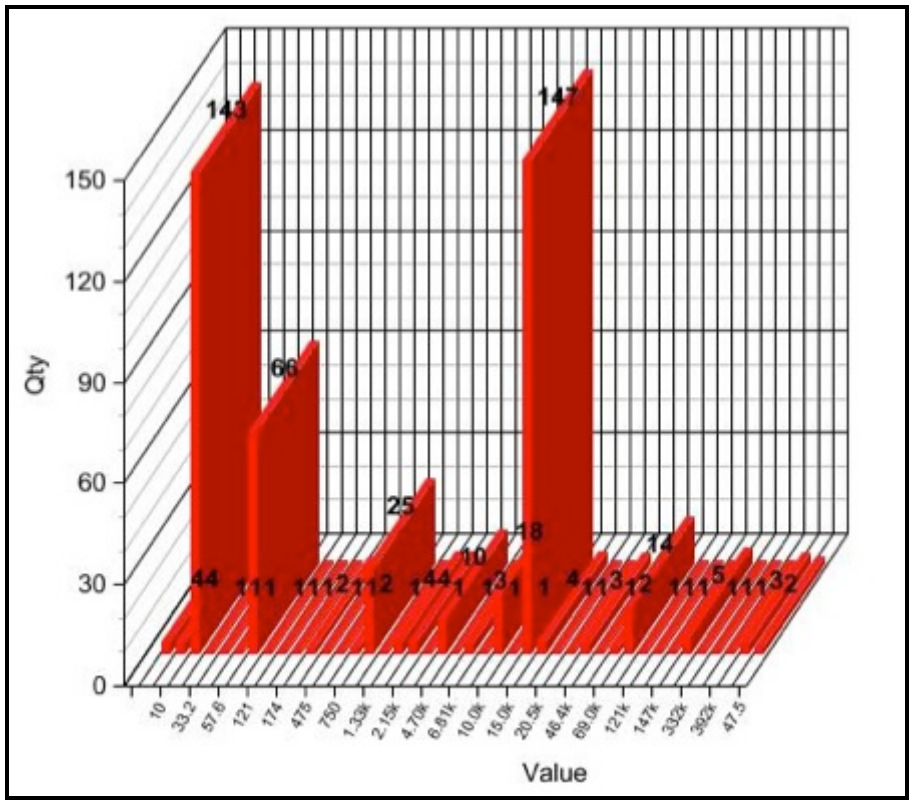
3.3V/GND (BC12TM)

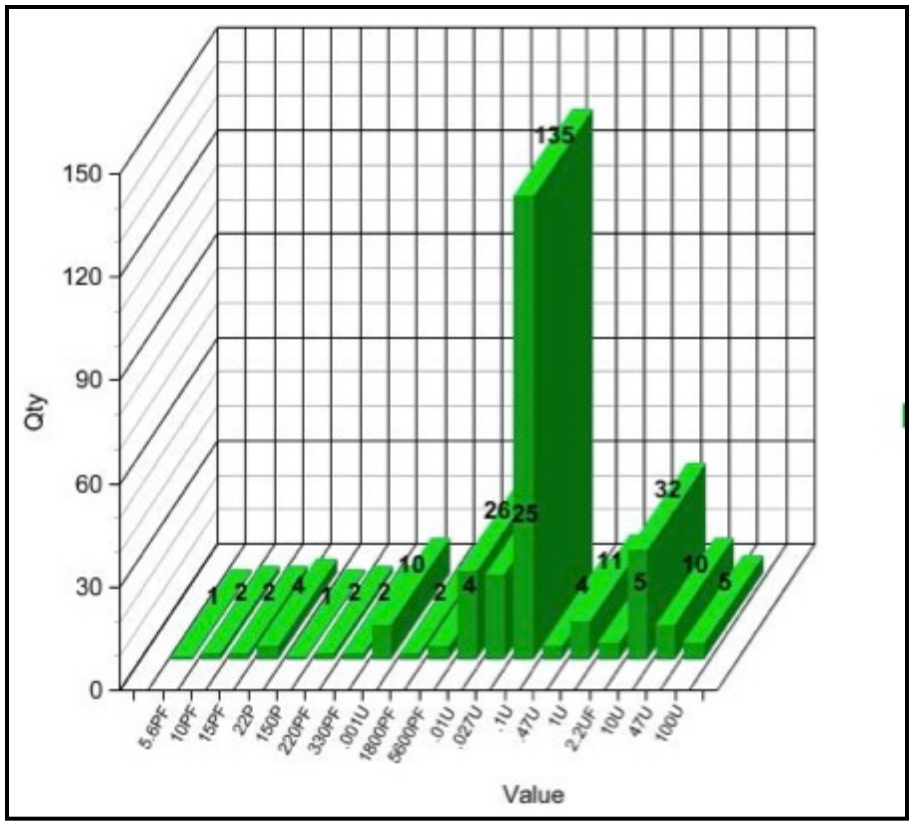


HARRIS CASE STUDY

The Embedded Passives Journey

IPC/APEX – April 2, 2008
Authors:
Bill Devenish – Harris Corp., Mechanical Advanced Development (MAD)
Andrew Palczewski – Harris Corp., PCB Technologist



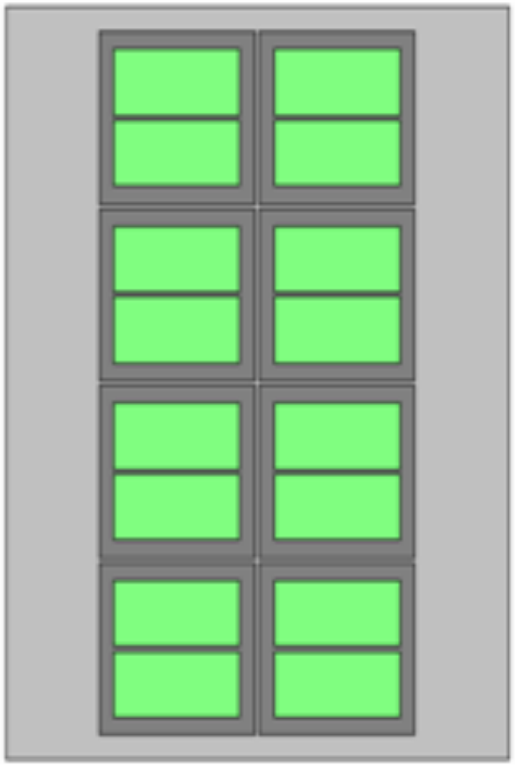


Used with the permission of Harris Corporation

COST SAVINGS		$37.88
-Part Cost		
	CAPACITORS	$1.19
	RESISTORS	$9.77
-Cost of Quality		
	Component	Body
	CAPACITORS	$4.04
		0603
		0402
	RESISTORS	$11.06
		0201
		0402
-Assembly Cost		$11.82
	Total Parts	591

Used with the permission of Harris Corporation

Original Panelization - 16 Up



Size:
Panel: 18.0 x 24.0
Array: 5.6 x 5.524
Part: 4.54 x 2.15

Panel Yield:
8 Arrays of 2 Parts
16 Parts Total
57.3% Material Utilization

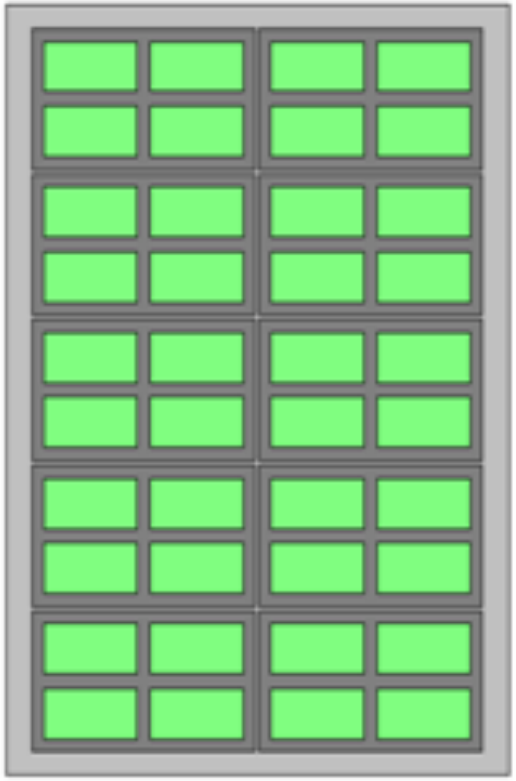
Matrix:
On Panel: 2 x 4, Origin: X3.35 Y0.802
On Array: 1 x 2

Spacing:
On Panel: 0.1 x 0.1
On Array: 0.1 x 0.1

Panel Borders:
Left: 3.35 Right: 3.35
Top: 0.802 Bottom: 0.802

Array Borders:
Left: 0.53 Right: 0.53
Top: 0.562 Bottom: 0.562

Revised Panelization - 40 Up



0N6B9749-B redux 25%

Size:
Panel: 18.0 x 24.0
Array: 8.0 x 4.42
Part: 3.4 x 1.61

Panel Yield:
10 Arrays of 4 Parts
40 Parts Total
81.9% Material Utilization

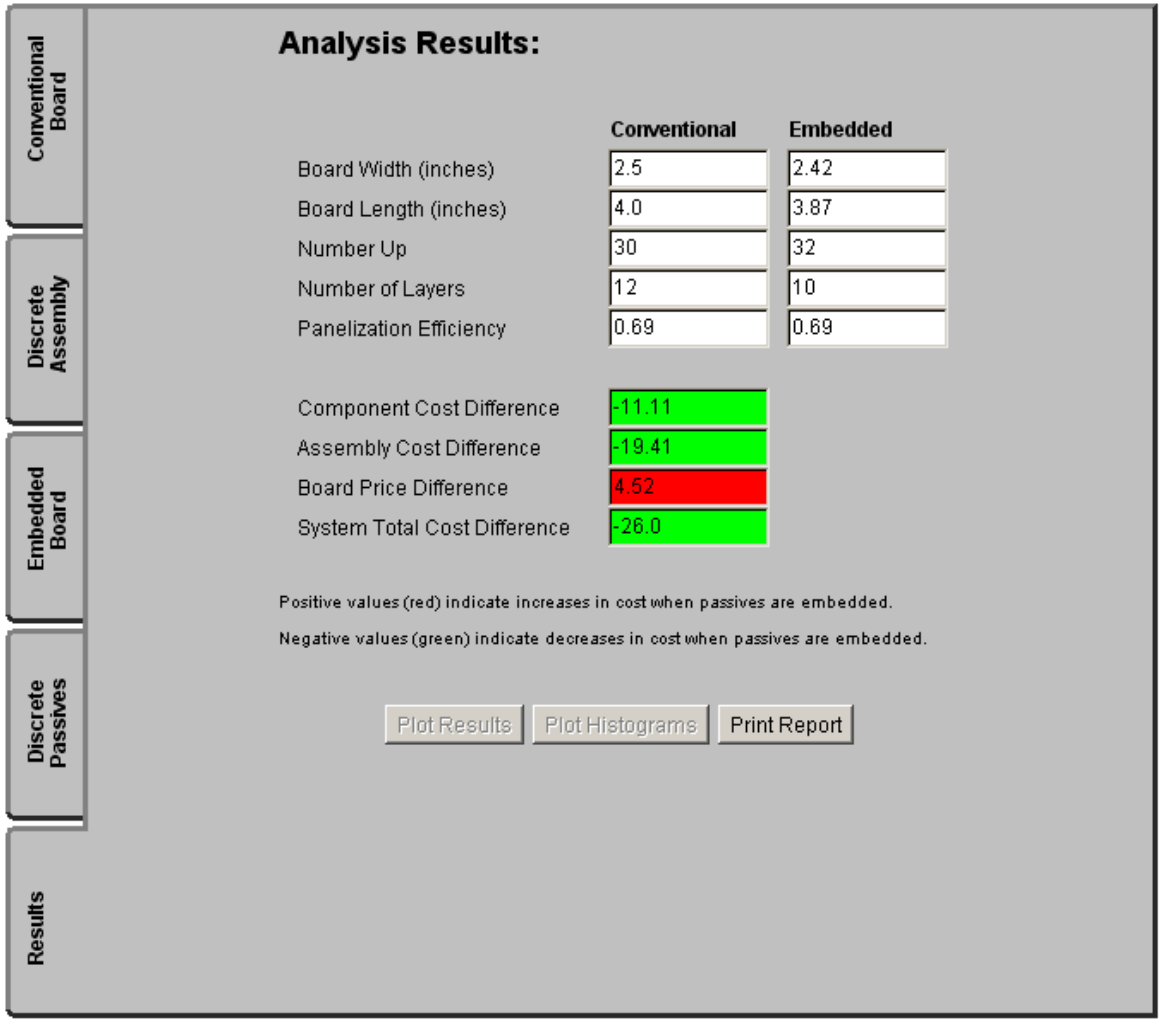
Matrix:
On Panel: 2 x 5, Origin: X0.95 Y0.75
On Array: 2 x 2

Spacing:
On Panel: 0.1 x 0.1
On Array: 0.4 x 0.4

Panel Borders:
Left: 0.95 Right: 0.95
Top: 0.75 Bottom: 0.75

Array Borders:
Left: 0.4 Right: 0.4
Top: 0.4 Bottom: 0.4

Used with the permission of Harris Corporation



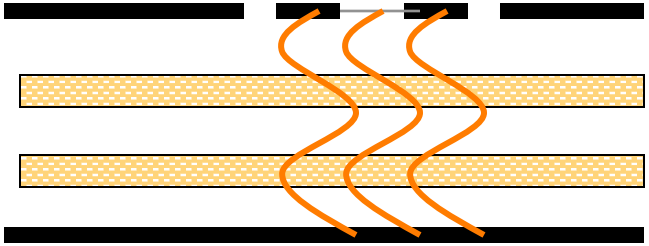
Courtesy of Harris Corp. and CALCE

Other Benefits Of FaradFlex

Performance: Thermal Stability

Buried Capacitance™ Core

Standard Core



FaradFlex **1.5 to 3** times better heat transfer due to thinness

Thinner dielectric provides better heat transfer to copper

Capacitor Material vs. FR4

Properties	NiP/Capacitor Core	NiP Core FR-4 (control)	Remarks and Conditions
Sheet Resistivities (ohm/square)	25	25	Nominal
Material Tolerance	+/-5%	+/-5 %	
Load Life Cycling Test Resistor Size: 0.500" X 0.050" Loaded: (Δ R%) @ 150mW Unloaded: (Δ R%)	 <0.9 after 3200 hrs.) <0.74 after 3200 hrs.)	 <5	MIL-STD-202-108I Ambient Temp: 70C On Cycle: 1.5 hrs Off Cycle: 1.5 hrs Length Of Test: 10000 hrs
Current Noise Index in dB	<-23	<-15	MIL-STD-202-308 Voltage Applied: 5.6 Volts
Humidity Test (Δ R%)	0.5	0.5	MIL-STD-202-103A Temp: 40 °C Relative Humidity: 95% Time: 240 hrs
Characteristic (RTC) PPM/°C	-6.0	50	MIL-STD-202-304 Hot Cycle: 25°, 50°,75° 125°C Cold Cycle: 25°, 0°,-25°, -55°C
Thermal Shock (Δ R%)	0.2	-0.5	MIL-STD-202-107B No of Cycles: 25 Hot Cycle Temp: 125 °C Cold Cycle Temp: -65 °C
Solder Float (Δ R%) After 1 Cycle After 5 cycles	 -0.4 -0.6	0.5	MIL-STD-202-210D Temp: 260°C Immersion: 20 Second
Power Density (mW/mil ^{2}) derated at 50%	0.45	0.15	Step-up Power Test Resistor size 0.020" x 0.030"

3X better power density through resistor due to better heat conductivity of FaradFlex

Courtesy of Bruce Mahler of Ohmega

Synergistic Effect !

Conclusion

- Embedded Capacitor and can Improve System Price/Performance by
  - Reducing Discrete Caps
  - Reducing PWB size
  - Increasing Functionality
  - Improving power distribution
  - Improving Signal integrity
- Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency
- New Substrates have demonstrated *excellent* electrical performance and physical properties.
- They are *compatible* with PCB processing; a truly "drop in" material.
- Materials are commercially available from many Fabricators
- Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PCBs
- GREEN and Lead Free Solution

FaradFlex ADVANTAGES

- Broadest Line Up of Products
- Delivery is 1 week or less in US and Asia
- Local sales and technical support in US and Asia
- Highest Quality Material compared with Competitive materials (no foreign material)
- Best Panel Size Flexibility for PCB Designs
- Most Copper Weight Options
- Lowest Profile Copper available used ONLY on FaradFlex
- Reliability: All panels HIPOT tested by Oak-Mitsui prior to shipment.

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john.andresakis@oakmitsui.com

Additional information available at
www.oakmitsui.com