High-Speed DDR4 Memory Designs and Power Integrity Analysis

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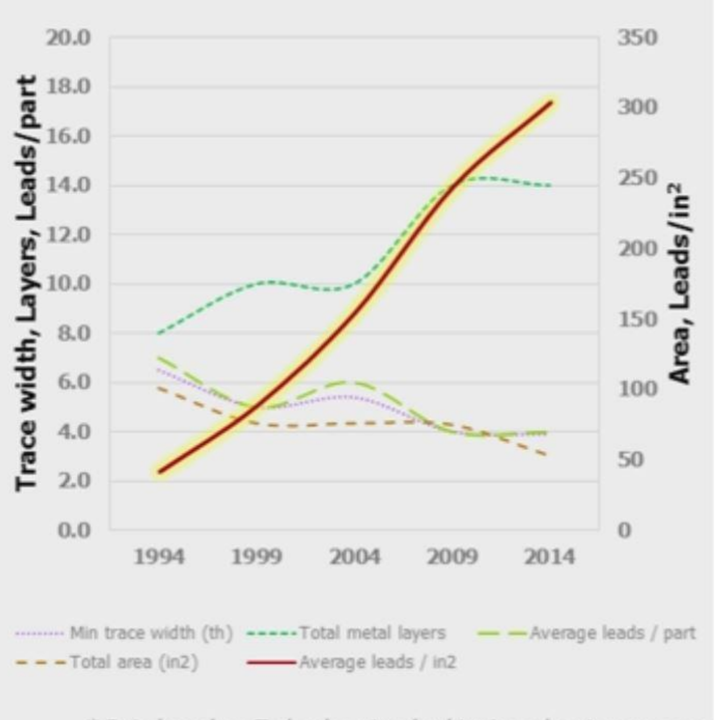
PCB Complexity is Accelerating

Trends in PCB Complexity

Design Trend	1994	2004	2009	2014
Min trace/spacing (th)	6.5/6.5	5.4/5.4	4/4	3.9/4.2
Total metal layers	8	10	14	14
Total area (in^2)	101	76	75	53
# Nets	1465	2952	3411	2109
# Pin-to-pin connections	5190	8813	10960	6228
# Components	649	1981	3400	2608
# Component pins	4214	7760	13505	10122
Leads / part	7	6	5	4
Leads / in^2	42	155	244	304



** Data based on Technology Leadership Awards entry averages*

- Use of Advanced Technologies…
  - HDI (40%), RF/Microwave (26%)
  - Flex/Rigid Flex (9%), Chip-On-Board (11%)

SI/PI Analysis in the Design Flow

PRE-LAYOUT | LAYOUT | PROTOTYPING

System Design, Pa... Sele... ar... Schematic Entry

Full Board Place-and-...ute

Prototype

EMI Testing & ...ebugging

SI/PI Analysis

To eliminate costly $$ design changes here

Signal Integrity, Crosstalk, EMC, and Timing Analysis

Board Partitioning and Critical Net Place-and-route

Post-layout Signal Integrity, Crosstalk, and EMC Verification

$

Pre-Layout

Design Constraints
Technology Investigation
Routing (topology) Options
Stackup Definition

Post Layout

Design Verification
Adhering to Constraints
Finding Design Flaws
Tuning Pre-emphasis and Equalization

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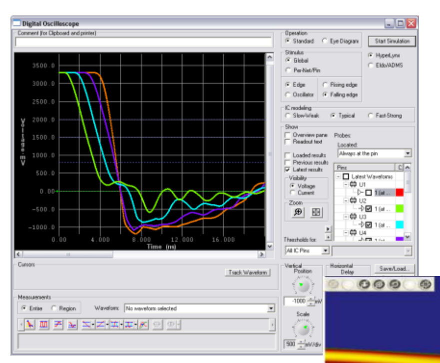
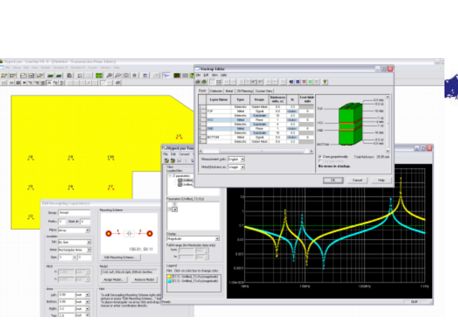
High-speed PCB Design Issues

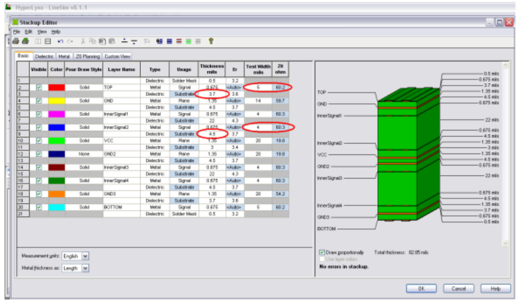
- **Signal Integrity**
  - General interfaces
    - Timing, crosstalk, signal quality
  - DDRx
    - Full STA, slew rate derating, write leveling
  - SERDES
    - Loss, impedance discontinuities, BER prediction
- **Power Integrity**
  - DC : do I have enough metal?
    - Voltage drop, high current density, neckdowns
  - AC : do I have enough caps? values?
    - Well-mounted? Good stackup?
    - Impedance profile, noise propagation
- **EMI/EMC**
  - Emission Regulations





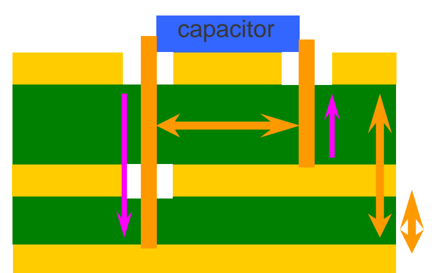
Setup/planning – Board Stackup Design

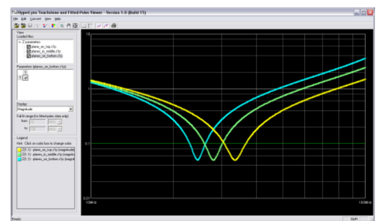
- **Signal Integrity**
  - Impedance
    - Highest impedance will drive layer thicknesses
    - Need reference planes for uniform impedance
  - Loss
    - Drives trace widths –> layer thicknesses
  - Crosstalk
    - Drives spacing requirements and routing density
- **Power Integrity**
  - Need enough thick planes to minimize DC drop
  - Need closely-spaced plane pairs for AC needs
  - Need stitching vias to relieve current choke points
- **EMI/EMC**
  - Need solid reference planes throughout stackup

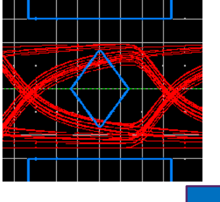


Basic | Dielectric | Metal | Z0 Planning | Custom View

	Layer Name	Usage	Thickness mils	Er	Diff Z0 ohm	Width mils	Gap mils	Z0 Curve
1		Solder Mask	0.5	3.2				
2	TOP	Signal	0.675	<Auto	100	6	6.975	
3		Substrate	3.7	3.6				
4	GND	Plane	1.35	<Auto>	100	14	12.027	
5		Substrate	4.5	3.7				
6	InnerSignal1	Signal	0.675	<Auto>	100	5	9.581	
7		Substrate	22	4.3				
8	InnerSignal2	Signal	0.675	<Auto>	60	4.5	1.169	



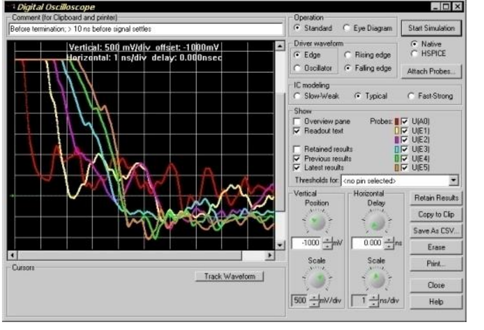




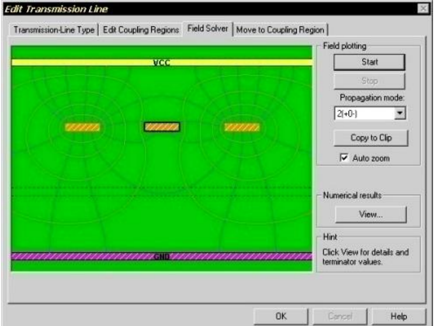
Design Considerations

- **Layout/Route**
  - Avoid crossing splits in reference planes (discontinuities)
  - Minimize Inter Symbol Interference (ISI) using matched Impedances
  - Minimize Crosstalk by isolating sensitive bits (ie. Strobes)
  - Match traces within byte lanes (DQ, DM, DQS) to minimize skews
- **Power Supplies**
  - Use precision resistors for V_{REF}
  - Short/Wide traces to minimize L and loss
  - 15~25mil clearance from V_{REF} to adjacent traces to minimize coupling
  - Decouple high frequency Power Supply noise w/caps
- **Signaling**
  - DQ Driver Impedance Matching with proper drive strengths
  - ODT is a must for better Signal Integrity (if not used then use T-branches or dumping resistor to minimize reflections
  - Choose termination carefully to balance power consumption, signal swing, and reflection
  - Use 2T timing for Address/Command

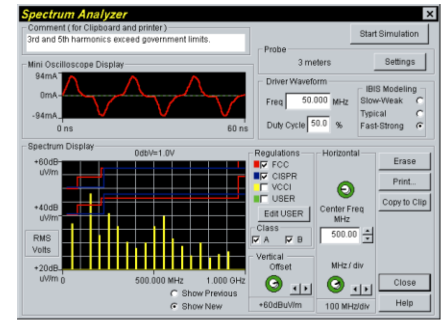
Signal Integrity Analysis



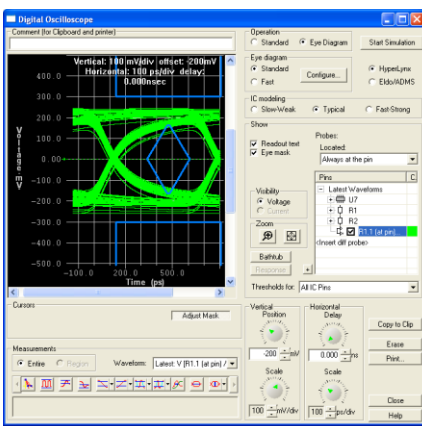
Signal Integrity



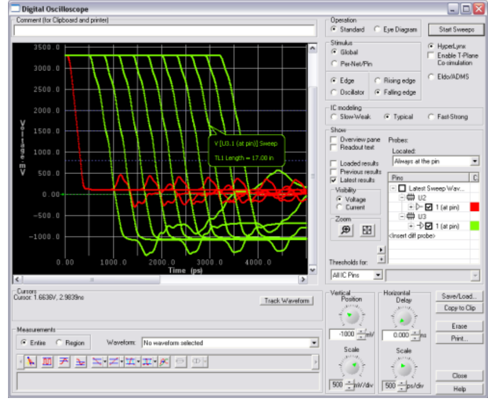
Crosstalk



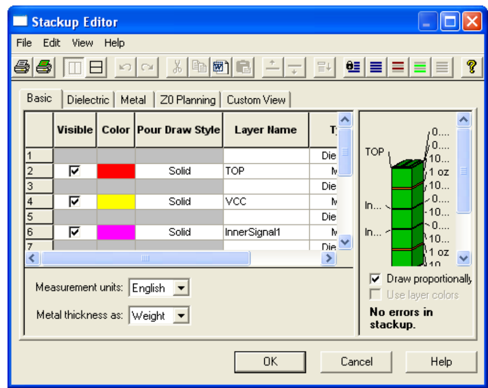
EMC



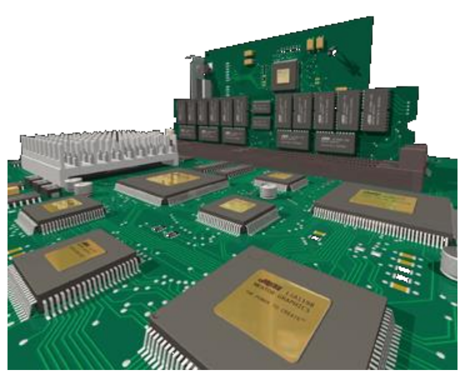
Eye Diagrams



Sweep Parameters



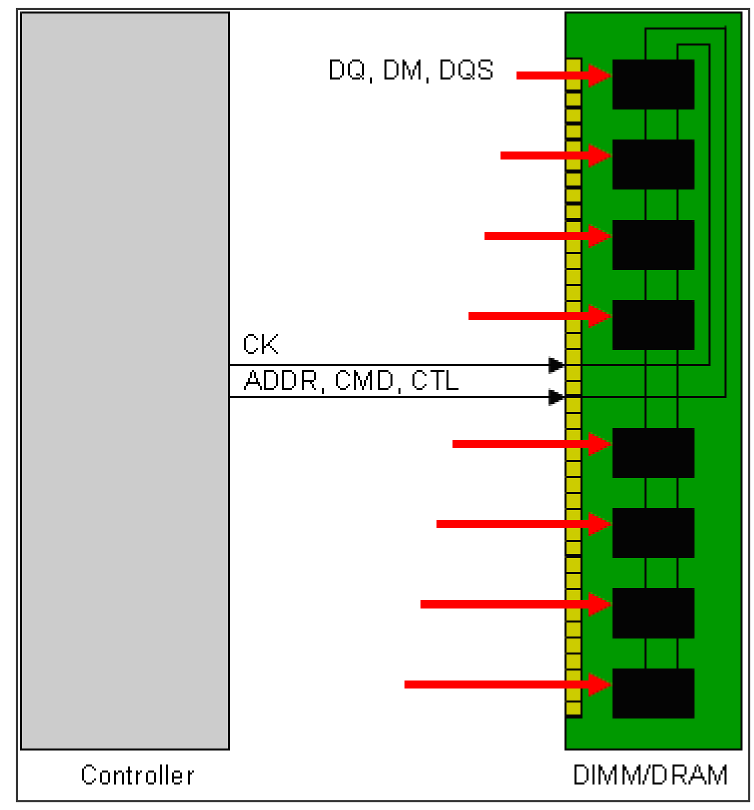
Impedance/Stackup Planning



Multi-Board

DDRx Fly-By Topology – Write Leveling

- Controller Delays DQ signals internally
- DQ & DQS signals are sent “Level” with the Addr/CLK



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Overview – DDR3 vs. DDR4

	DDR3	DDR4	Comments
VDD/VDDQ/VPP	1.5/1.5/NA (1.35/1.35/NA)	1.2/1.2/2.5	Up to 20% power saving
Clock Frequencies	400-1600MHz	800-1600MHz+	Higher BW
CAS Latency	5~14	9~24	
Vref	VDDQ/2 (Ext)	Internal	
DQ Validation	Setup/Hold	Data Eye	Borrowed from SERDES
Data Termination	VDDQ/2 (VTT)	VDDQ	Asymmetric Term.
Add/Cmd/Termination	VDDQ/2 (VTT)	VDDQ/2	
I/O Standard	SSTL15	POD12	Power savings on “1” bits
On Chip Error Detection	No	Parity (Cmd/Add) CRC (DQ)	Server Class
Bank Grouping	No	4	“Ping-Pong” for efficient use

Overview – LPDDR3 vs LPDDR4

	LPDDR3	LPDDR4	Comments
CLK	400-800MHz	800-1600MHz	2x speed (possibly more)
Bandwidth	12.8GB/s (2ch)	25.6GB/s (2ch)	Higher BW
VDD2/VDDQ/VDD1	1.2/1.2/1.8	1.1/1.1/1.8	Power reduced 10%
I/O Interface	HSUL	LVSTL	40% I/O Power reduction vs. POD
DQ ODT	Vtt Term	VSSQ Term	
CA ODT	No term	VSS Term (optional)	
Vref	External	Internal	

- DDR4 to use Pseudo Open Drain (POD)
  - Address, Command, Control continue to be SSTL
- LPDDR4 to use Low Voltage Swing Terminated Logic (LVSTL)
  - Both Data and Address

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Overview – Speed related Eye challenges

Mode	LPDDR1	LPDDR2	LPDDR3	LPDDR4
Data Rate	400Mbps	800Mbps	1600Mbps	**3200Mbps**
tCK	2.5ns	1.25ns	0.625ns	**0.3125ns**
Data eye area (Normalized)	14	1	0.5	**0.09**

Semicon West: High Performance & Low Power Memory Trends – SK Hynix

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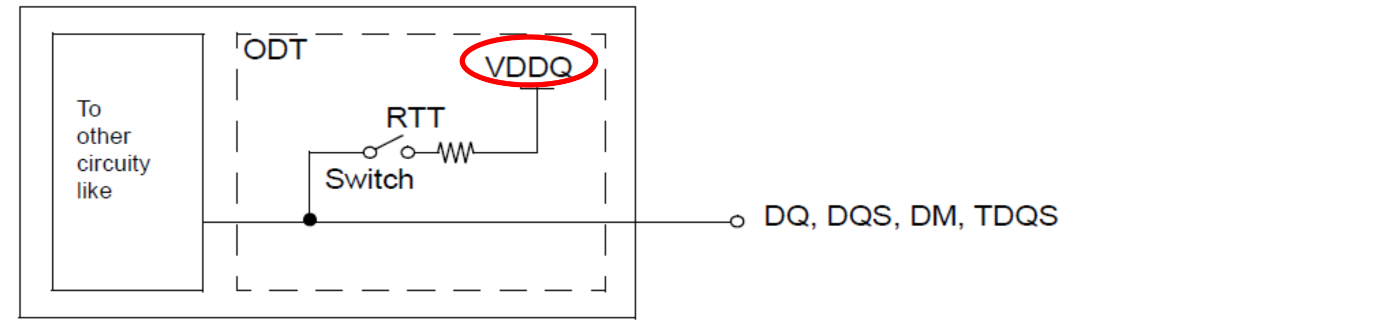
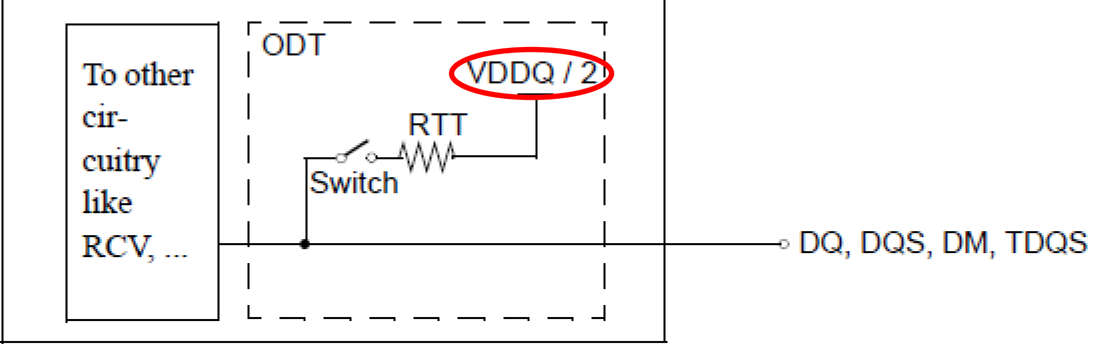
New Drive Standards – Difference



DDR4



DDR3

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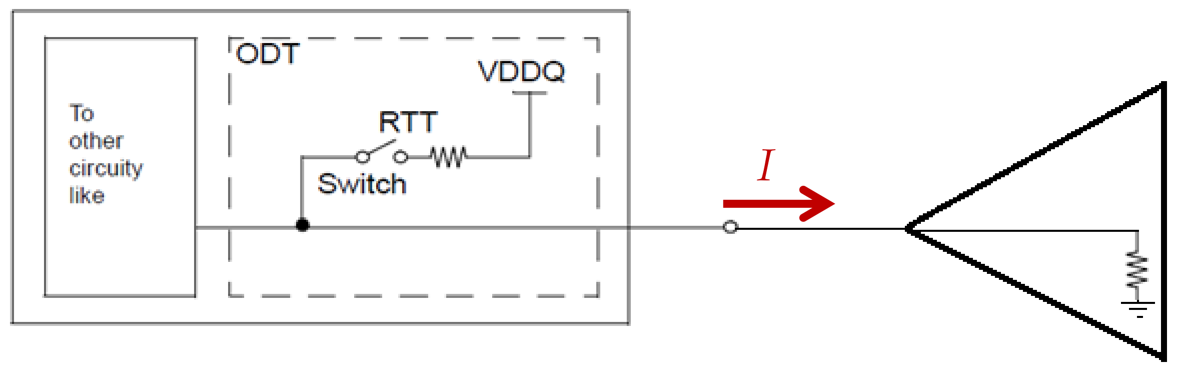
New Drive Standards – Why?

- Current still flows when driving low



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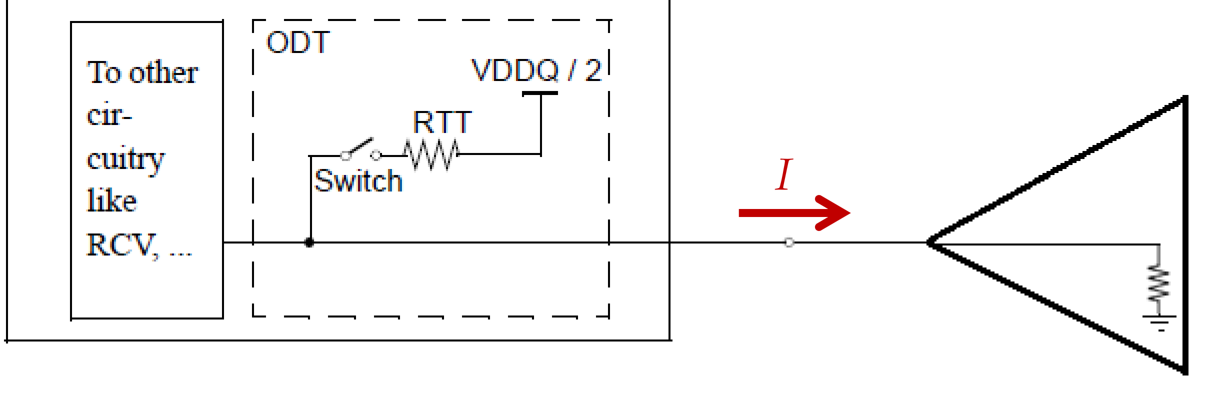
DDR4



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DDR3

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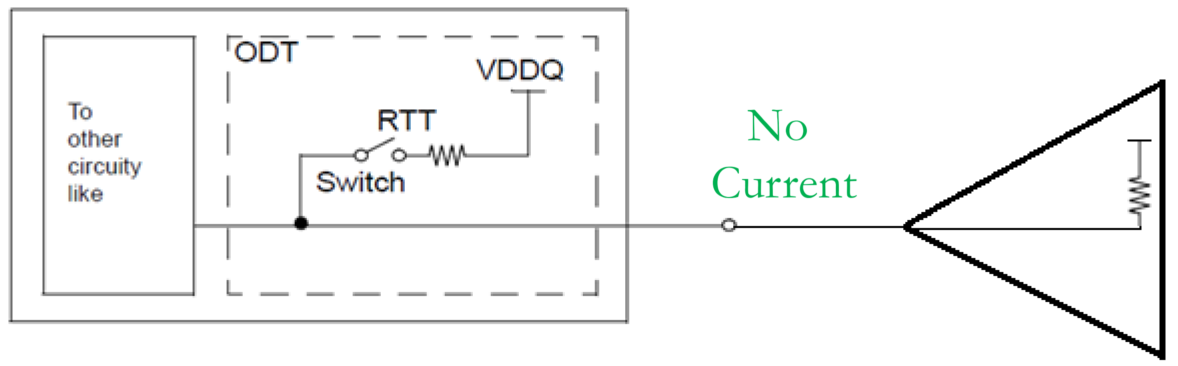
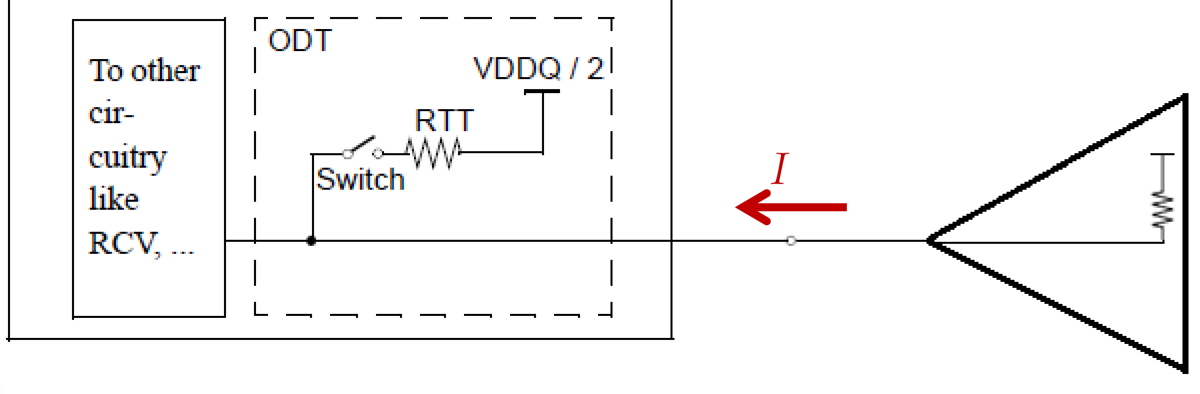
New Drive Standards – Why?

- No current draw when driving a high



DDR4



DDR3

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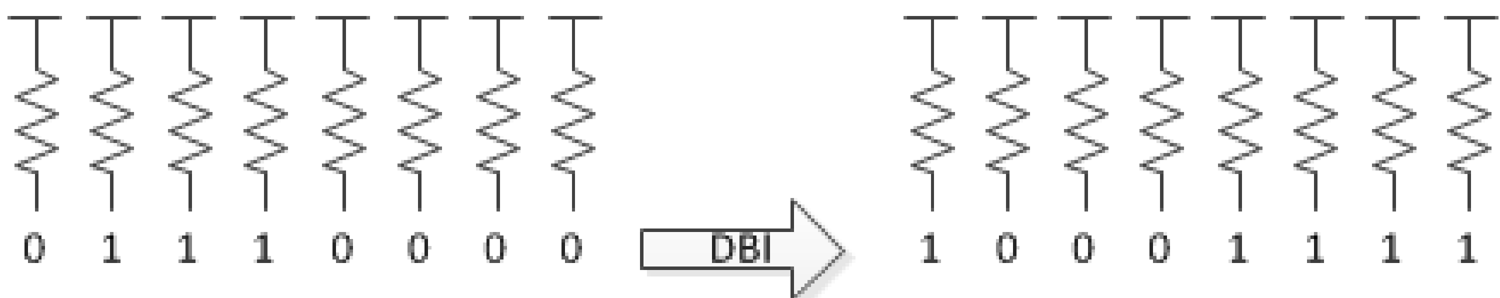
Power Savings with DBI

- Ensure more 1's than 0's with POD
- If more than 4 bits in a byte are 0, toggle bits
- DBI (Data Bit Inversion) shared with DM => only one feature enabled
- DBI pin is I/O (affects both reads and writes)



PreLayout SI Simulation

HyperLynx - LineSim v9.2 - [DDR3_AllSignals.ffs <C:\Mentor_AE\Nitin_B\DDR_Workshop\Lab1\> - Free-Form Schematic Editor]

File Setup Edit View Models Simulate SI Simulate PI Export Window Help

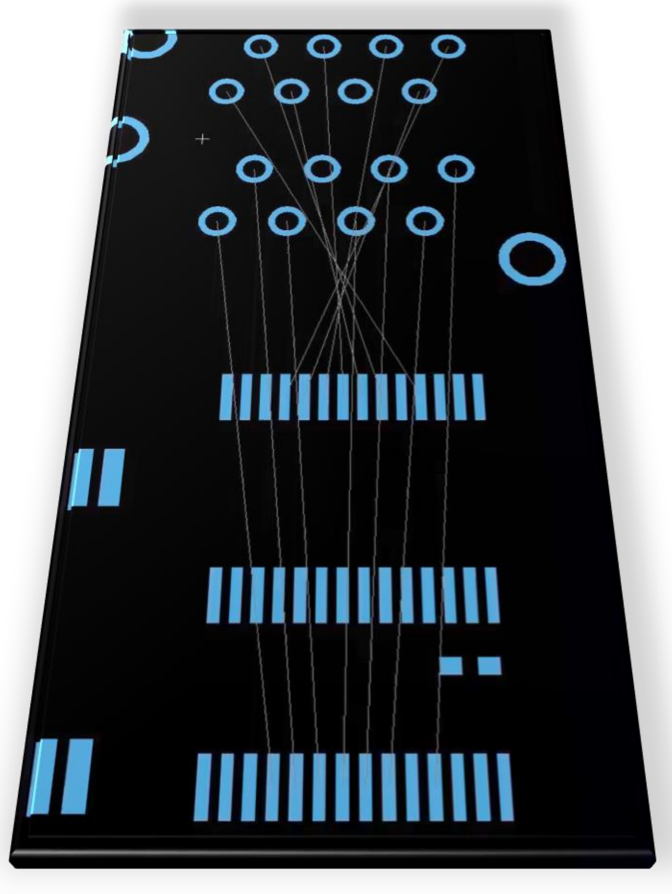
Output

:: Warning: The sum of the maximum clamp curves is not monotonic at voltage -2.4.
Success : Parse succeeded on file C:/Mentor_AE/Nitin_B/DDR_Workshop/Lab1/v89c_1p5.ibs.

X=020.050, Y=004.900 in CAP NUM

DDRx Routing Guidelines

- Constraint-driven routing
  - Designer knows where the traces should be routed
    - Precise location of traces & vias
    - Control style of routing incl serpentines
  - Things to observe while routing DDRx
    - Width & clearance rules
    - Placement intentions
    - Netline organization
    - Layer restrictions
    - Pad/via entry rules (angle, size)
    - Diff pair rules



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Using Sketch routing with DDR3 (video)

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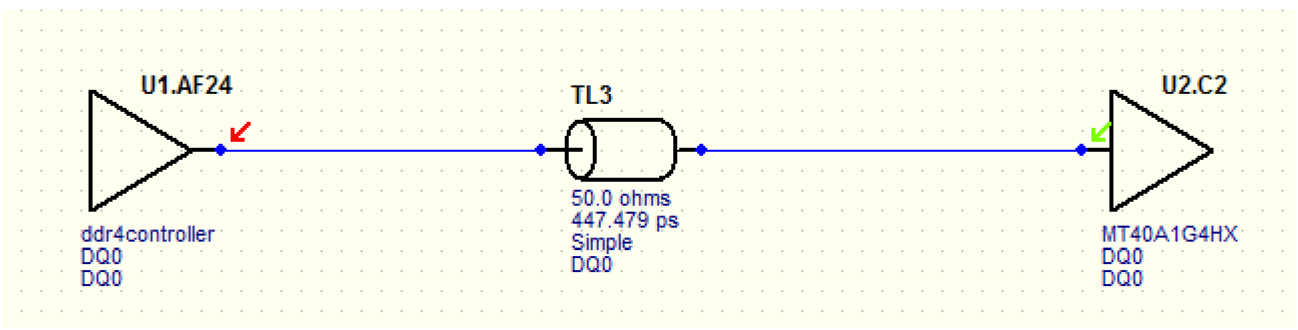
Simple Comparison



- Controller -> 50 Ohm T-Line -> DRAM
- Vary DRAM's ODT to see center level of eye
- 2400Mbps Data rate

DDR3 – sweeping Rx ODT

ODT120
ODT60
ODT40

Voltage (V)
Time (s)

No change in Center of Eye with ODT

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DDR4 – Eye shifting

Simple50_ODT4
Simple50_ODT6
Simple50_ODT8

Vinh
Vinl
ODT40
ODT60
ODT80
Voltage (V)
Time (s)

Eye center shifts with ODT change

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LPDDR4 – Eye shifting

Eye center shifts with ODT change

Xilinx VCU108 UltraScale Dev Board

HDMI Video Output
USB-UART Connector
JTAG Header
FMC1 (10x GTH)
DDR4 80-bit with ECC (5 x 16 Components)
FMC2 (10x GTH)
BPI Flash Memory
Ethernet Port (10/100/1000 Mb/s Tri-Speed Ethernet)
USB-JTAG Connector
Samtec BullsEye Connector Pads for 4 GTY Transceivers
Pmod Header
MicroSD Card Slot
CFP2 Cage (10x GTYs)
PMBus Header
QSFP28 Cage (4x GTYs)
User Clock SMAs
PCIe® Edge Connector Gen3 x8 (8x GTHs)
DDR4 80-bit with ECC (5 x 16 Components)
XCVU095-2FFVA2104E
RLDRAM3 72-bit 2 x 36 Components)

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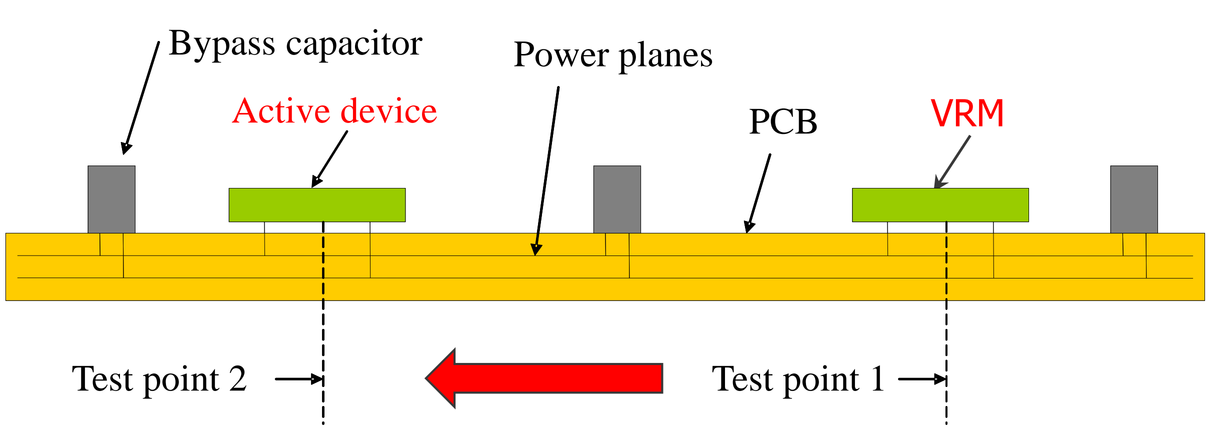
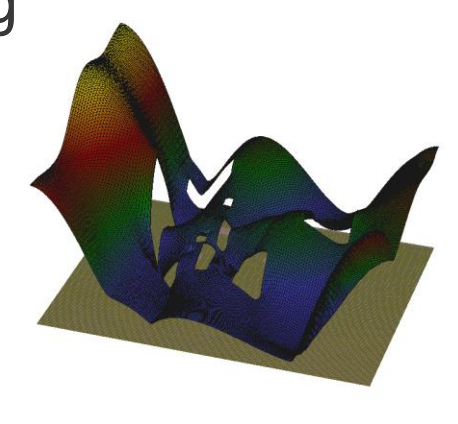
Altera Aria10GX FPGA Dev Board

FMCA (J1)
Arria 10 FPGA (U28)
FMCB (J2)
Clock In/Out SMA (J6, J7)
User Dipswitch (SW2)
LTPowerPlay interface Connector (J24)
Power Switch (SW1)
On-Board USB-Blaster II (J3)
DisplayPort Connector (J5)
MAX V CPLD (U16)
Gbps Ethernet Port (J9)
SFP+ Interface (J12)
QSFP Interface (J18)
PCIe ATX Connector (J4)
DC Input Jack (J13)
Fan Power Header (J19)
PCIe Dipswitch (SW3)
PCI Express Edge Connector (J22)
SDI Video Port (J20, J21)
HiLo Connector (J14)
JTAG Header (J17)
Transceiver TX (J15, J16)
Character LCD (B2)
DDR4 Module

What is Power Integrity?

- What is a Power Distribution Network (PDN)?
  - The path (or interconnects) from PWR to ICs (Active Devices)
  - Including PCBs and packages
    - Planes, routed traces, and decoupling capacitors
- Deliver adequate power from DC->HF
- Minimize EMI issues
- Provide low-noise reference path for signaling





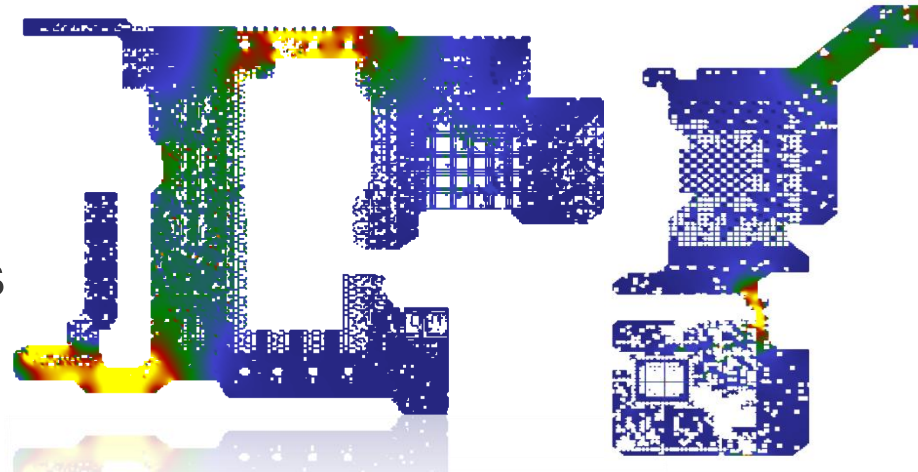
Plane Design & the PDN

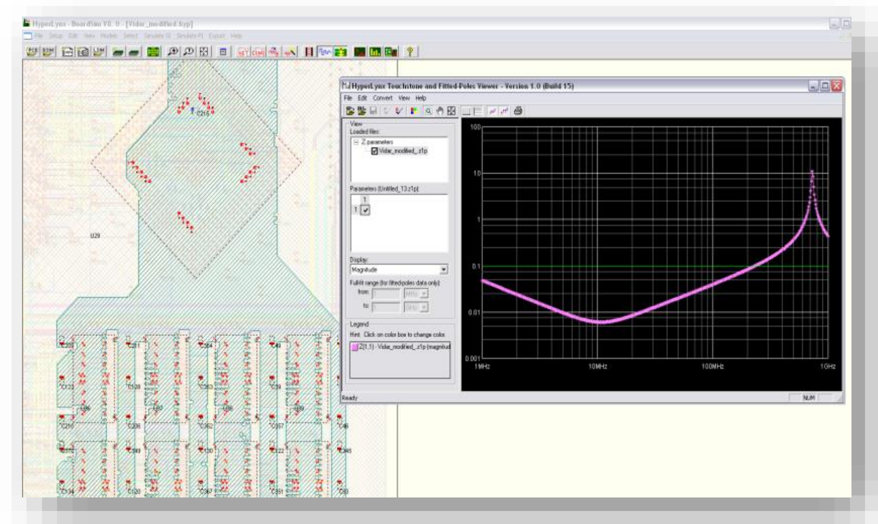
- Meeting Power Integrity requirements
  - Design PDN (path from power supply to ICs) of low impedance
    - As if an ideal voltage source were directly connected to ICs
  - Use impedance to represent and measure PDN quality

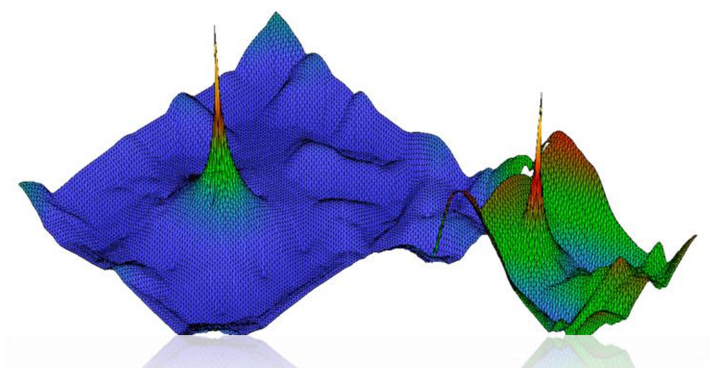
Power Delivery Path
Die
Chip to Package Bumps
Package
Package to Board Bump and/or Connectors
PCB
PCB Routing

Power Integrity Analysis

- **DC Drop Analysis**
  - Excessive Voltage Drop & High Current Densities
  - Batch Analysis of Supply Nets
- **AC Power Plane Analysis**
  - Capacitor Selection/Mounting
  - Power Supply Impedance
- **Plane Noise Analysis**
  - Voltage Ripples







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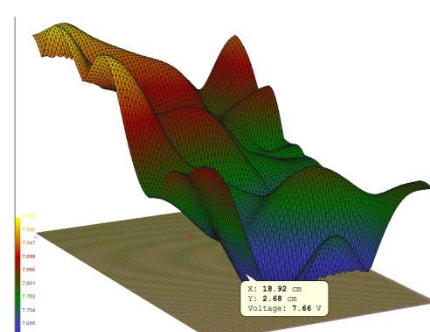
Power Integrity Optimization (Why?)

- Reduce Product Costs
  - Minimizing capacitor BOM (more Caps is worse)
  - Reducing PCB size and layer count
  - Eliminating design iterations
    - Up-front PDN planning & Improve time-to-results
- Improve Product Reliability
  - Identifying excessive voltage drop and high current densities at DC
  - Providing stable AC power through capacitor decoupling



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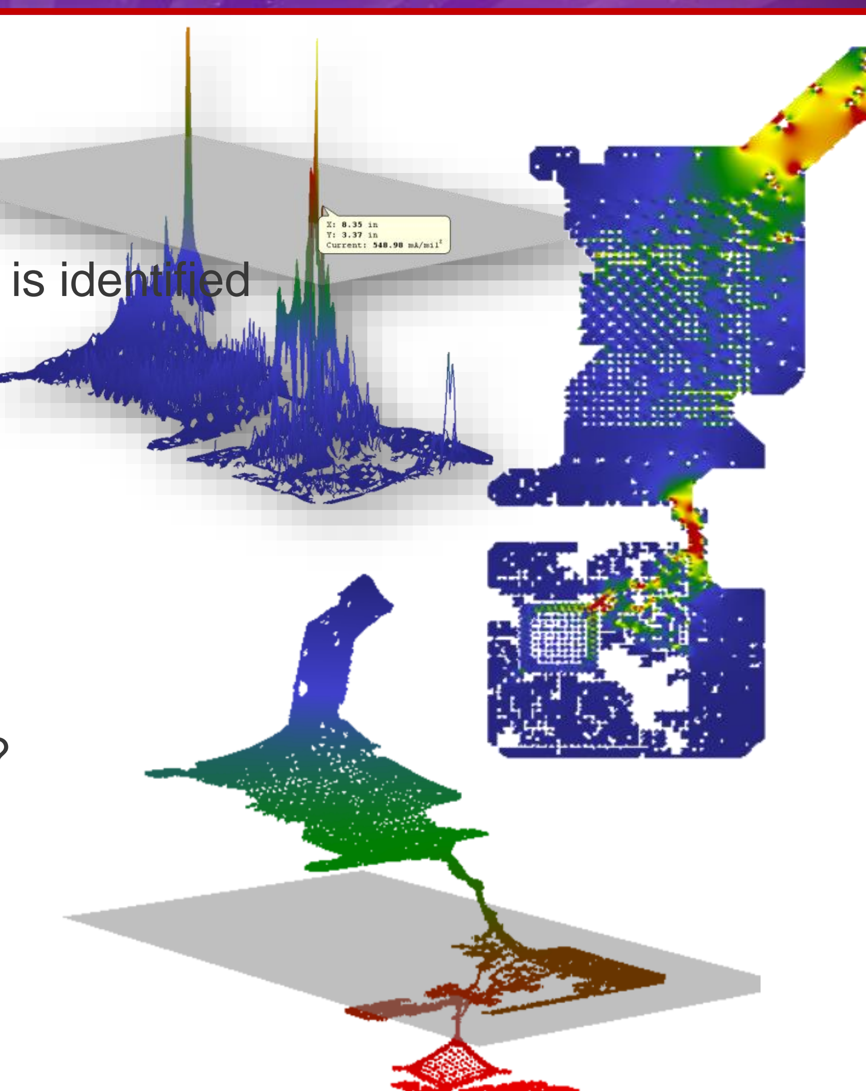
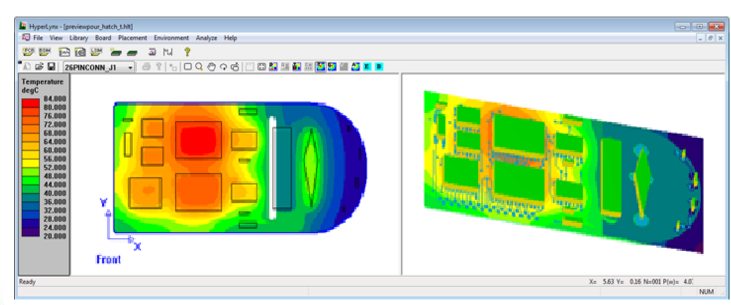
DC Drop and Thermal Analysis

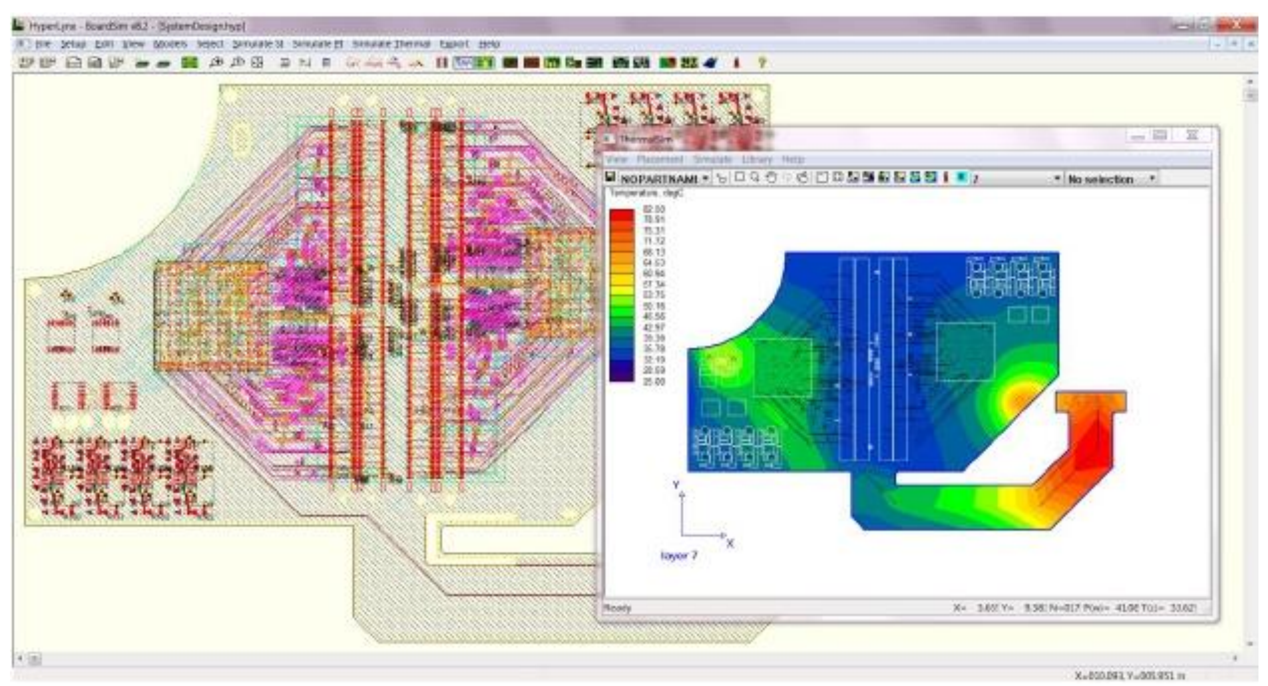
- Identify Failures Easily
  - Voltage drop magnitude is easily measured
  - Excessive current density is identified clearly
  - Determine if current density is causing thermal failure
- Create an Optimized Solution
  - How much copper is needed?
  - Optimize component placement?
  - Are additional stitching vias required?





Power Integrity/Thermal Integrity Effects

- Analyze Joule Heating effects in traces
  - Identify/localize sensitive area on board
  - Minimize field failures and increase product reliability



Power Integrity Effects

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Power Integrity Effects from DDR3 switching

Signal held high

PDN From DDR3 Board

Remaining signals PRBS @ 2400MT/s

DQS clock @ 1.2GHz

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Power Integrity Effects from DDR3 switching

U2-C2 With PDN
U2-C2 PDN Disabled

H1: 1.19786
H2: 1.04347
(dy = -154.39430M)

Voltage (V)
Time (s)

150mV noise from switching of other bits in lane

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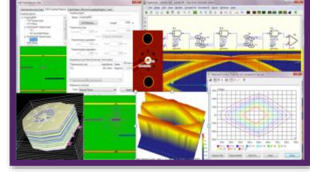
Integrated Design Flow

- Tight validation for Pre/Post Layout
- Minimize errors, increase accuracy
- Reduce risk and field failures
- Lower cost and reduce time-to-market



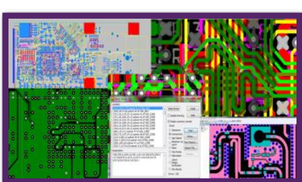
Architectural/Technology Investigation
Performance/Feasibility Analysis
Noise/Crosstalk/Termination/EMI

SI/PI/Thermal Simulation Pre/Post

Constraints

Constraints

Stackup/Placements
Length/Impedance/via

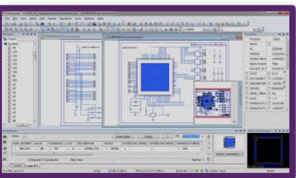


Board Layout/Route

Constraints

Schematic Design

Library/Symbols
Design Variants



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