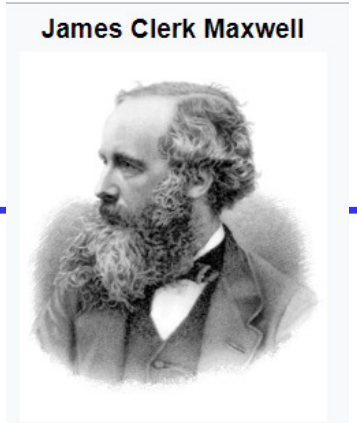
High Speed PCB Structures

Governing Equations

1861
No computers!



Maxwell Equations

$$\nabla\times\vec{E}=-j\omega\mu\vec{H}$$
$$\nabla\times\vec{H}=j\omega\varepsilon\vec{E}+\vec{J}$$
$$\nabla\cdot\left(\varepsilon\vec{E}\right)=\rho$$
$$\nabla\cdot\left(\mu\vec{H}\right)=0$$

material interfaces

$$\vec{n}\times(\vec{E}_1-\vec{E}_2)=0$$
$$\vec{n}\cdot(\varepsilon_1\vec{E}_1-\varepsilon_2\vec{E}_2)=\rho_s$$
$$\vec{n}\times(\vec{H}_1-\vec{H}_2)=J_s$$
$$\vec{n}\cdot(\mu_1\vec{H}_1-\mu_2\vec{H}_2)=0$$

impedance surfaces

$$\vec{E}_t=Z_s\vec{H}\times\vec{n}$$

Helmholtz Equation

$$\nabla\times\frac{1}{\mu}\nabla\times\vec{E}+$$
$$j\omega\sigma\vec{E}-\omega^2\varepsilon\vec{E}$$
$$=-j\omega\vec{J}$$

PEC

$$\vec{n}\times\vec{E}=0$$
$$\vec{n}\cdot\varepsilon\vec{E}=0$$

PMC

$$\vec{n}\times\vec{H}=0$$
$$\vec{n}\cdot\mu\vec{H}=0$$

metal skin impedance

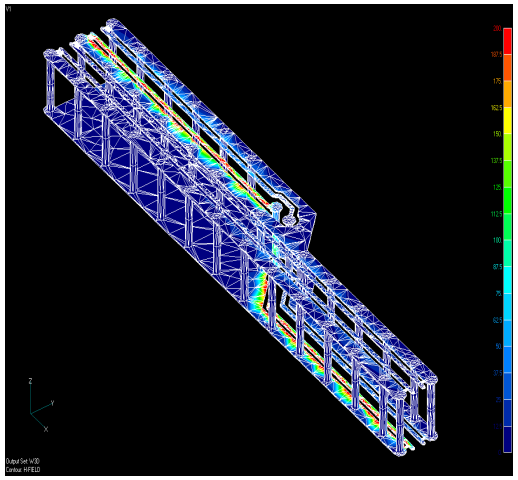
$$Z_s=\sqrt{\frac{j\omega\mu}{\sigma}}$$

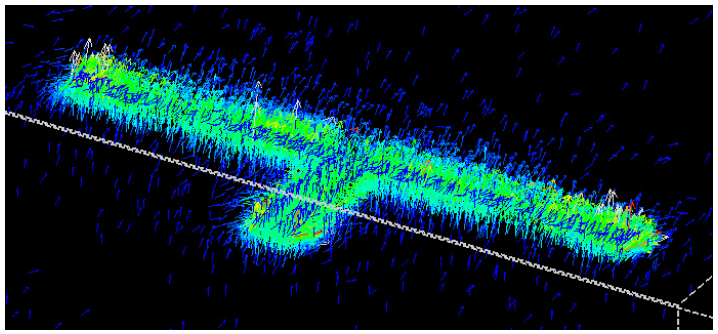
1st order ABC

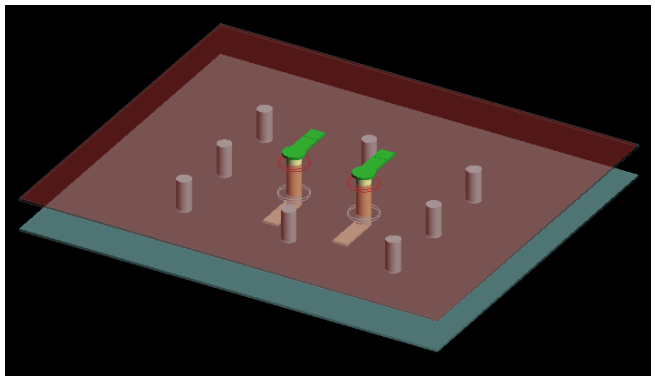
$$\vec{E}_t=\sqrt{\frac{\mu}{\varepsilon}}\vec{H}\times\vec{n}$$

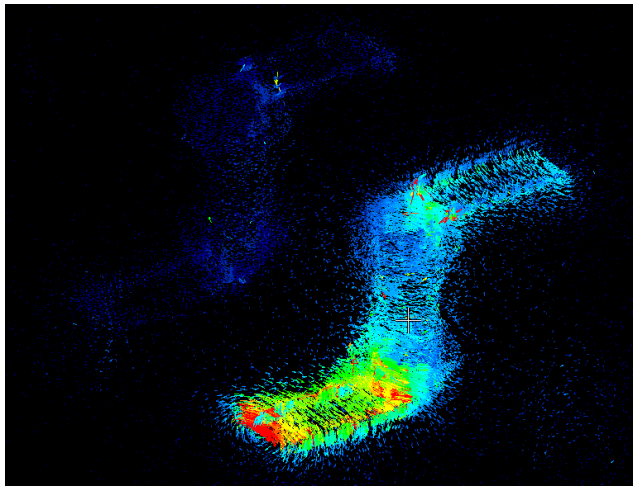
Electromagnetic fields

- The signal or energy transferred is propagated as an electromagnetic wave.



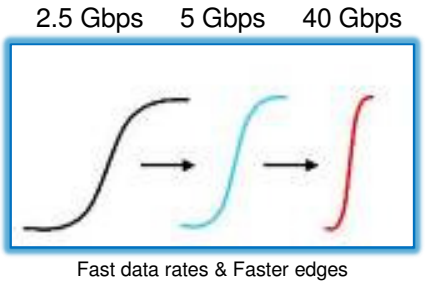






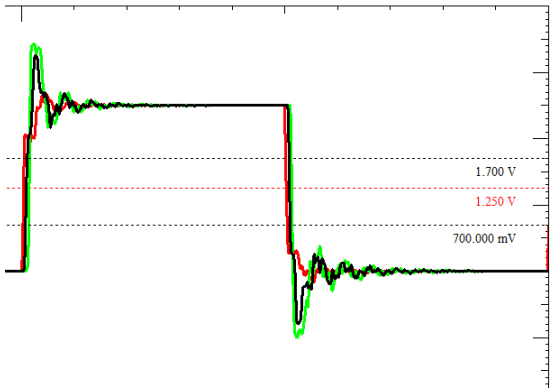
Trend Today

- Ever increasing data rates; more high speed signal routing
- Signal quality issues arise: Reflection, loss, cross-talk
- High speed is the speed at which you need to worry about it
  - Sometimes as low as 1 G
- What is DDR4, 5 and serdes at today?
  - 1.2V to 1.4V 2G 5G 12G
- DDR4 now requires eye diagram analysis



Fast data rates & Faster edges

$$V = \frac{\Delta I}{\Delta T}$$



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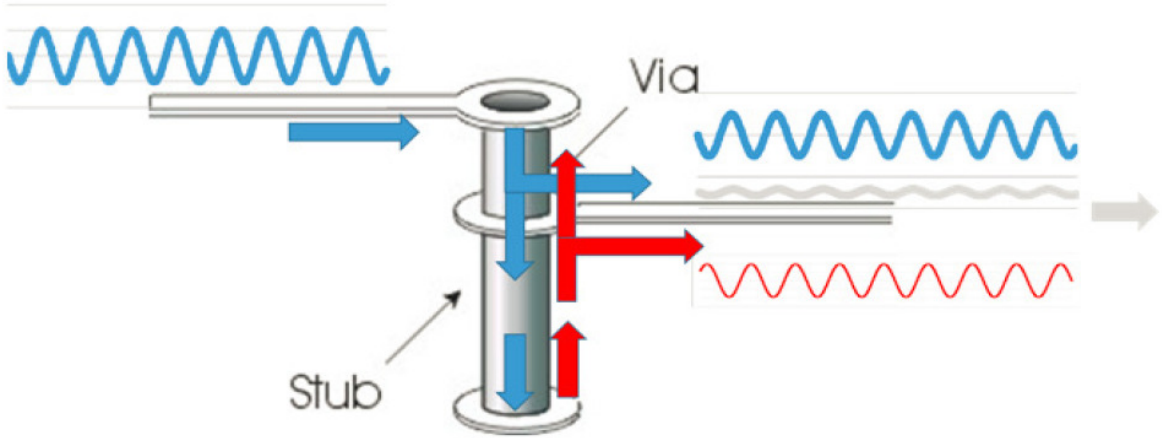
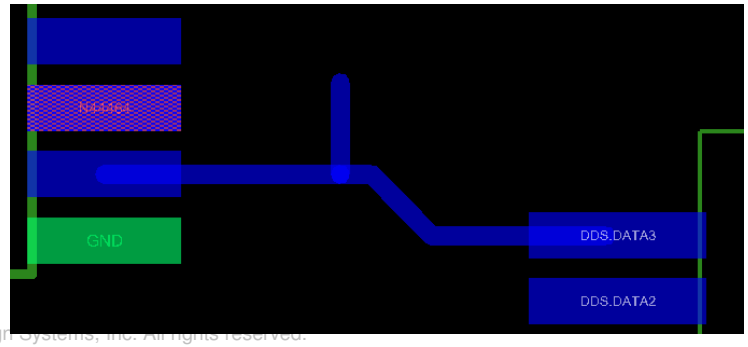
Via Stubs effect on signals

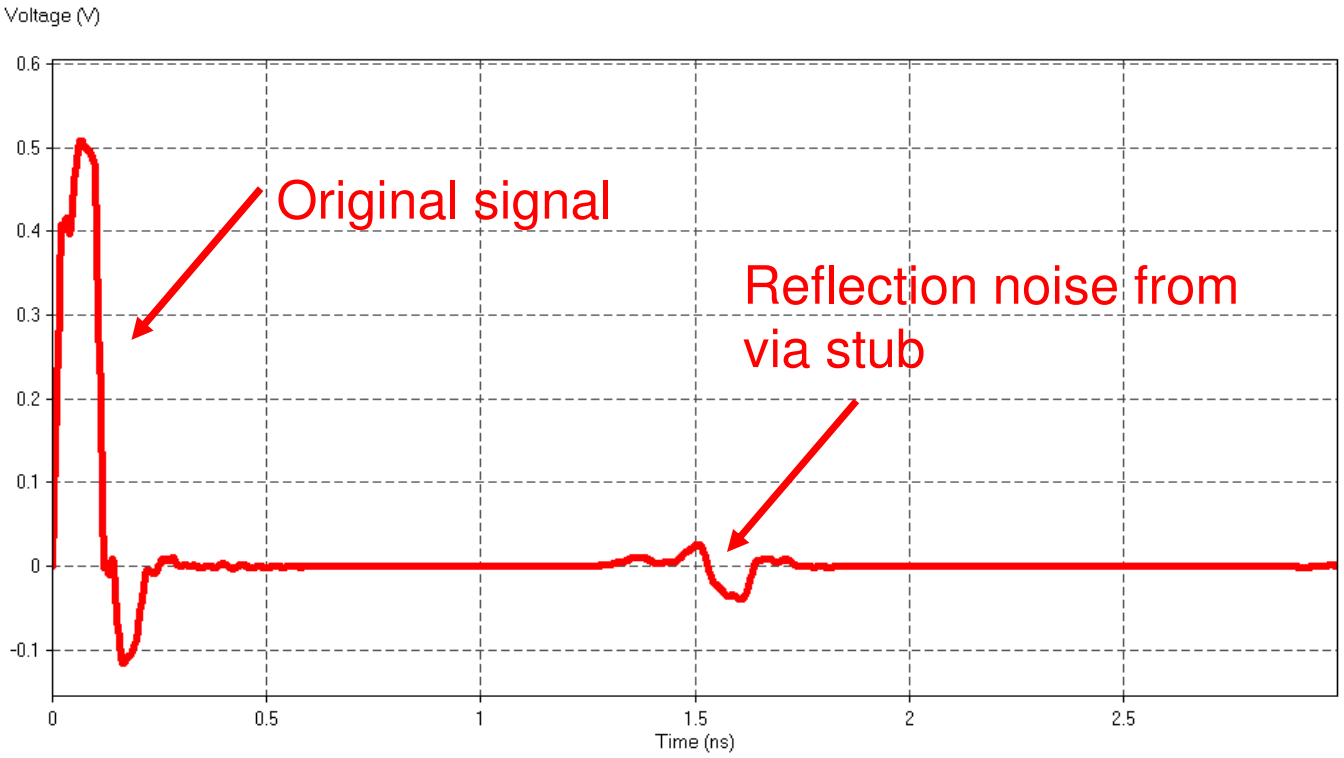
When a signal is injected into a trace it travels until it reaches the junction of the via stub and the trace. The signal splits, some continues to the receiver while some continues to the bottom of the stub. At that point it reflects back up interfering with the original signal



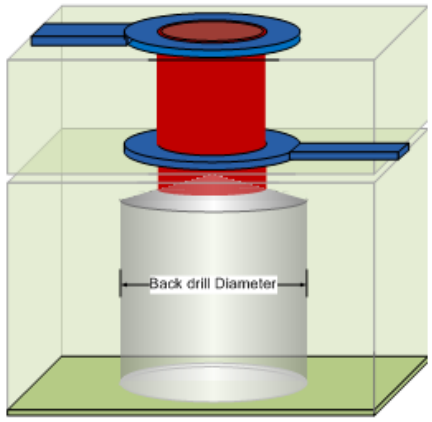


A Via Stub is electrically similar to a T in a routed trace

Effect of a via stub in time

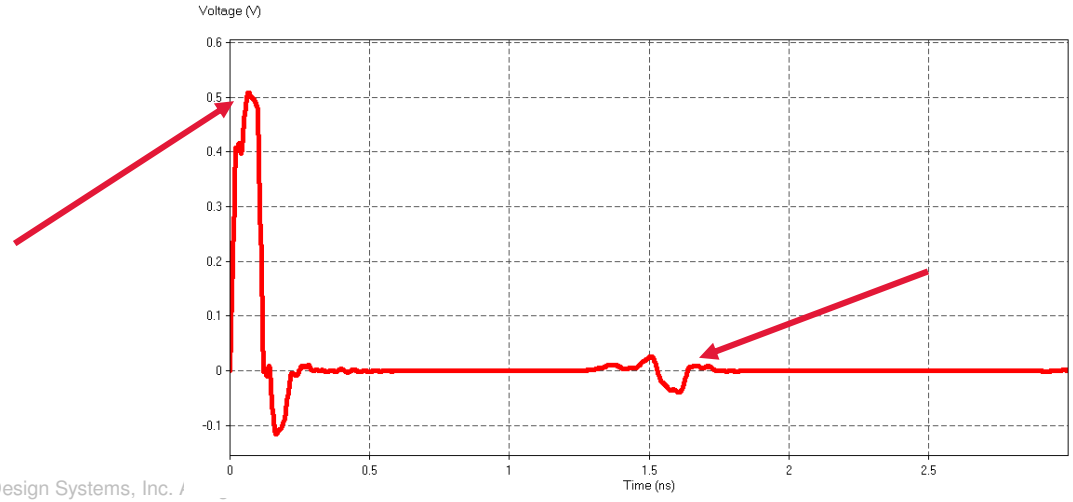


Backdrill

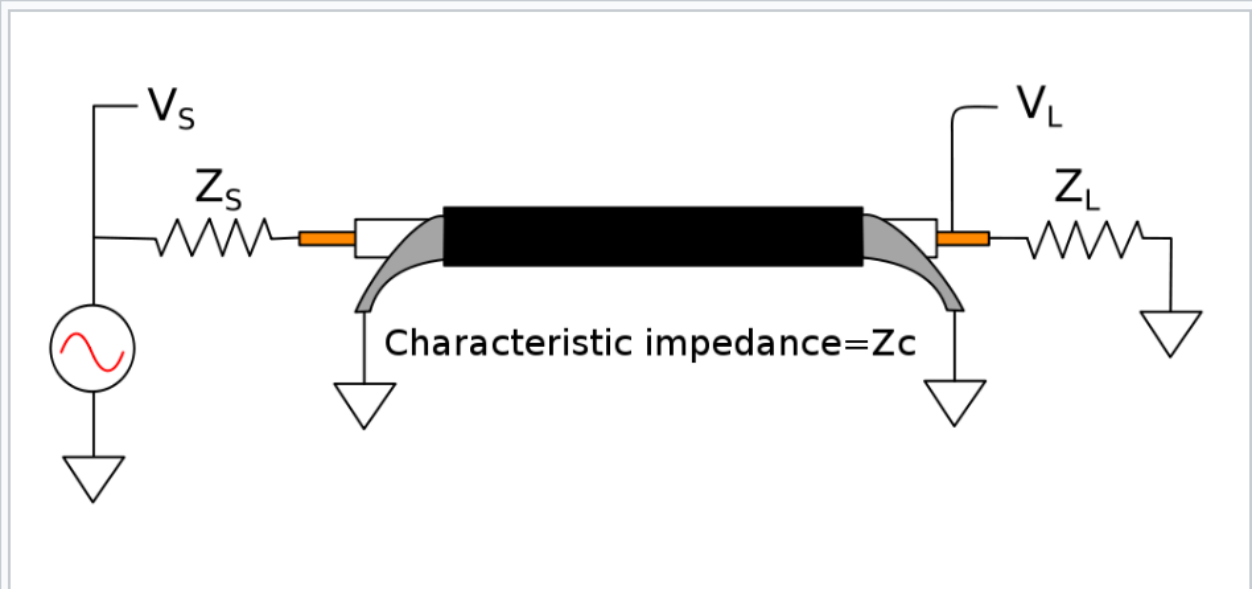


Drilling the via stub away eliminates the reflection issues
-More accurate high/low voltage
-Less ringing and noise

Do you need to backdrill every via?
No
It's a trade off between cost and performance



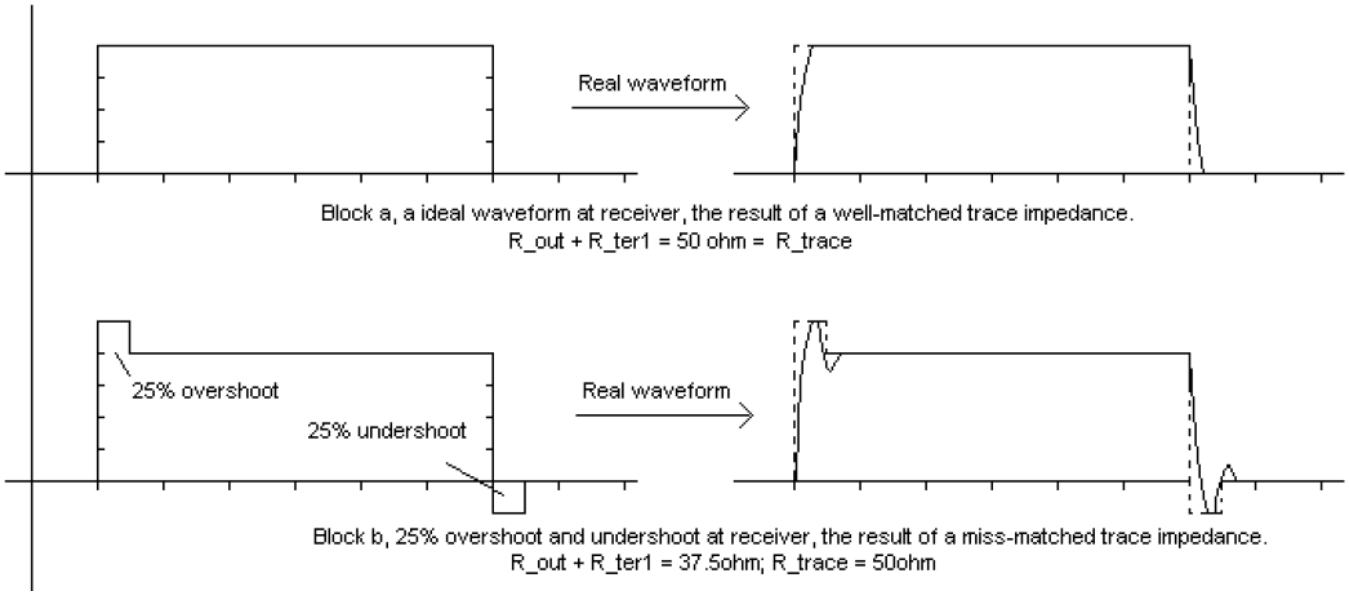
Impedance



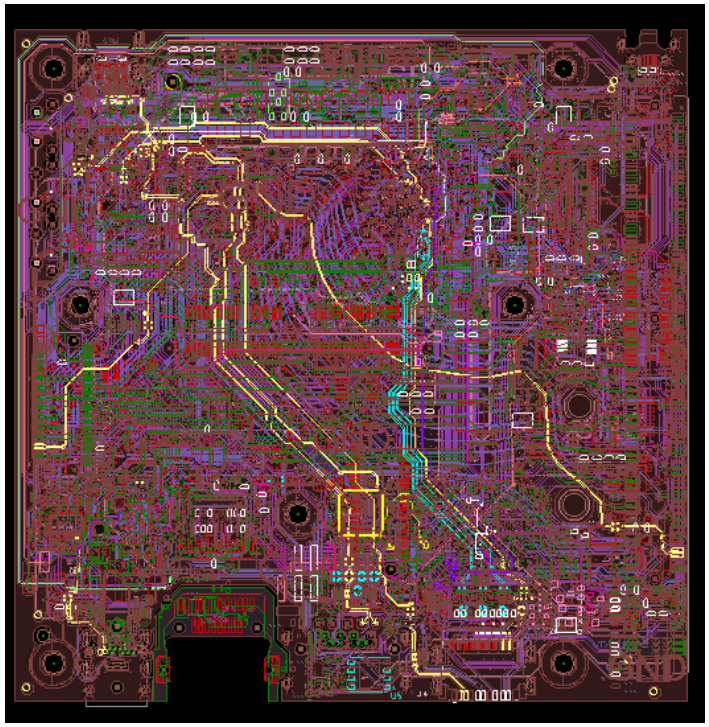
The purpose of a transmission line is to get the maximum amount of energy to the other end of the line (or to transmit information with minimal error), so the reflection is as small as possible. This is achieved by matching the impedances so that they are equal

Impedance

- Impedance discontinuities generate reflections.
- Reflections cause temporary ringing (voltage oscillations above and below the eventual steady-state level)



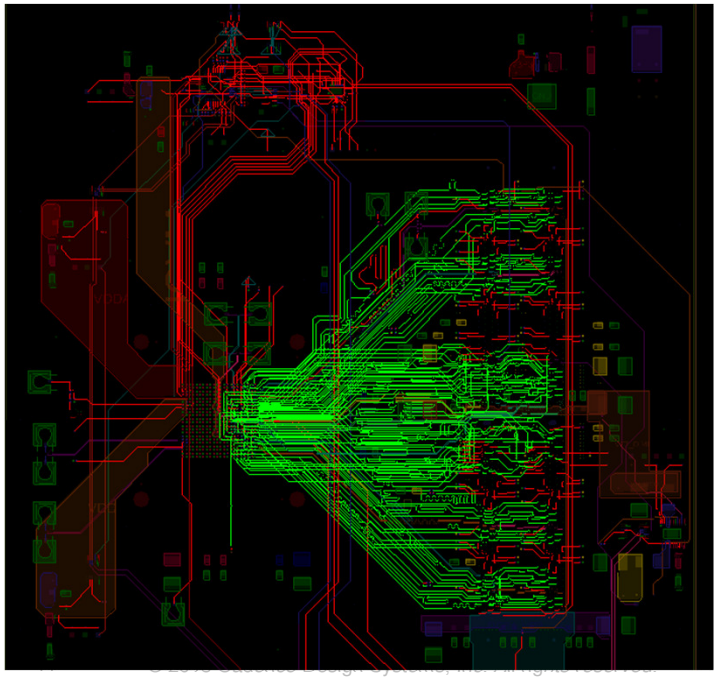
Where are the impedance problems?

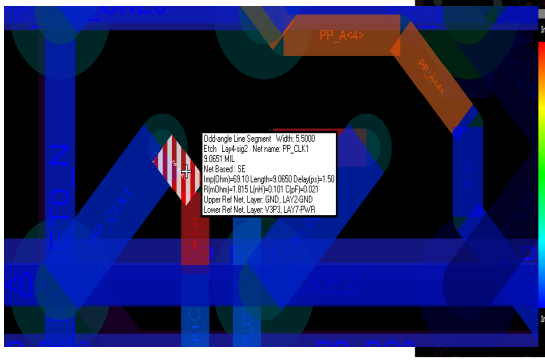


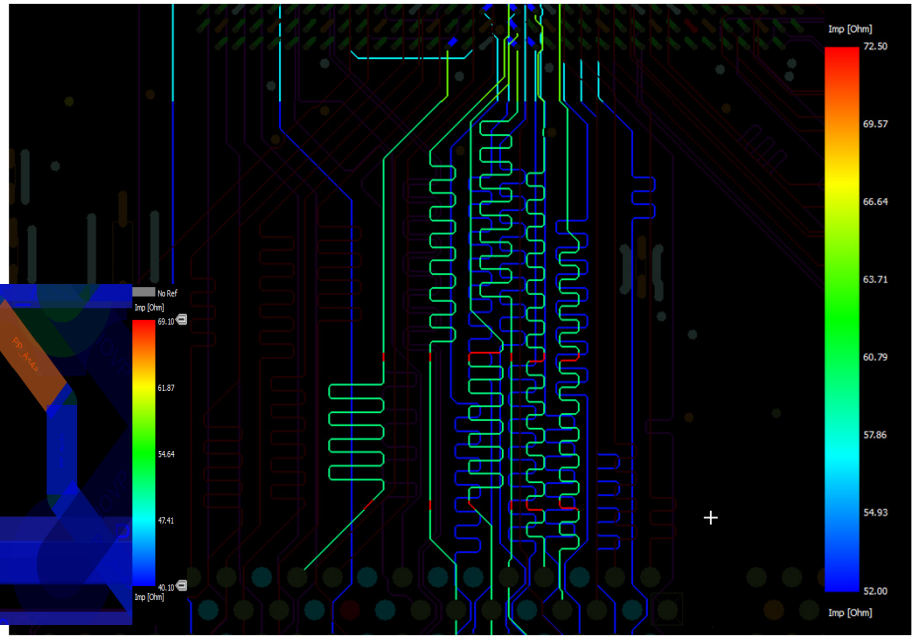
Rules of thumb and line width rules may no longer cut it

Impedance discontinuities examples

- Major issues caused by stackup or line width change
- Hard to find segments tweaked for routing
- Impedance change due to gap in return path







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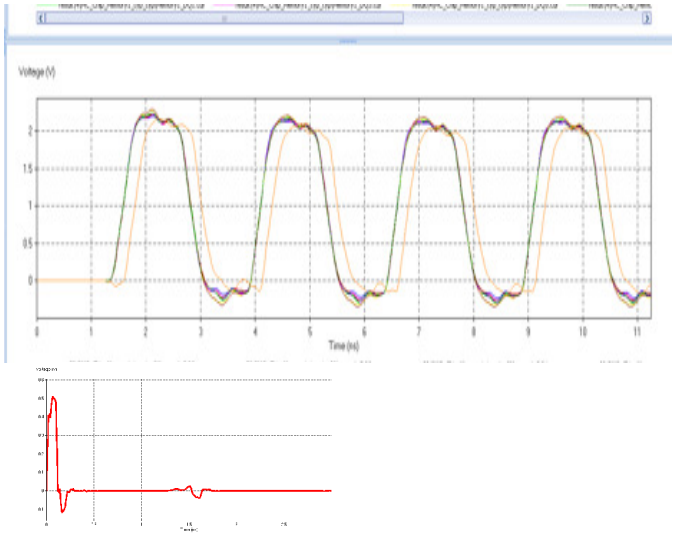
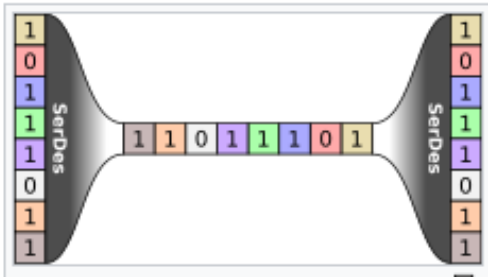
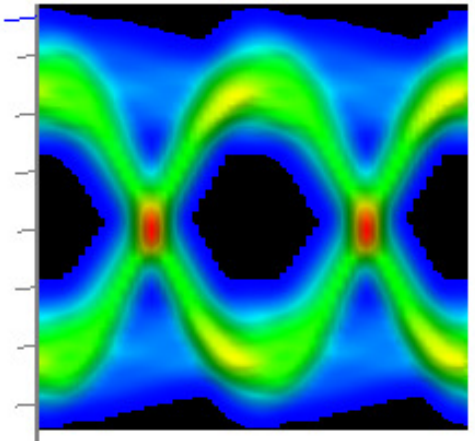
What's an Eye Diagram

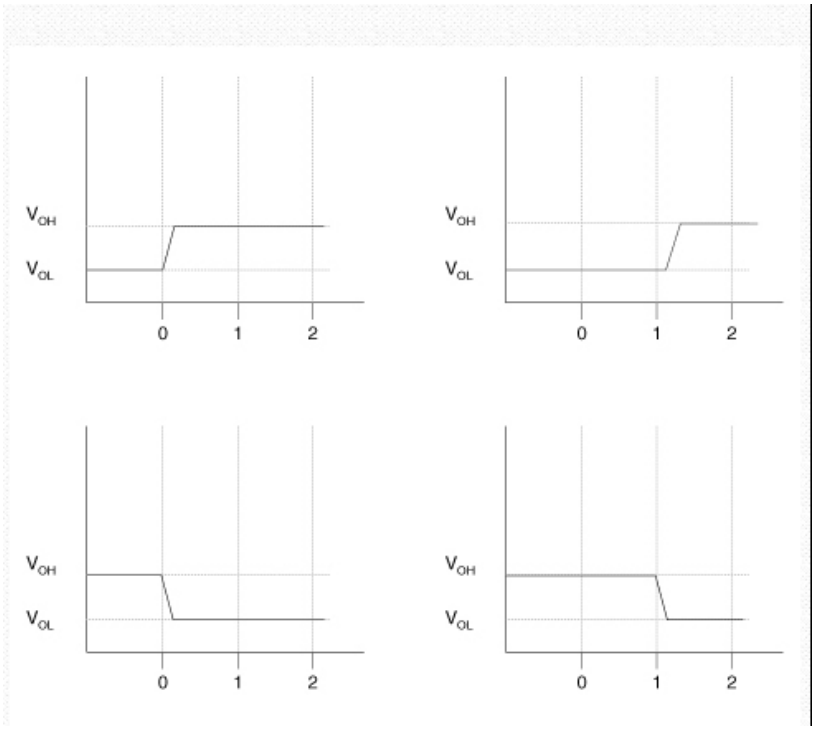
- High speed differential interfaces like DDR4 or PCIE carry billions of bits.
- An Eye diagram is a method to ensure every single one of those bits will be properly received
- A simulation is run, capturing the waveforms for each 0-1 and 1-0 transition.
- The waveforms are then super-imposed on top of each other
- The results look like eyes, the opening is the area where the signal is samples at the receiver

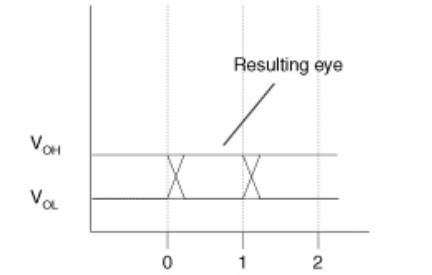




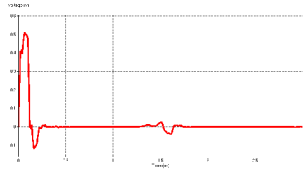


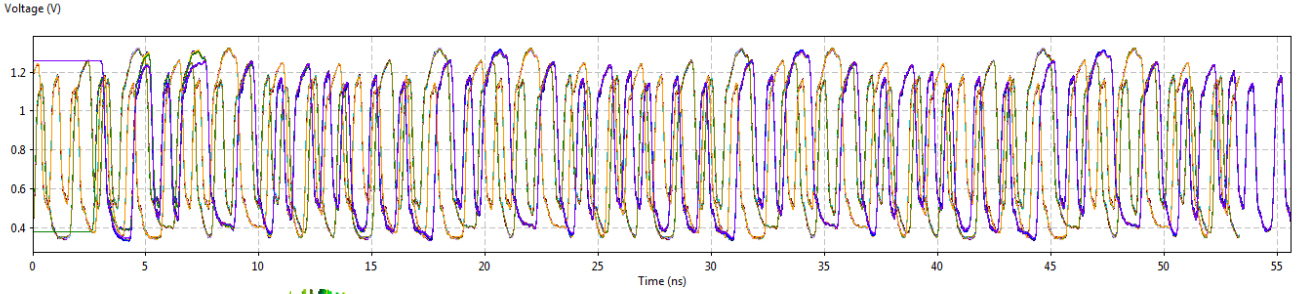
Bit sequences 011, 001, 100, and 110 are superimposed over one another to obtain the final eye diagram.

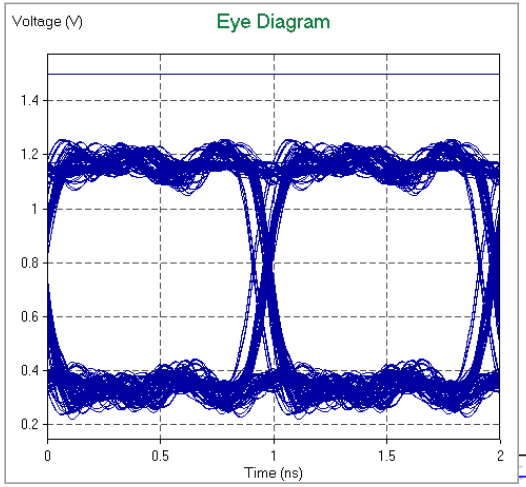


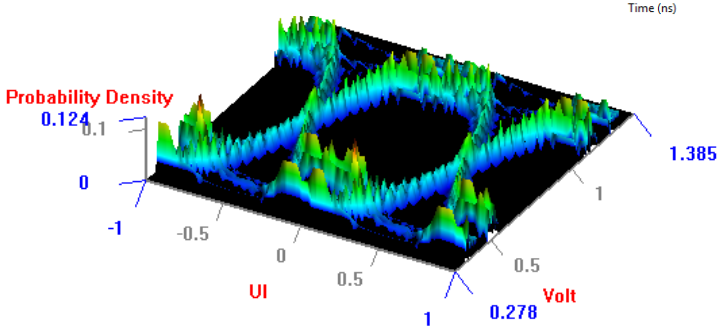


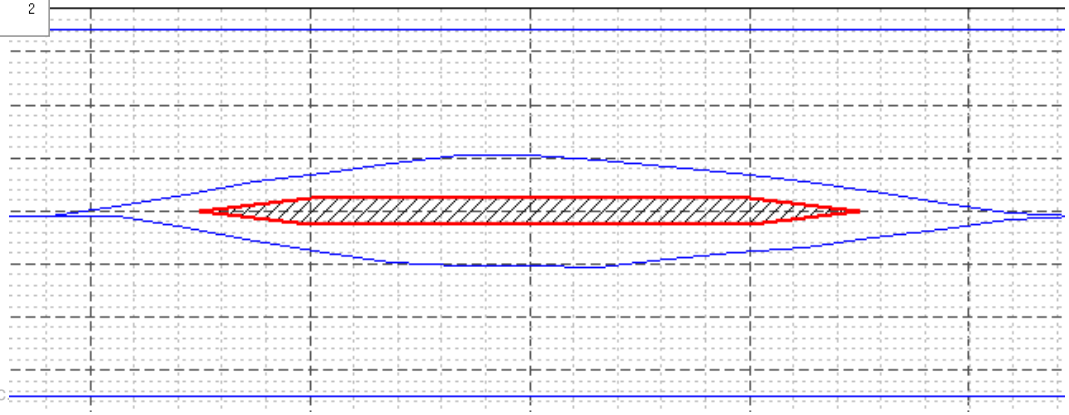
What's an Eye Diagram











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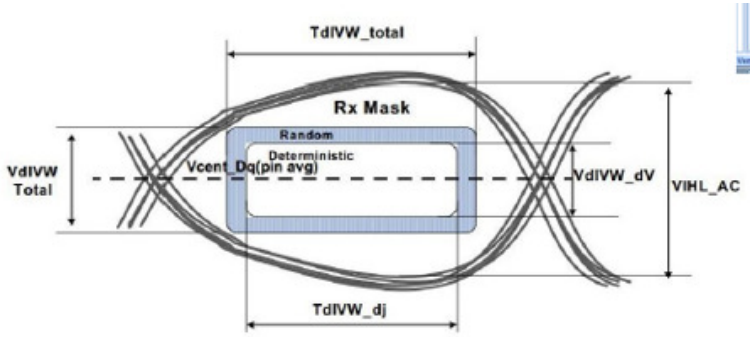
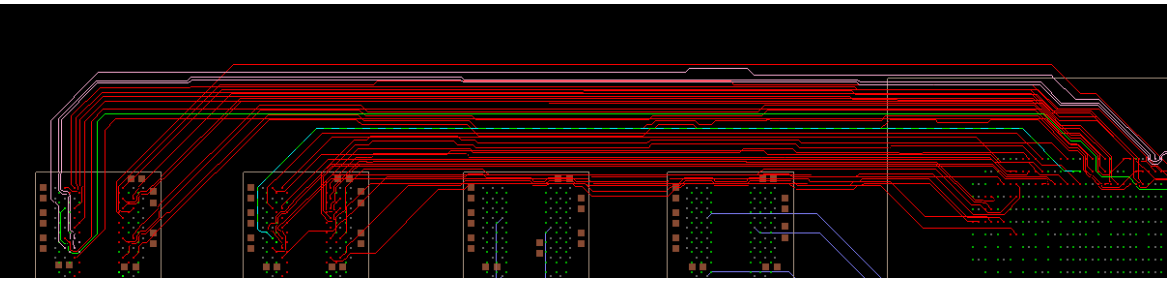
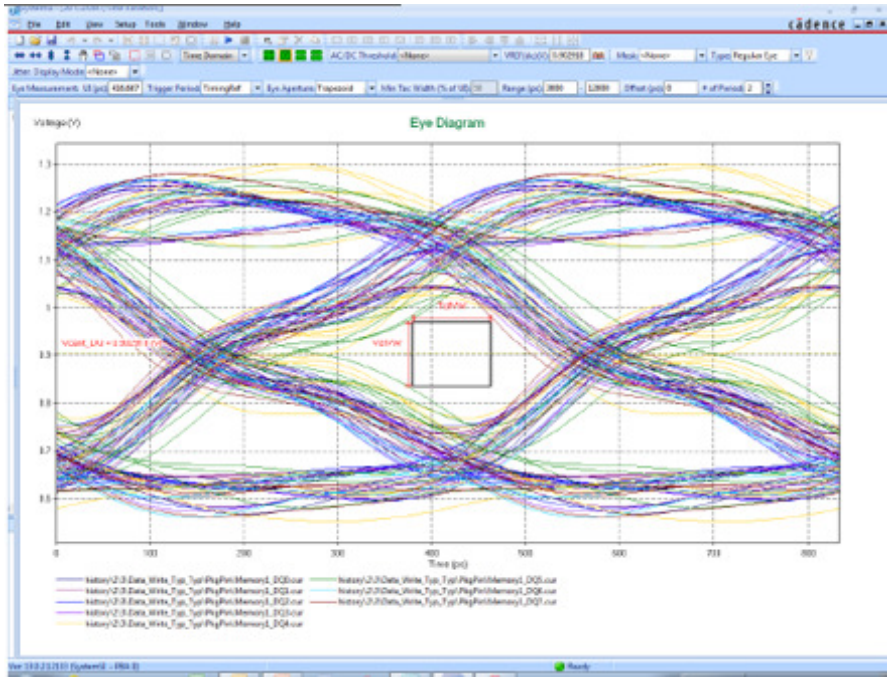
DDR4 compliance
How an Eye diagram is used

Relative Propagation Delay Match Groups

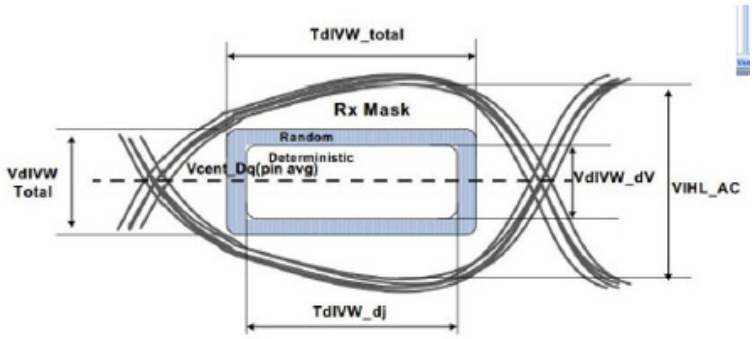


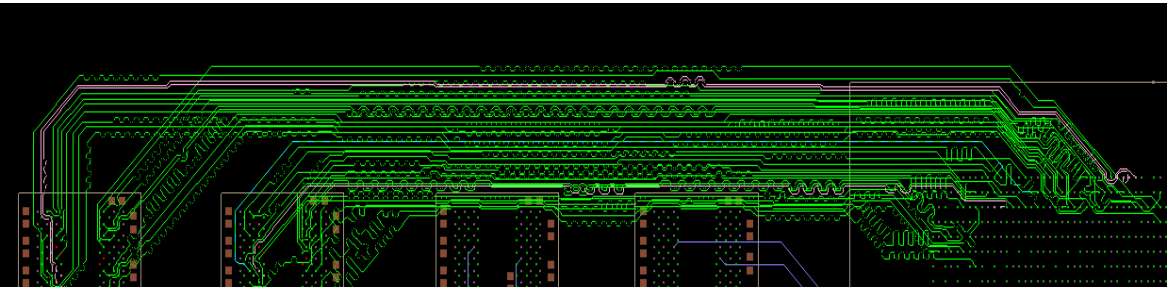


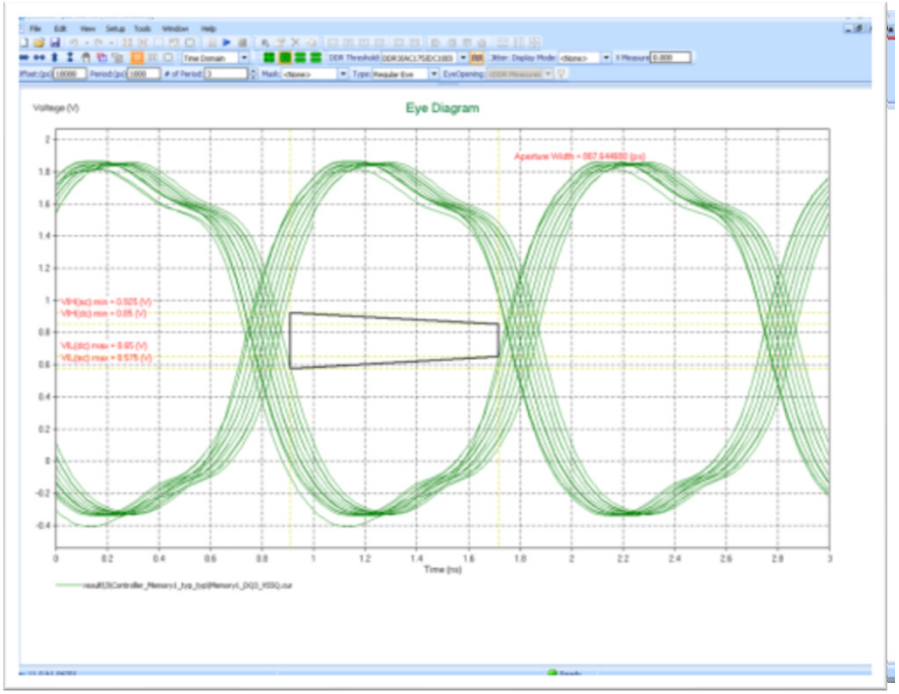


DDR4 compliance
How an Eye diagram is used

Relative Propagation Delay Match Groups

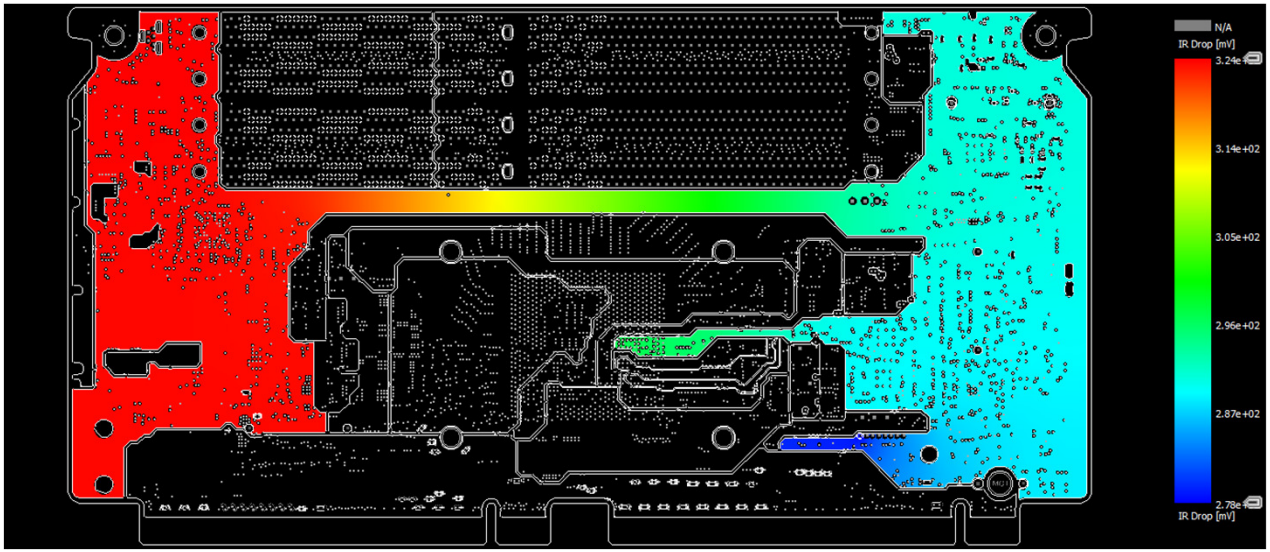


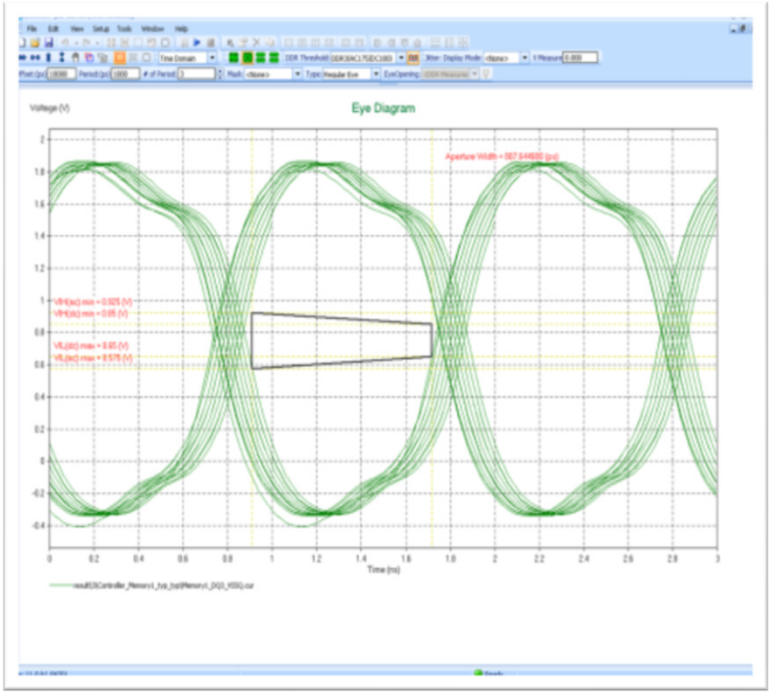




How does DC analysis contribute to eye diagrams

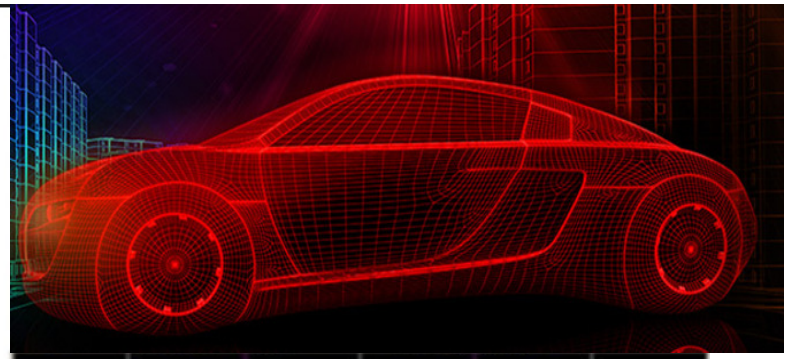
- Proper supply voltage contributes to the height of the eye

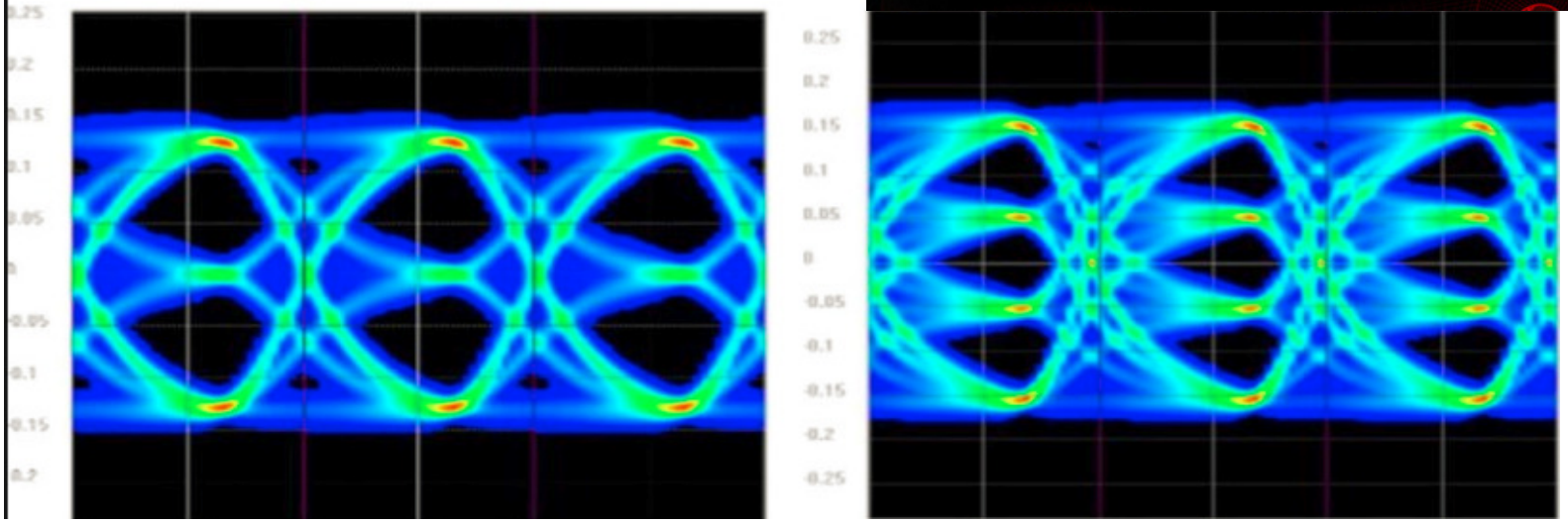




Pulse Amplitude Modulation
3 or 4 logic states instead of only 2

- PAM3 and PAM4 signaling and simulation
- PAM-aware example AMI modeling





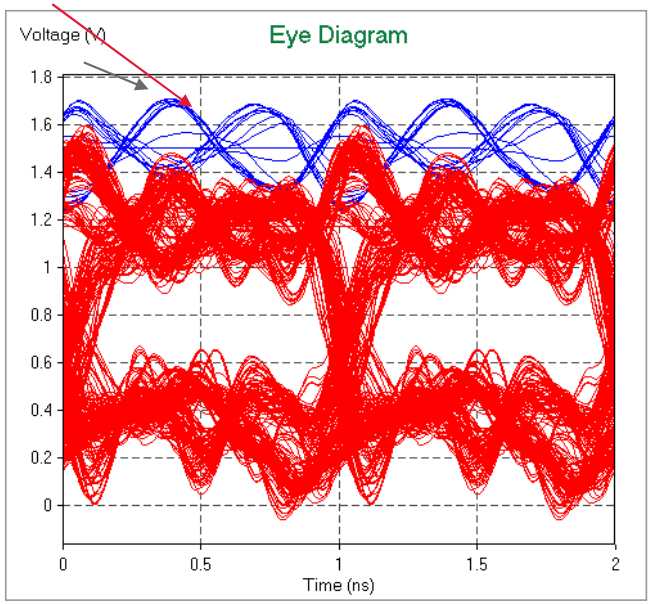
Loop Inductance
"Worthless decoupling capacitors"

Power Aware

- Power needs to be accounted for as well as the signal
- Coupling with other signals also needs to be accounted for

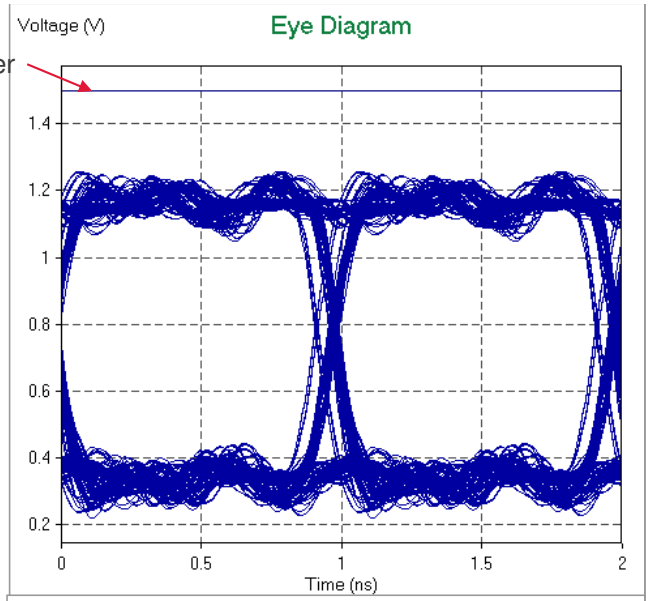
Power Aware

Real PDN



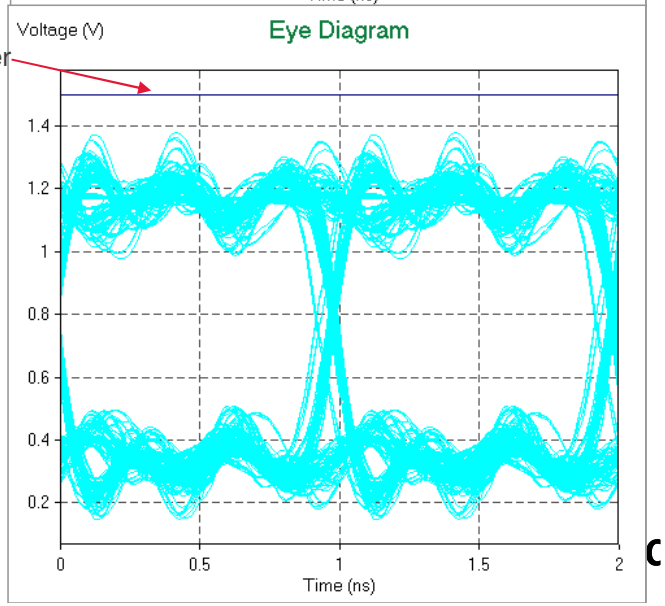
Ideal Power

no Coupling



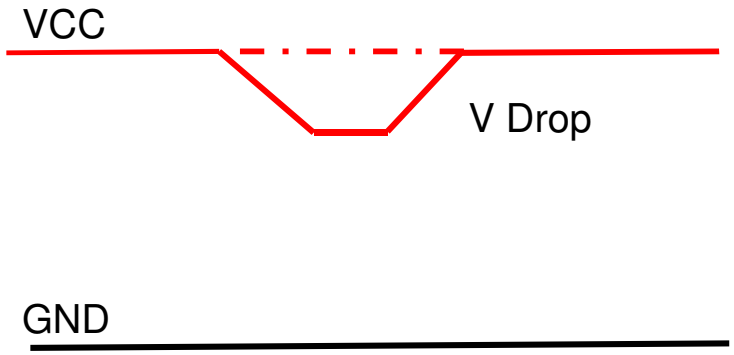
Ideal Power

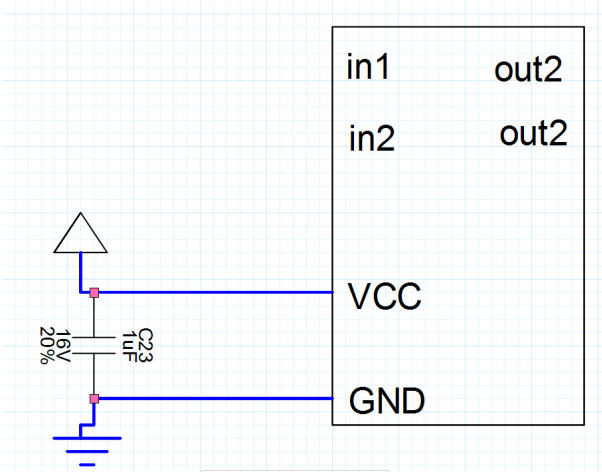
With Coupling



How a decoupling capacitor maintains ideal power

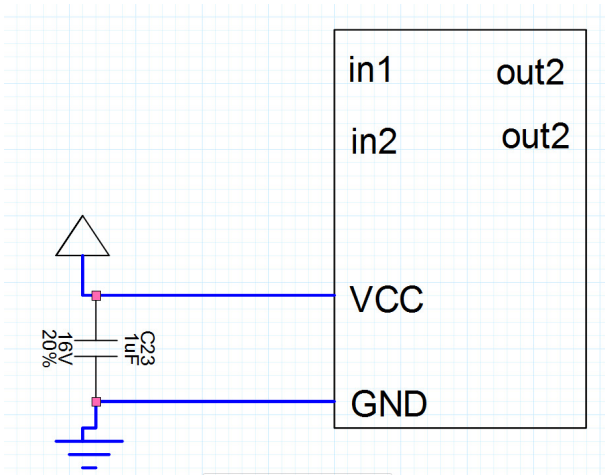
- A De-Cap reacts to change in voltage by releasing it's charge
- Ideally that charge compensates for the change in voltage, caused by noise or IR drop, seen by the IC

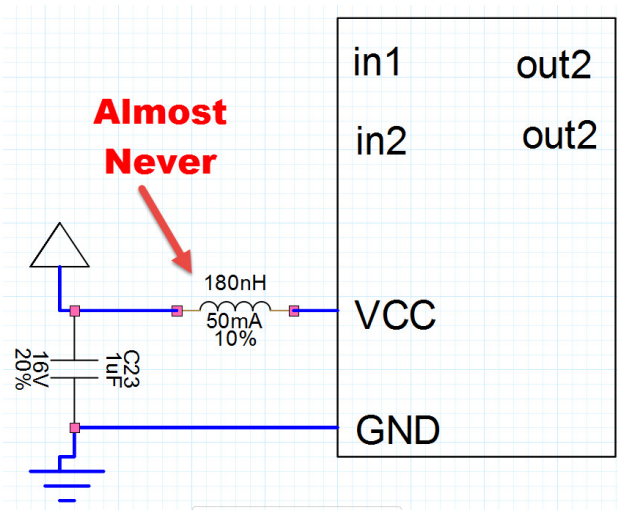




How a decoupling capacitor becomes useless through loop inductance

- How often does the hardware designer place inductors in series with the decoupling capacitor





- So as a layout designer you have to be careful not to make an inductor out of metal

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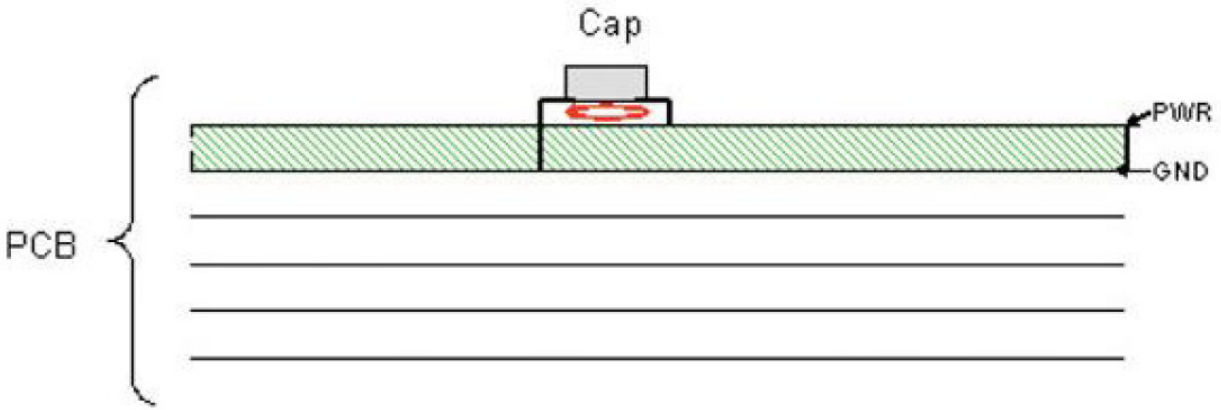


Figure 2. Low inductance connection with capacitor mounted on top of board.

Do this

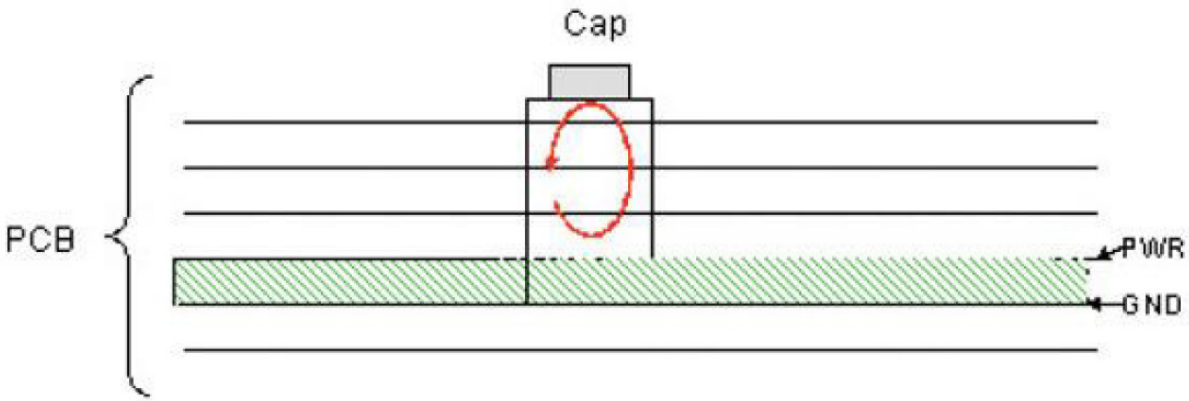
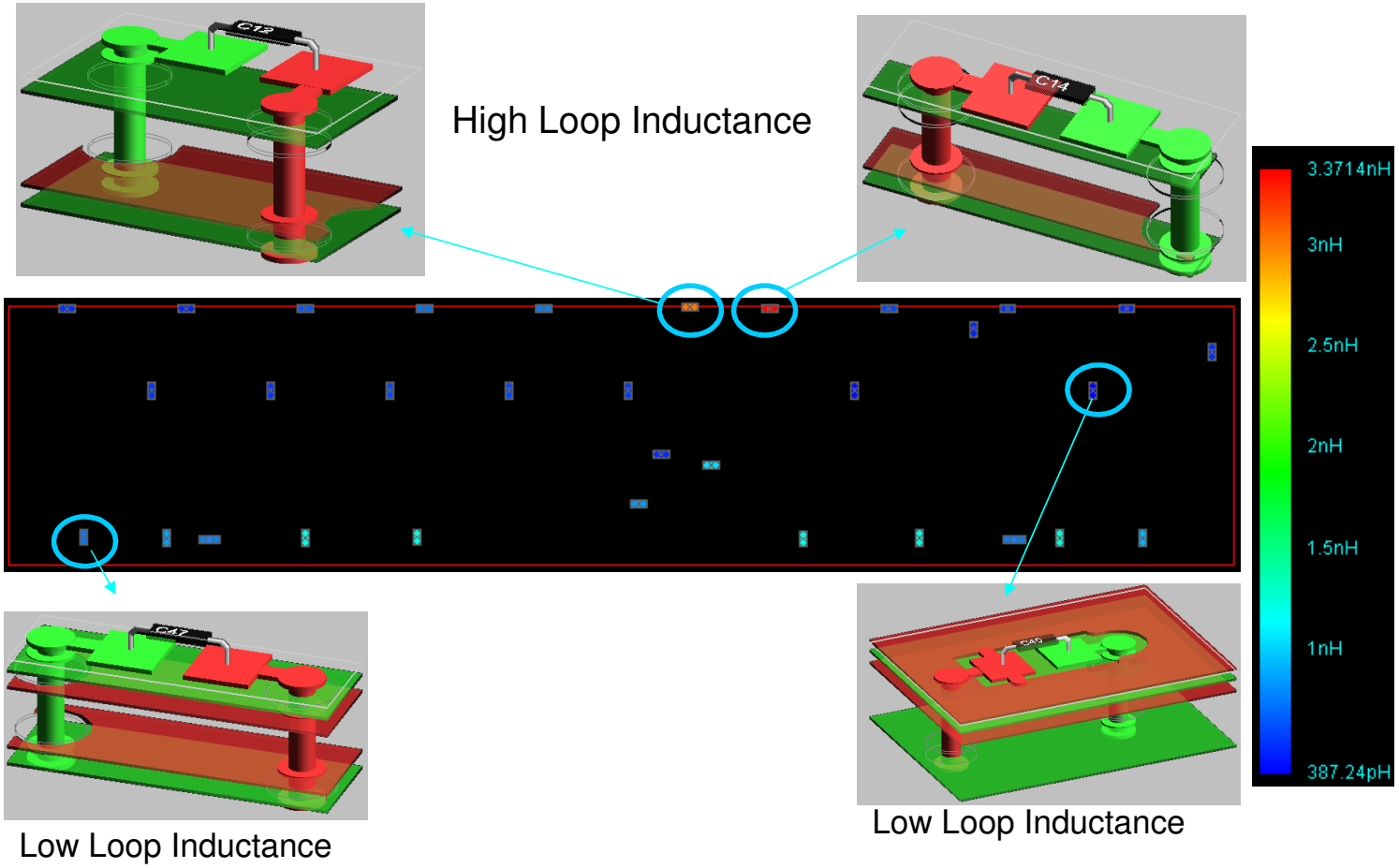


Figure 3. High inductance connection with capacitor mounted on top of board.

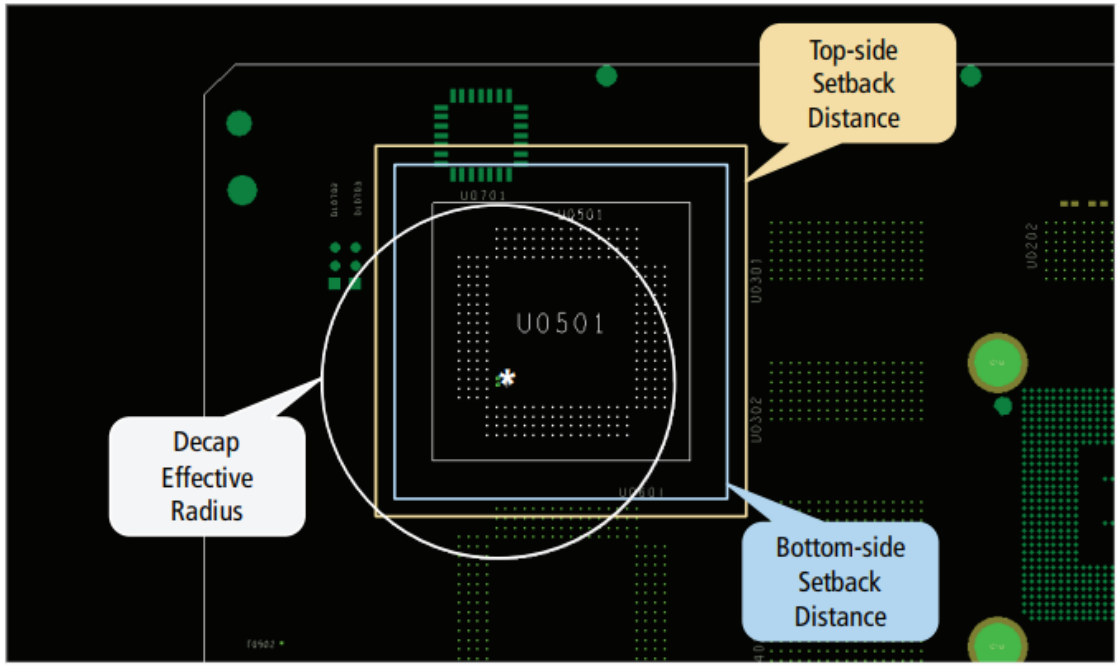
Don’t do this

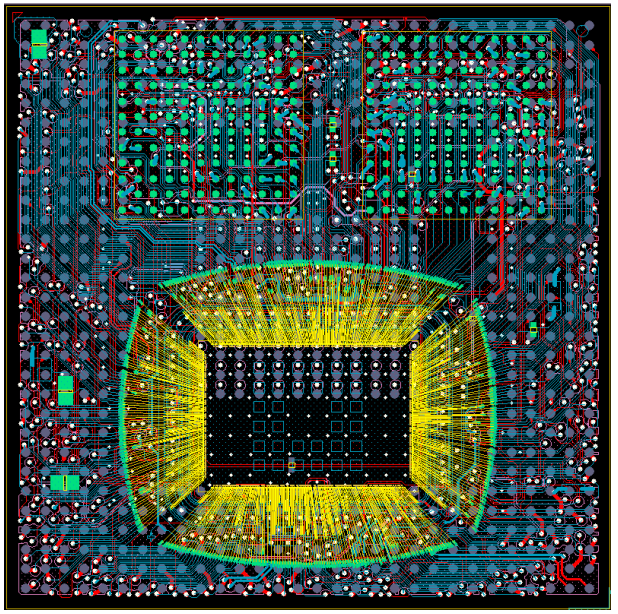
Loop Inductance



Smaller capacitors, effective at higher frequency, need to be placed closer to the device to be effective.

De-Caps are often placed inside the IC package design





Return Path Vias

John Carney
Cadence AE

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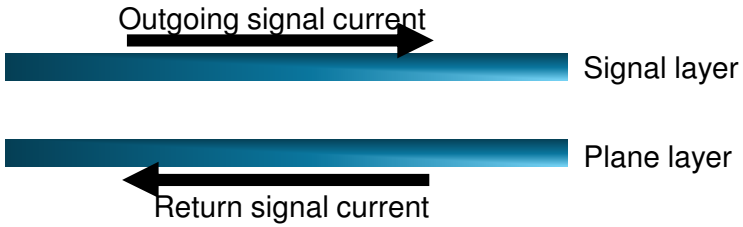
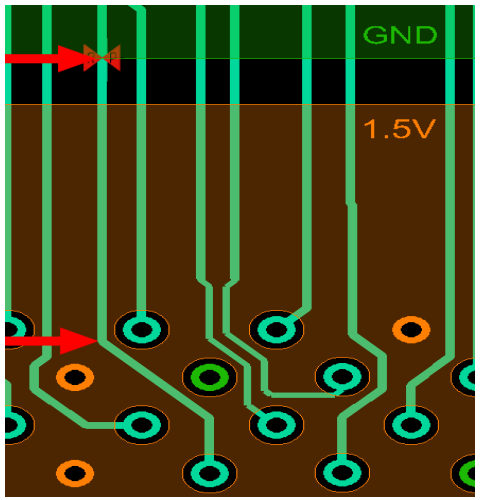
Understanding Return Path

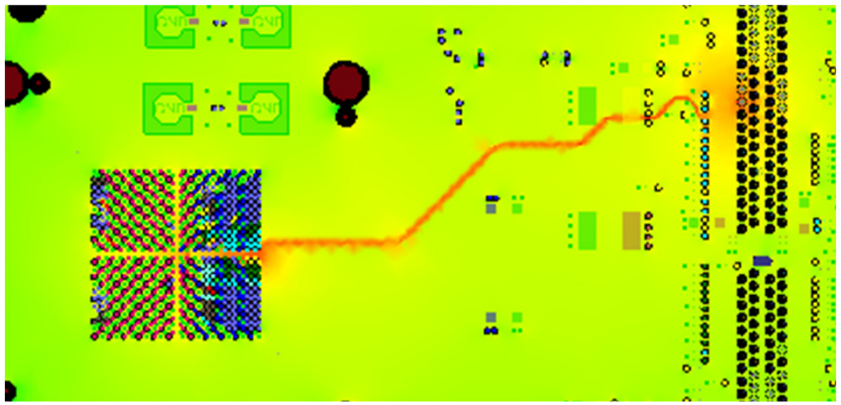
- Currents must always return to their source.
- Return current will return to their source along the path of the least impedance.

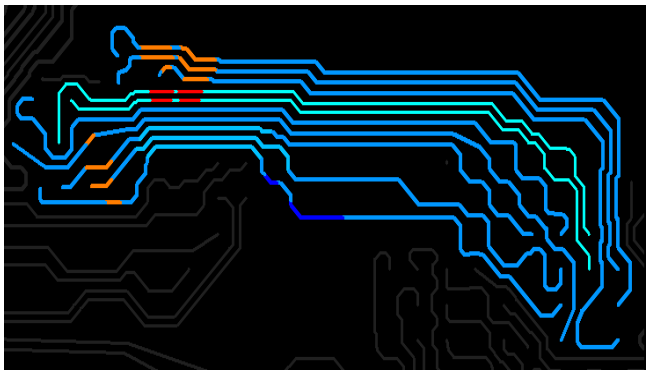


The return currents must complete the loop



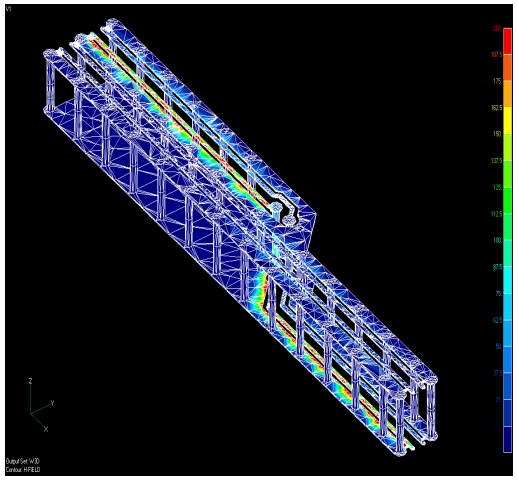
Void Crossing Incorrect Reference Plane

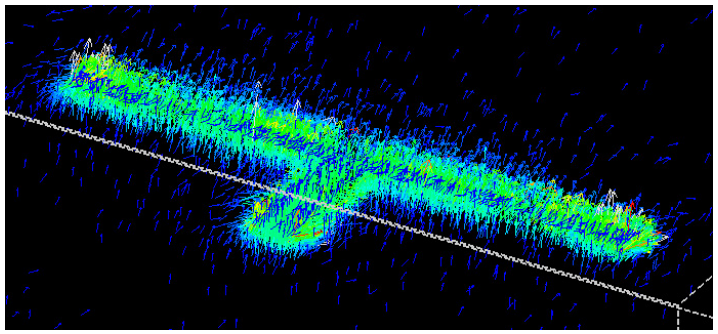


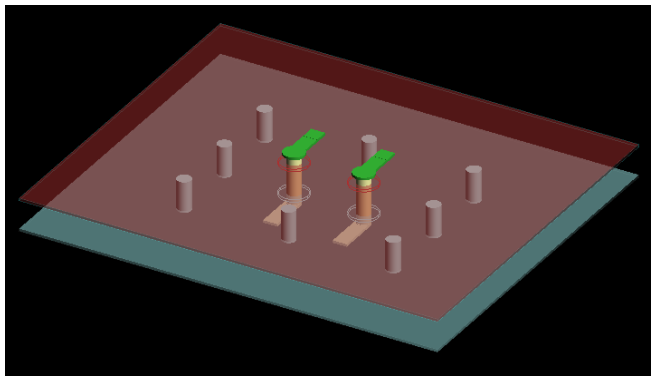


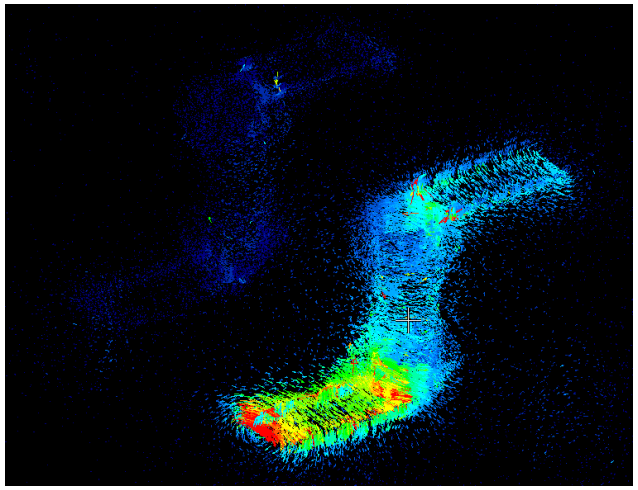
Electromagnetic fields

- The signal or energy transferred is propagated as an electromagnetic wave.



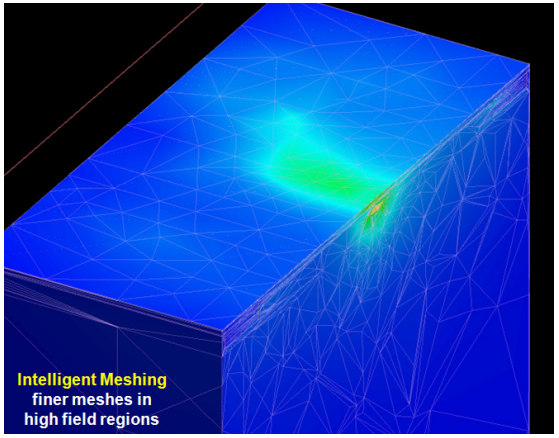


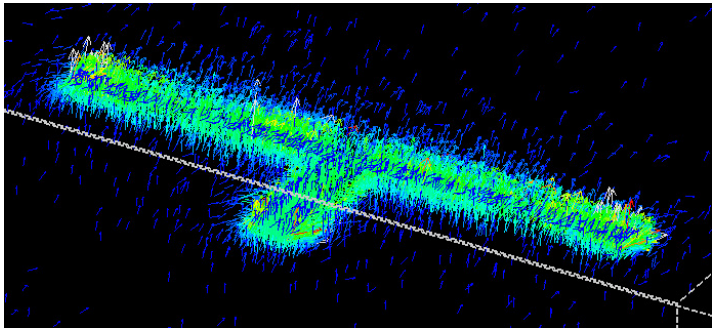


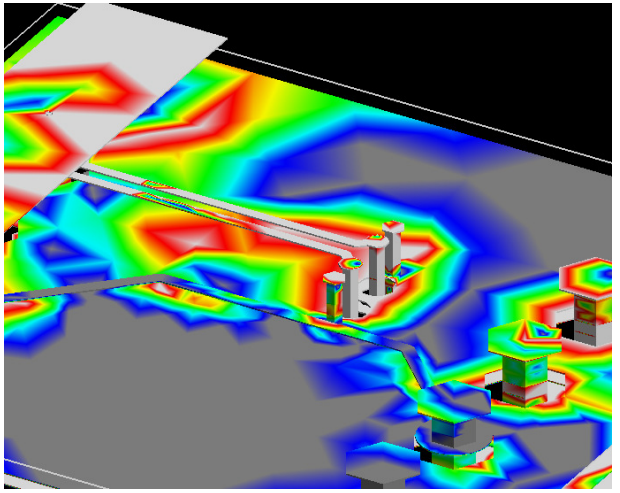


Electromagnetic fields

- Electric fields on PC boards exist between any two conductors, such as a Microstrip over a return plane.
- Current flows in loops and must have an uninterrupted path back to the source.
- If the return path is broken, the electromagnetic field
  - Will “latch on” to the next closest metal and will not likely be the return path you want.
  - Will “leak” throughout the dielectric and cause common mode currents to flow all over the board, as well as cause cross-coupling of clocks or other high speed signals.

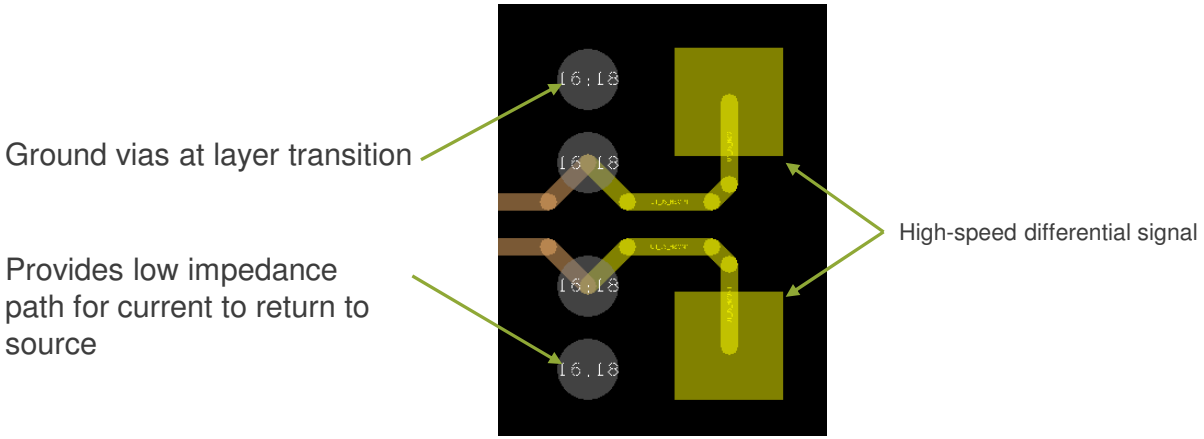






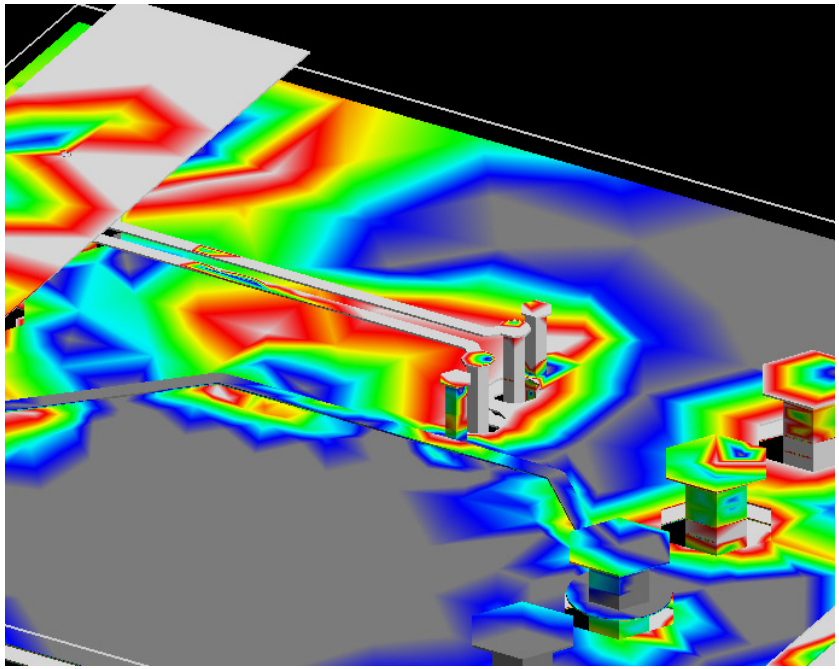
Providing Return Path

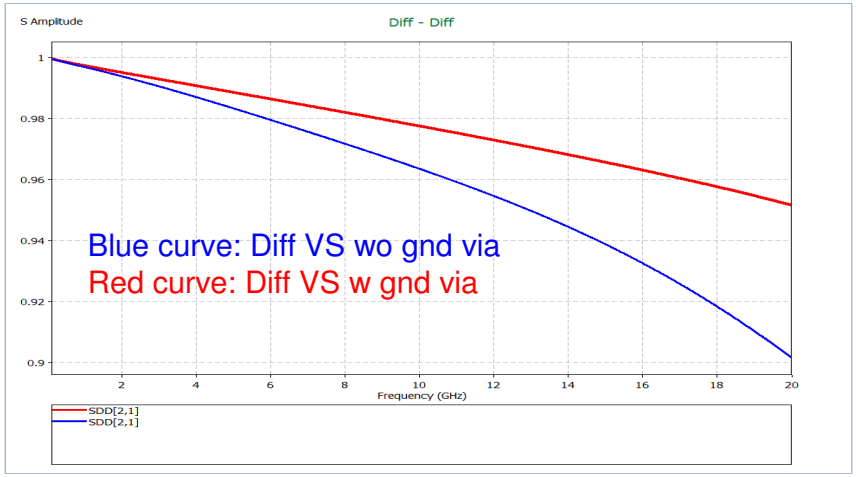
- For system clocks and high speed I/O interfaces such as **DDR, PCI Express®, USB, SATA**, etc. - if via transition is necessary, it is required to place return path via(s) as close as possible to the location of transition
- Without proper placement of return path vias, the return current must find its own way. Results in the current spreading over a large area, which greatly increases the possibility of cross contamination with other signal currents creating a loss of SI



Return path vias

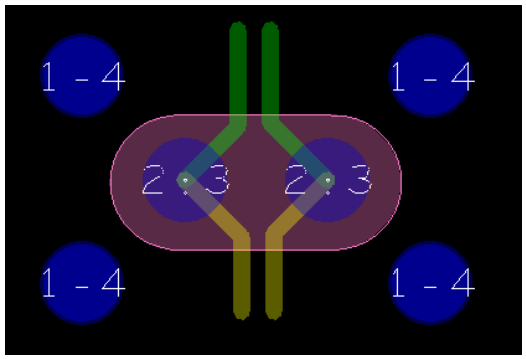
- Return path vias limit the amount of area the energy can disperse into.
- At multi Ghz these return path vias are typically tuned and driven by simulation.
- Insertion loss (the amount of energy lost in the channel) is also better with return Path vias due to lower impedance

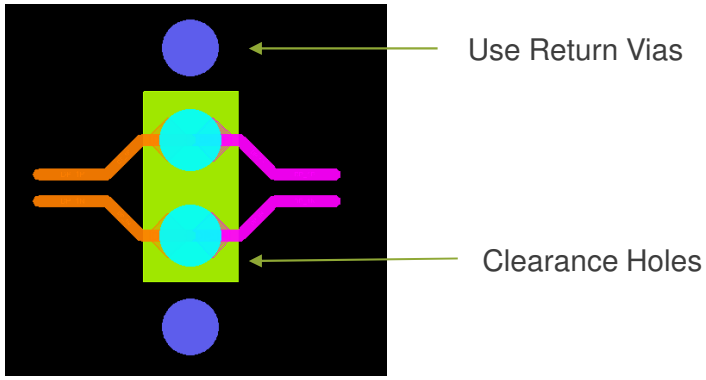




Most Common Guidelines for High-Speed Via Transitions

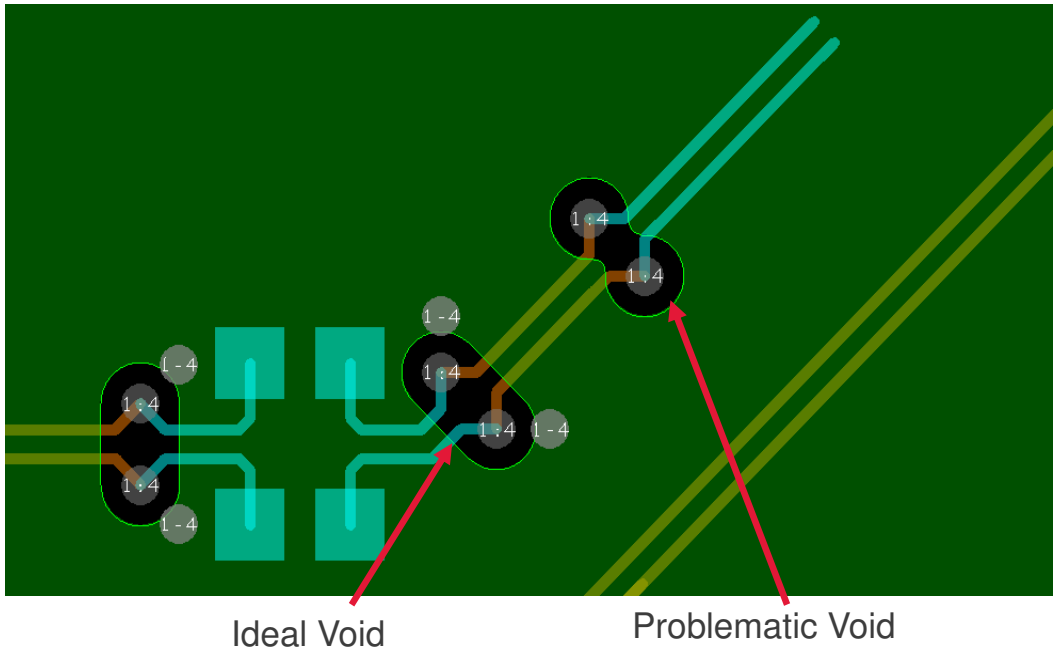
- Use closely coupled impedance matched differential vias
- Use return vias in close proximity to signal vias
- Use large clearance hole (anti-pad) in the via stack



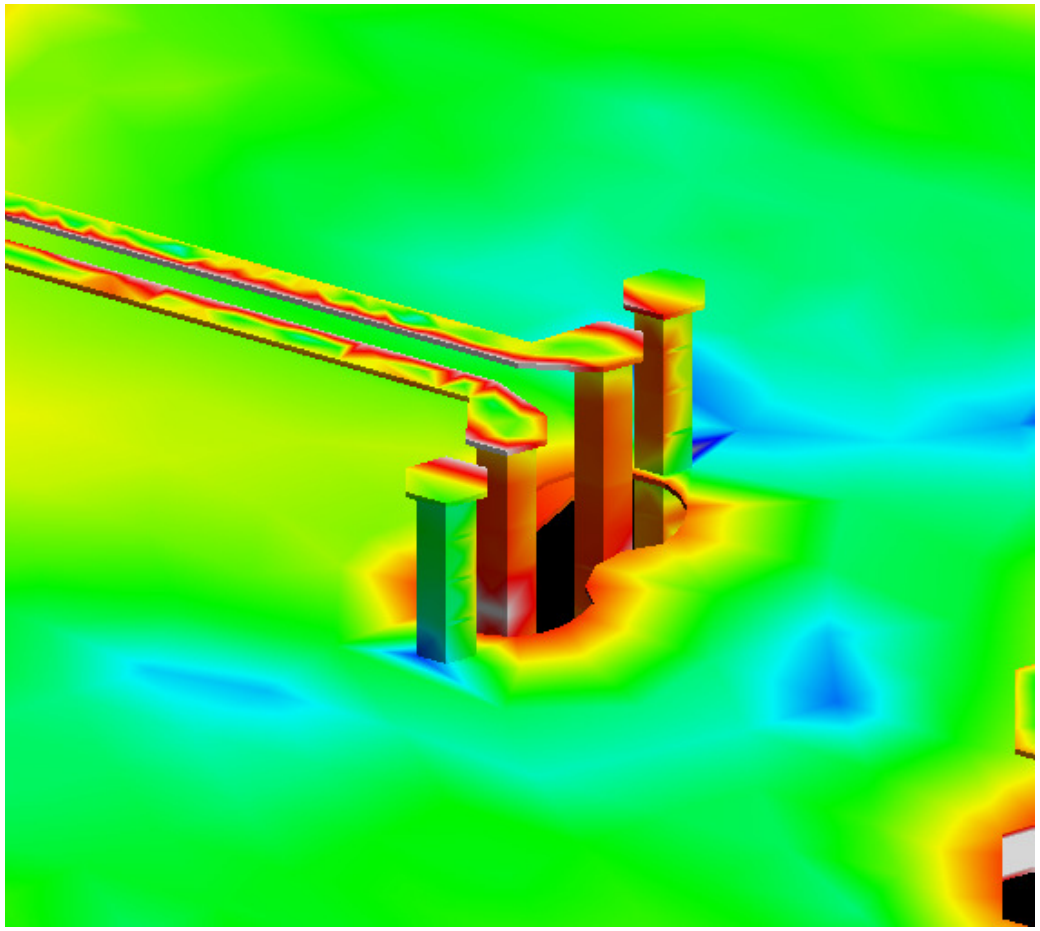


Diff Pair Via Voiding

- The shape of the void is important
- An oblong instead of a void created by the via/shape clearance is highly preferable at high speeds



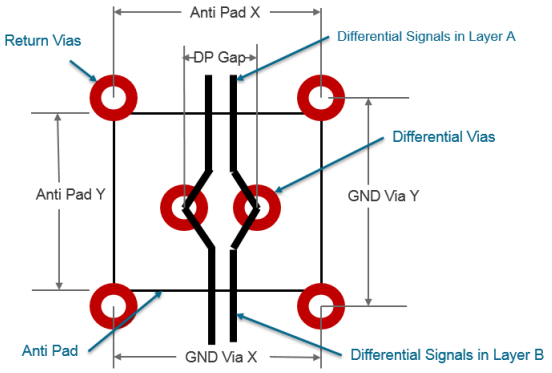
Differential Vias with bad void

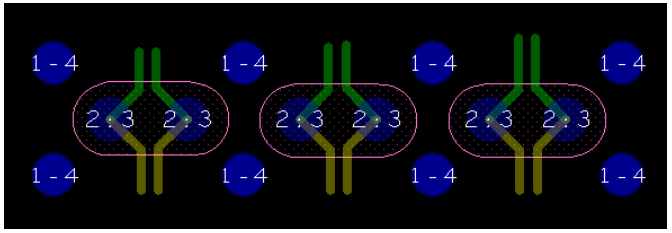


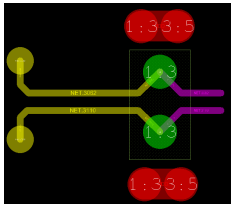
Increased EM coupling to the plane due to the conductor closer to the signal vias

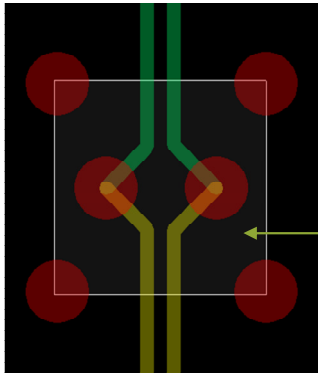
High Speed Via Structures

- SI engineers are getting more creative, which results in more complex requirements on:
  - Return path vias: type (thru, BB Stacked/Staggered), quantity, pattern, and proximity locations
  - Differential pair pad entry/exit (trace width, entry/exit pattern)
  - Void (layers, pad clearance, shape)

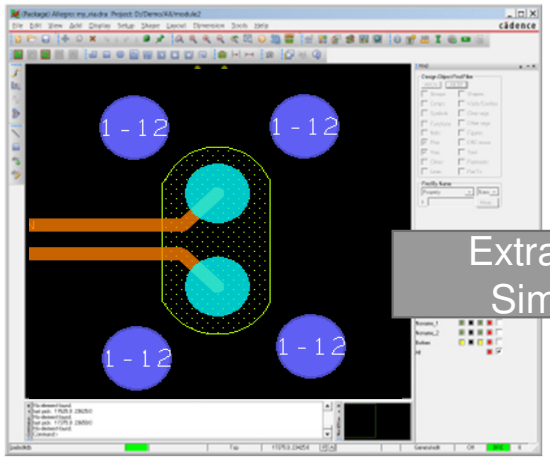




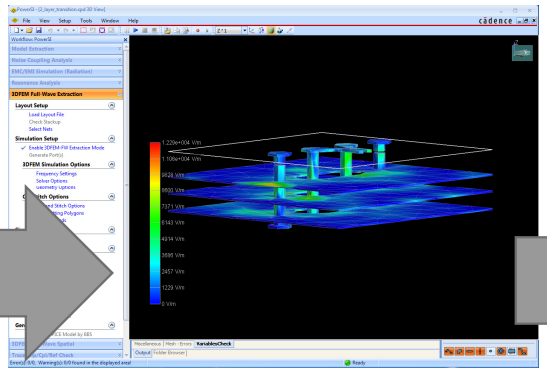




Simulation Driven, Optimized, Via Structures

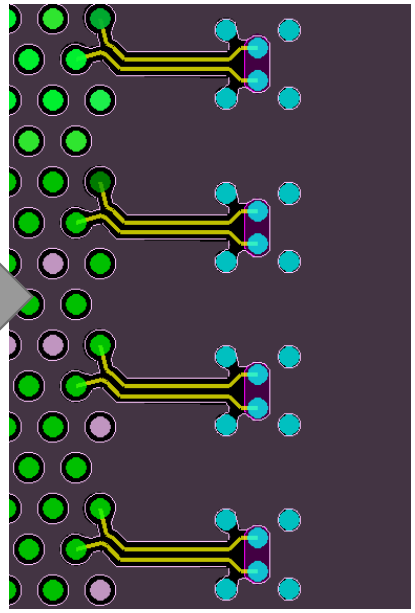


Extract and Simulate



Parametric 3D EM Simulations

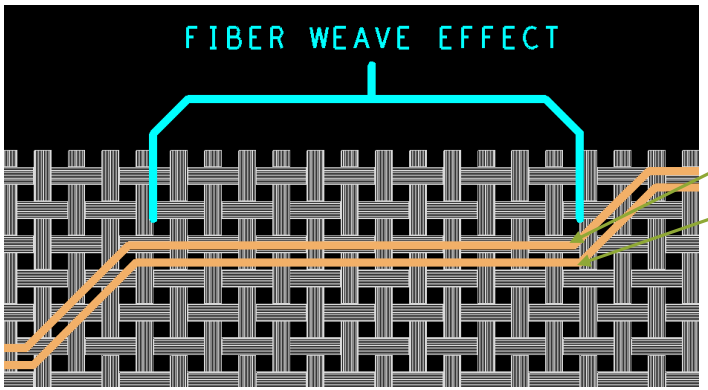
Via Structures



Fiber Weave

What is “Fiber Weave Effect”?

- When timing or phase skew caused by fiberglass reinforced dielectric substrate between two transmission lines of the same length happens
- Traces routed directly over the fiberglass weave will see a different Dielectric Constant than the traces that are routed over the voids in the weave where only epoxy resin is present.
- At high data rates, this dielectric constant mismatch can cause signal integrity issues when running these high speed signals parallel to the void areas of PCB fiberglass weave.



Trace running directly over glass fiber

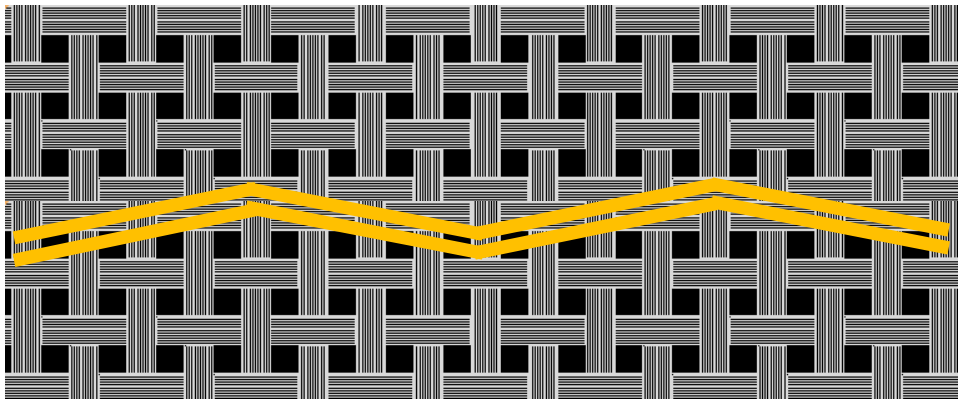
Trace running directly over epoxy

This results in a degraded differential signal as glass and epoxy have different permittivity's on PCBs.

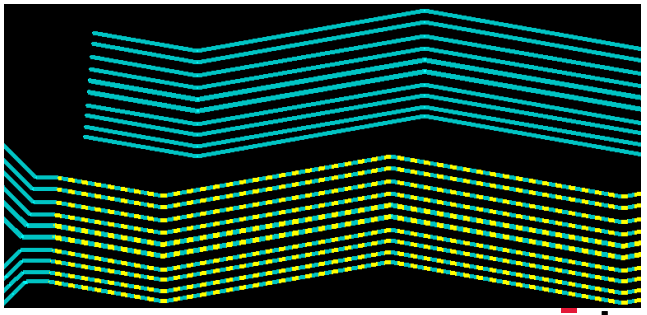
Typical Layout Routing Guideline

When routing for a considerable length, it is oftentimes recommended to do zigzag routing to mitigate the negative effects of fiber weave on high-speed differential signals by forcing the traces to be out of alignment with the fiber weave.

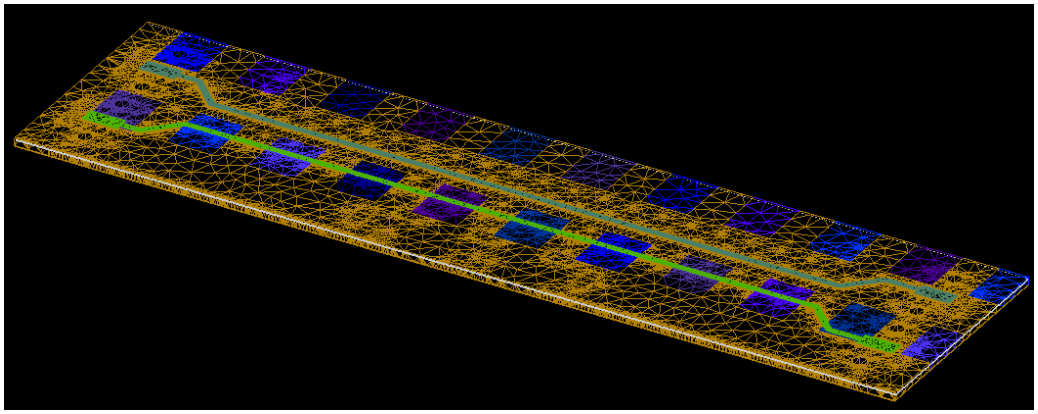
– Angle of zigzag can be 1-10 degrees to skew traces relative to weave. Typical value used is 10 degrees to sufficiently skew trace.



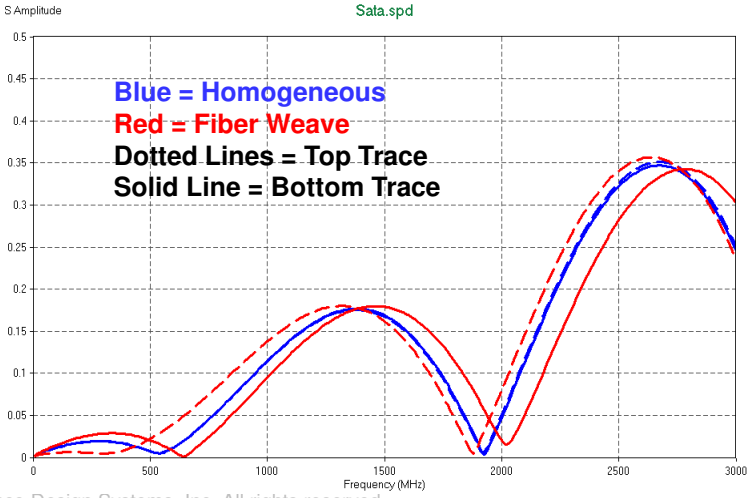
Typical for **>5 GT/s**, the fiber weave effect becomes significant when the trace alignment to weave is 4”or longer.

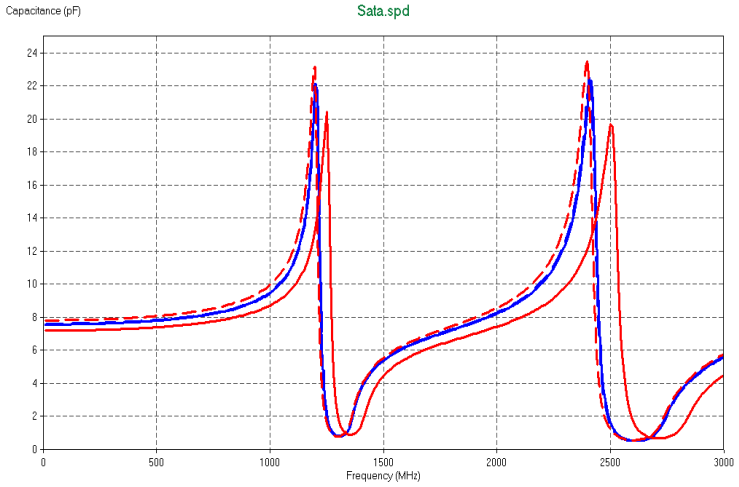


Fiber Weave Effects (sample case 1)

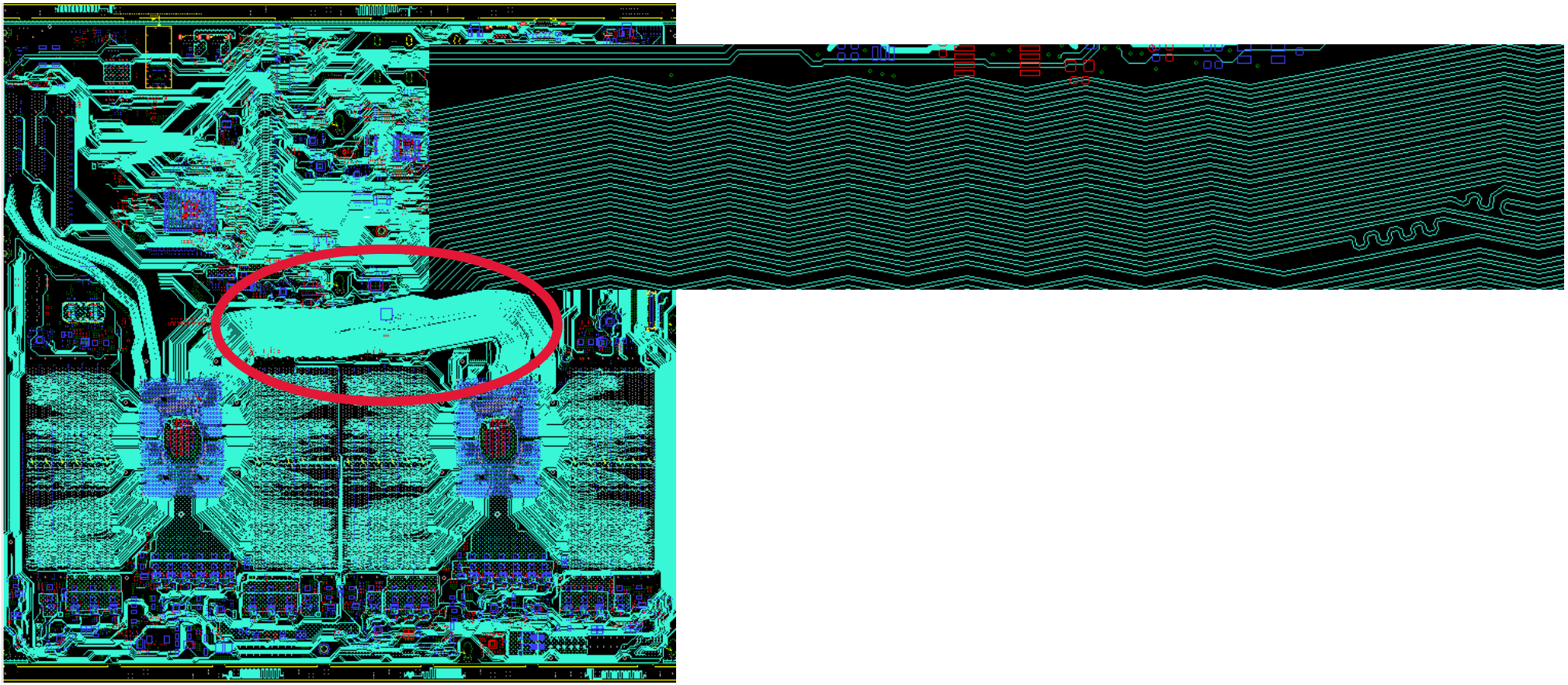


Top trace and bottom trace have different Amplitude(S), Capacitance(c), and Zc due to inhomogeneous materials created by fiber weave.





Fiber weave compensation example



3D Modeling of Fiber Weave Effect

Test Cases: Channel Simulation Results (3)

Homegeneous

```
        Characterization Data           = E:\Cadence\Products\PowerSI-
        Delay                           = 0.48856 ns
        Intra-Pair Skew                 = 0.38521 ps


Algorithmic Models:

        Rx Models                       = C:\Cadence\Sigrity2015\share
        Primary Tx Tx1 Models           = C:\Cadence\Sigrity2015\share

Jitter Inputs:

        Random Jitter                   =  1 %

Noise Inputs:

        Random Noise                    =  1 mV

Eye Contour Measurements:

        Eye Height                      = 552 mV
        Eye Jitter                      = 0.40 UI
        Eye Norm Jitter and Noise (NJN) = 0.81

BER Measurements:
```

With Fiber Weave

```
        Characterization Data           = E:\Cadence\Products\PowerSI-
        Delay                           = 0.482429 ns
        Intra-Pair Skew                 = 14.0522 ps


Algorithmic Models:

        Rx Models                       = C:\Cadence\Sigrity2015\share
        Primary Tx Tx1 Models           = C:\Cadence\Sigrity2015\share

Jitter Inputs:

        Random Jitter                   =  1 %

Noise Inputs:

        Random Noise                    =  1 mV

Eye Contour Measurements:

        Eye Height                      = 564 mV
        Eye Jitter                      = 0.34 UI
        Eye Norm Jitter and Noise (NJN) = 0.78

BER Measurements:
```

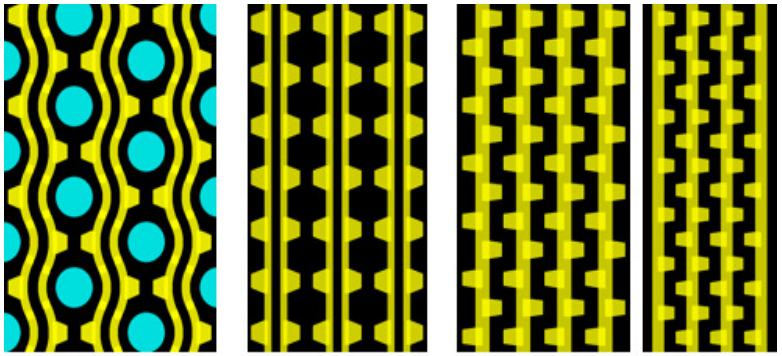
Tabbed Routing

What is “Tabbed Routing”?

- New routing method in which trapezoidal shapes called tabs are added to parallel traces

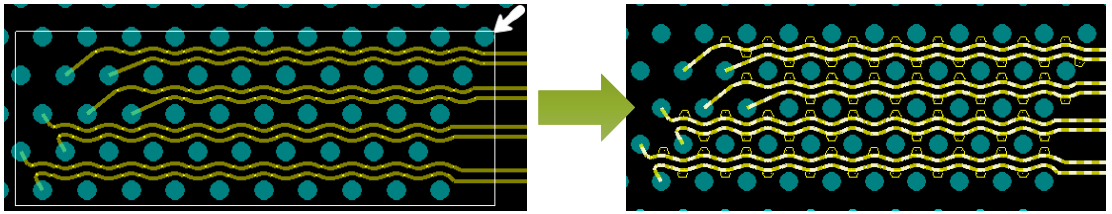
Benefits

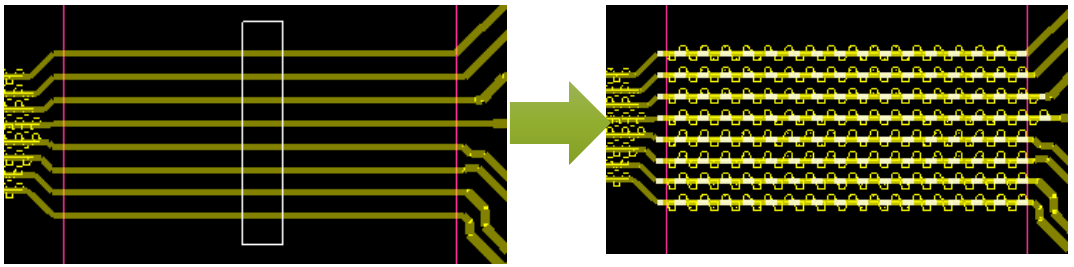
- Impedance control in pin field/breakout region
- Manage crosstalk in open field region
- Allows for longer trace lengths and more compressed routing

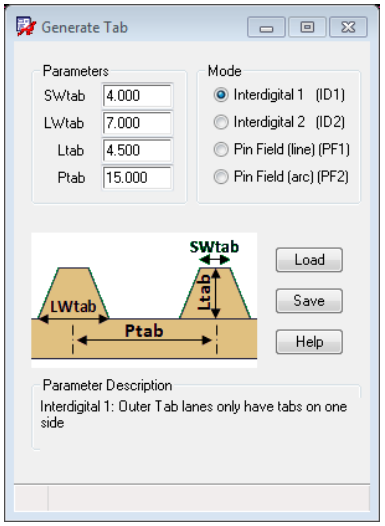


Layout Tips and Techniques

- Tab applications and parameters are typically provided by the IC vendor.







Tabbed Routing Simulations

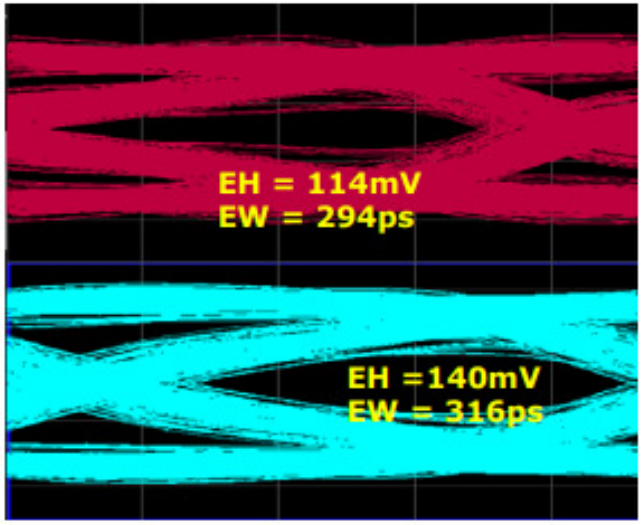


Figure 9: Eye diagram comparison. Red: normal microstrip wiring. Blue: tabbed line wiring.

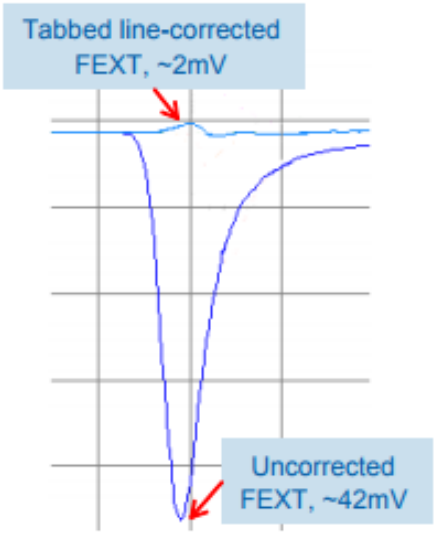
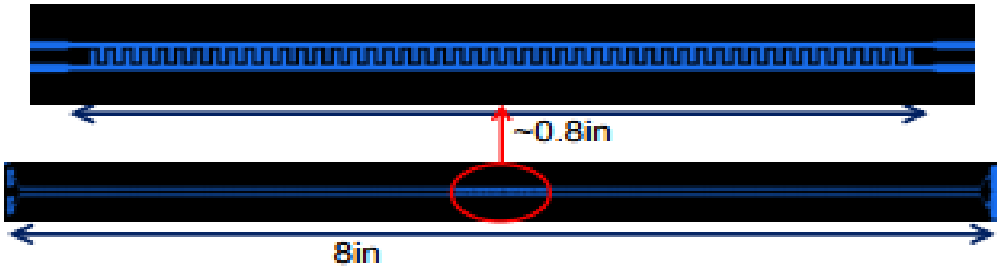
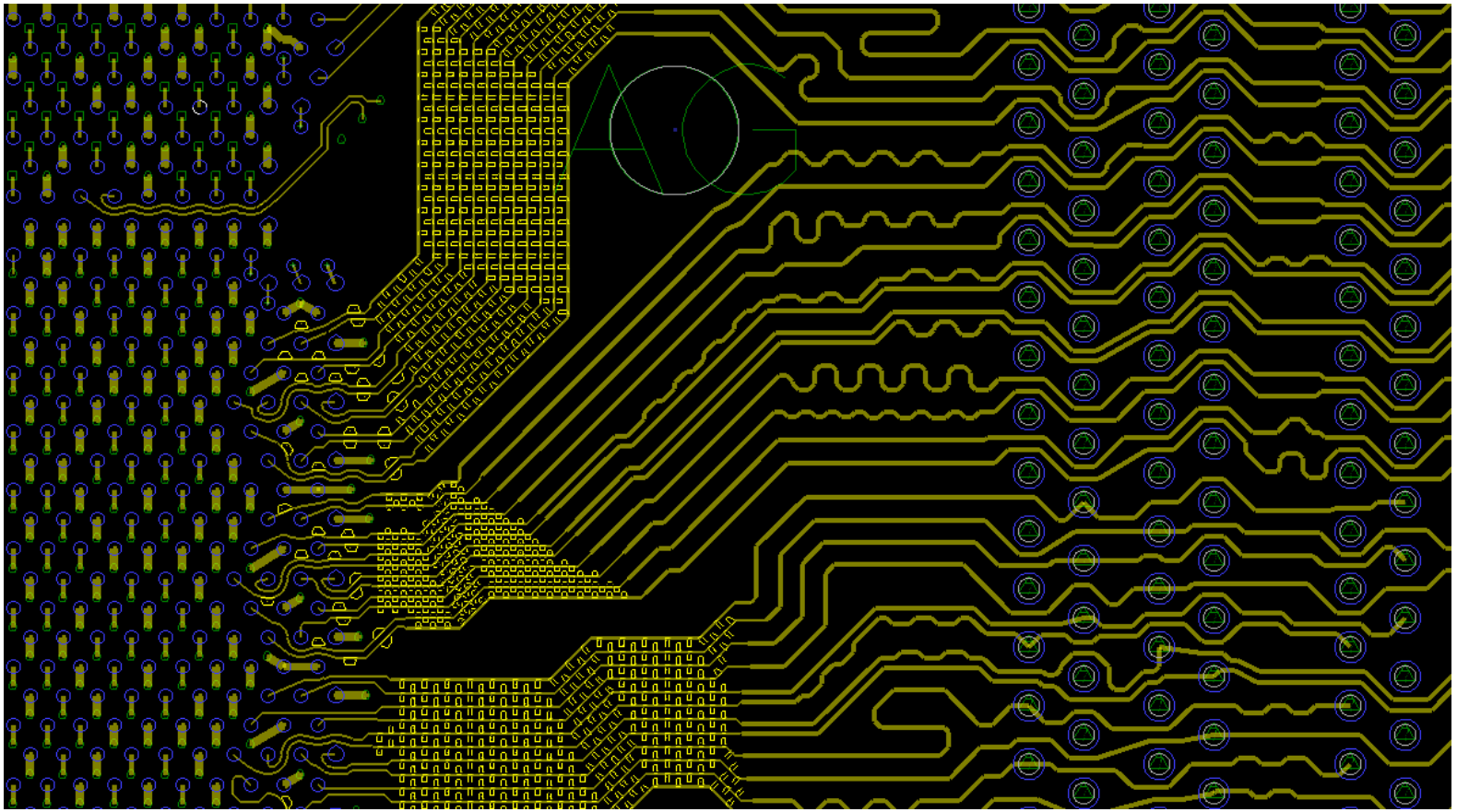


Figure 3: Measurement results showing net FEXT amplitude reduction due to Type (II) tabbed line compensation

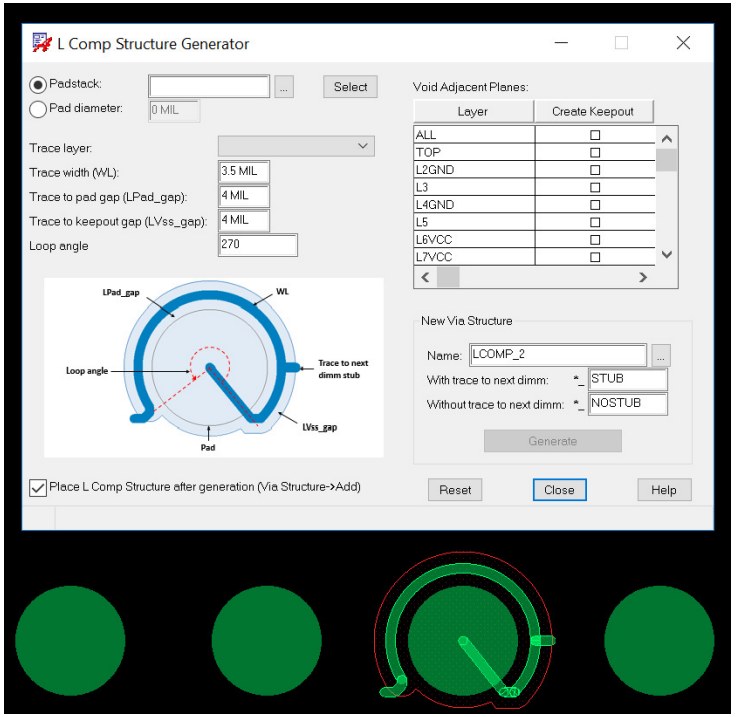


Tabbed Routing Example



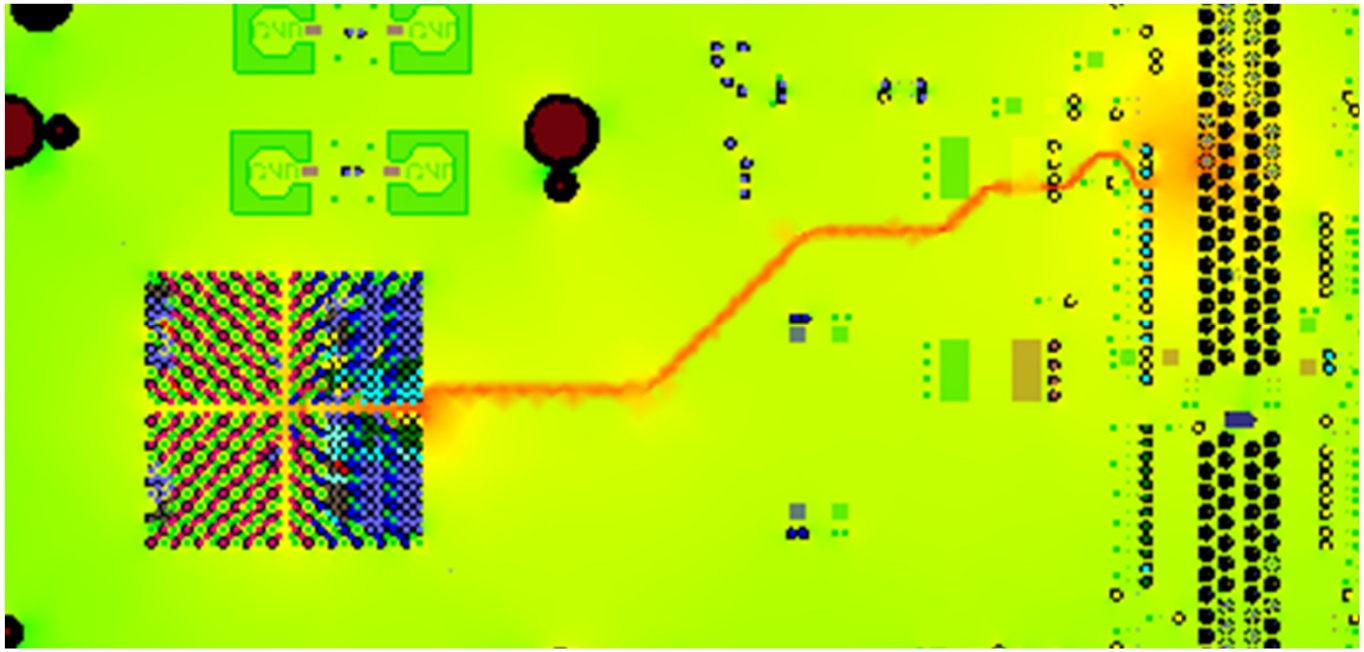
Inductance (L) Compensation Structures

- Recent advances in high-speed design have required complex structures for proper performance
- Adding inductive structures helps counter component capacitance



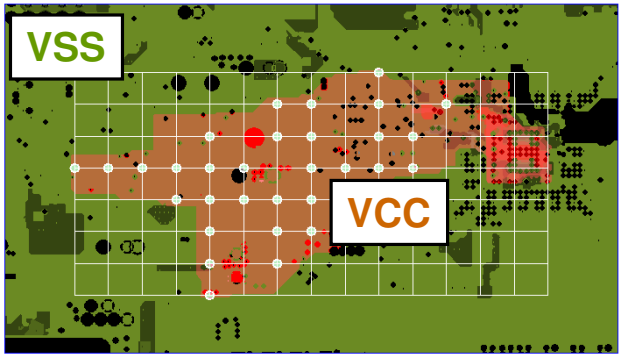
Extra slides

Return path analysis

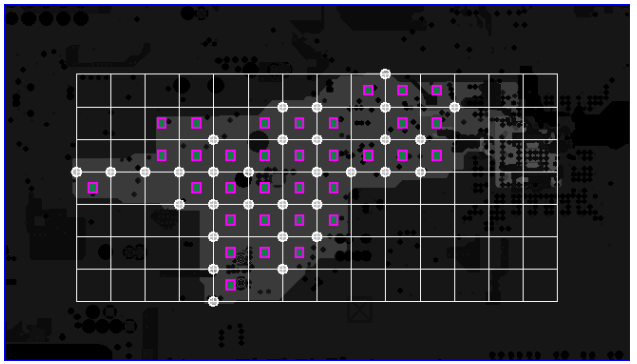


How to Reduce PDN Emissions

- Reduce impedance throughout the entire PDN
  - reducing device impedance tends to reduce emissions, but is not guaranteed to do so
    - especially for high device decap count
  - reducing PDN impedance assures reduced emissions
  - new capacitors are usually required

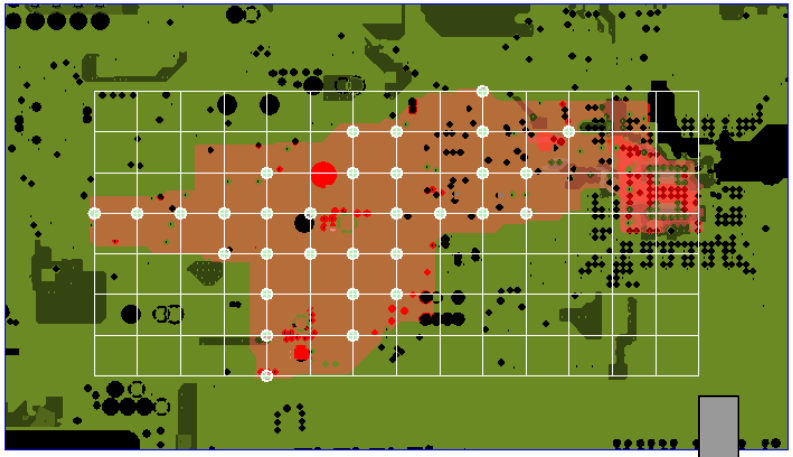


Impedance observation locations

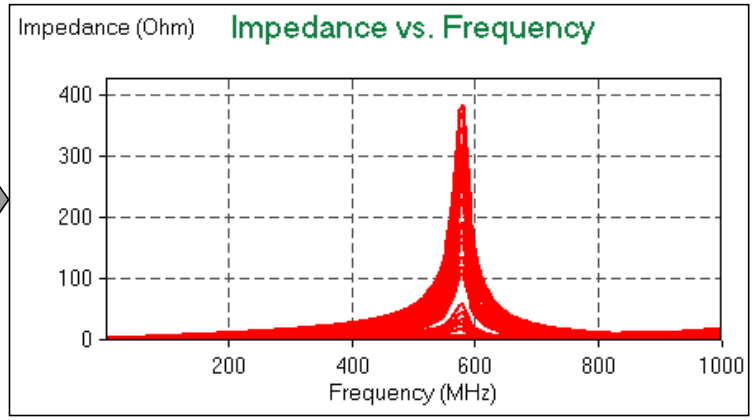


New emicap candidate locations

PDN Impedance Sample Locations



All 31 PDN impedances have a 580MHz peak.



Consider 31 impedances across the power/ground cavity at all X-Y gridline intersections that lie with the cavity boundary.

NOTE: Not all gridline intersection impedances are used because the point is not within the PDN parallel plate cavity.

EMI Optimization Setup

Objective

Determine number of capacitors, types, and locations to improve EMI radiation.

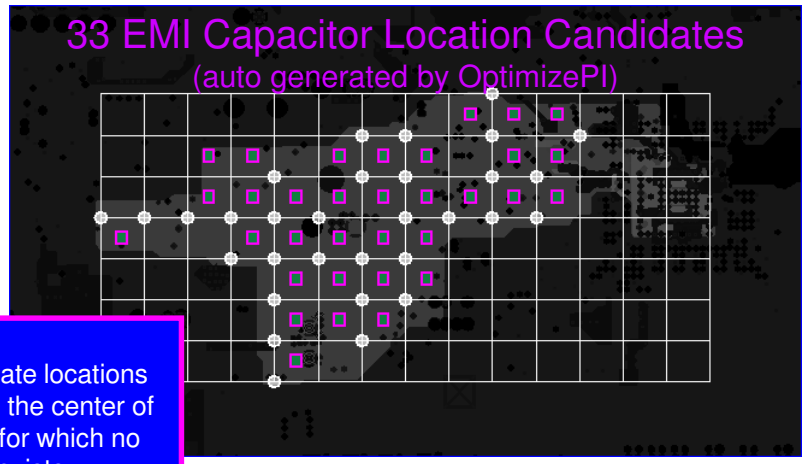
1

Optimization Objective
Best Performance vs. Number of Capacitors

2

Optimization Frequency

Starting Frequency	Ending Frequency
10MHz	**1GHz**



NOTE:
Emicap candidate locations are selected at the center of grid cell areas for which no capacitor now exists.

5 Capacitor Type

3

Cnom(nF)	Size
10	0402
22	0402
33	0402
47	0402
100	0402

4 Limit Number of Capacitors to 5

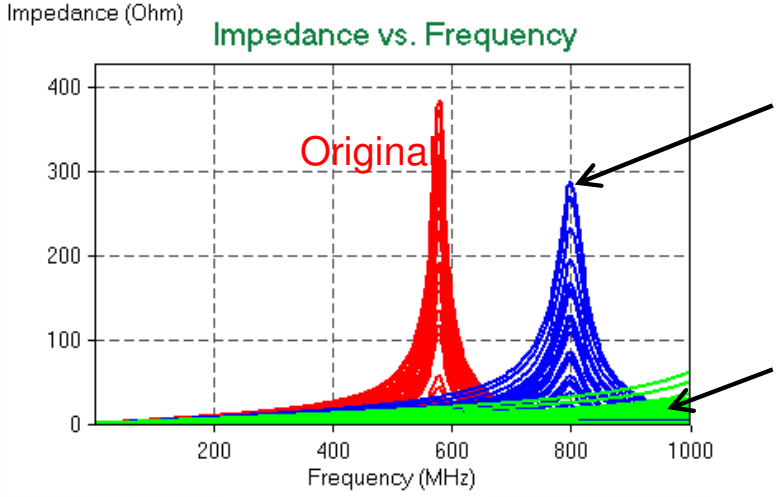
Optimization Range

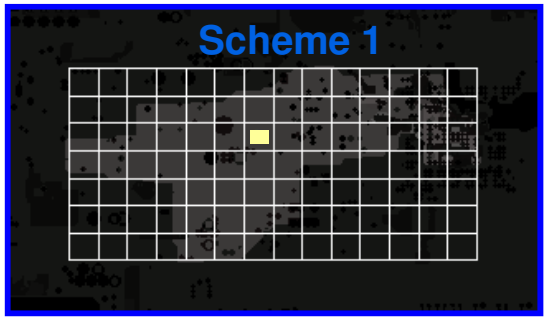
Optimization Range	Min	Max
Best Performance vs. Number of Capacitors	**1**	5

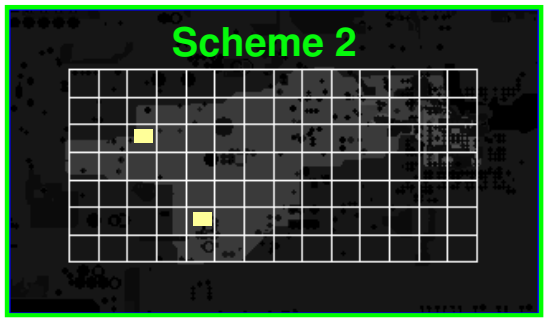
EMI Optimization Result

Impedance at all PDN locations

Scheme ID	Number
Original Scheme	0
Scheme 1	1
Scheme 2	2
Scheme 3	3
Scheme 4	4
Scheme 5	5



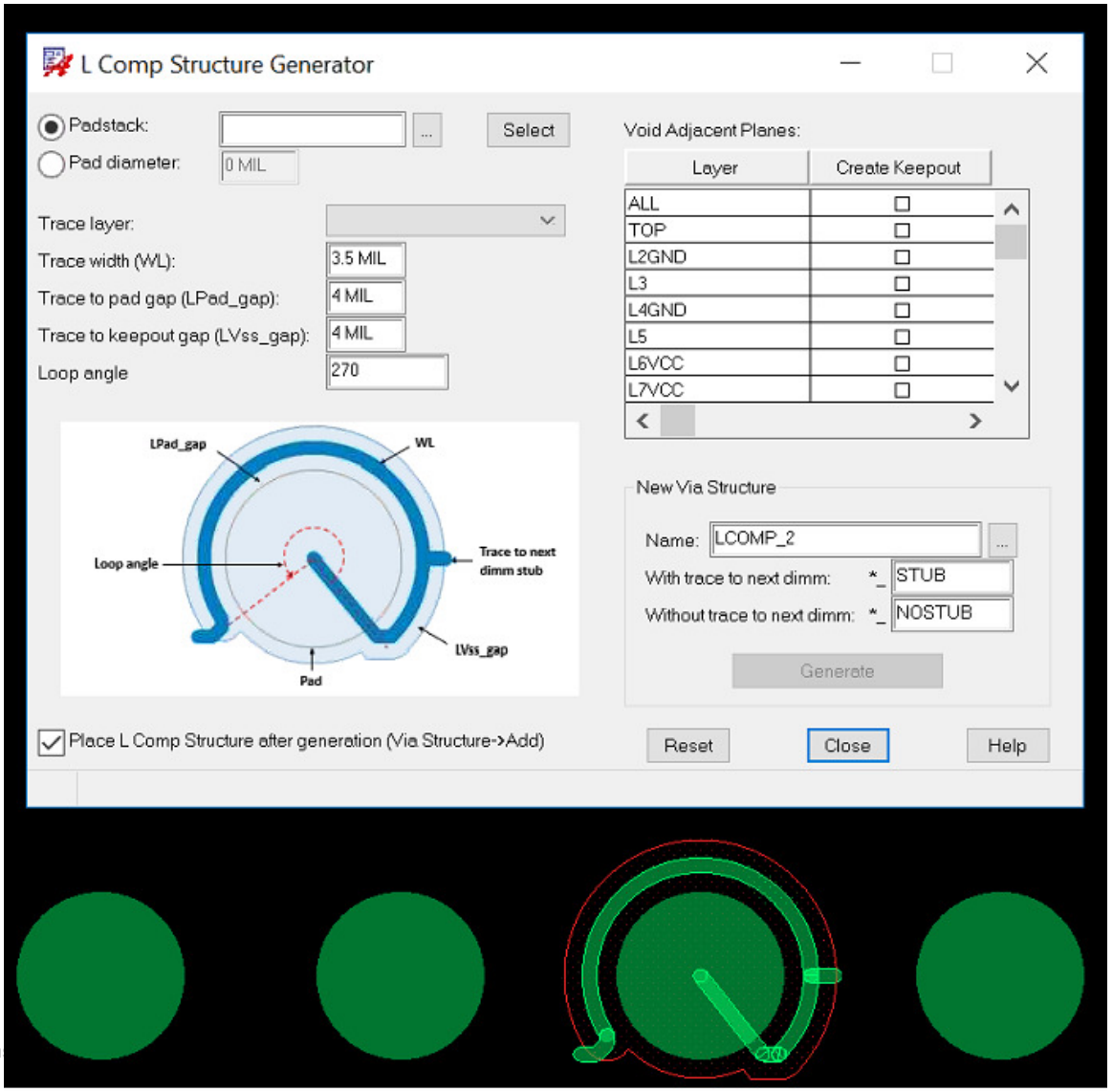




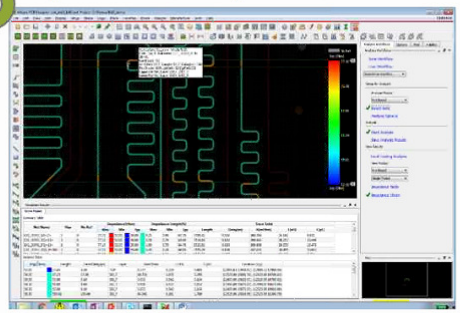
Scheme 2: OptimizePI predicts adding 100nF at these two locations will significantly improve power plane impedance at high frequency.

We know that reduced PDN impedance implies reduced emissions.

NOTE: Neither of the capacitors from the optimal 2-emicap scheme is in the same location as the 1-emicap scheme. This contrasts with iterative manual schemes to eliminate resonances.



1 Impedance Analysis and Vision



Analysis data on canvas and in tables
Cross-probe, zoom into problem areas

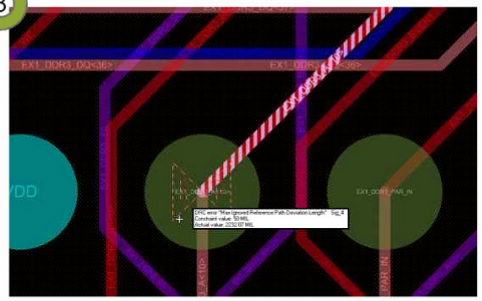
Quickly identify nets that are out of spec
Sliders on scale allow for filtering of view

2 Coupling Analysis and Vision

View victim and aggressor
nets on canvas

Quickly identify nets that are coupled
Sliders on scale allow for filtering of view

3 Return Path DRC



Signal not next to
required Ground Plane

Identify critical nets without a
reference plane quickly
Above or below or both

Mutual Inductance

Understanding Inductance in the Real-World | Interference Technology

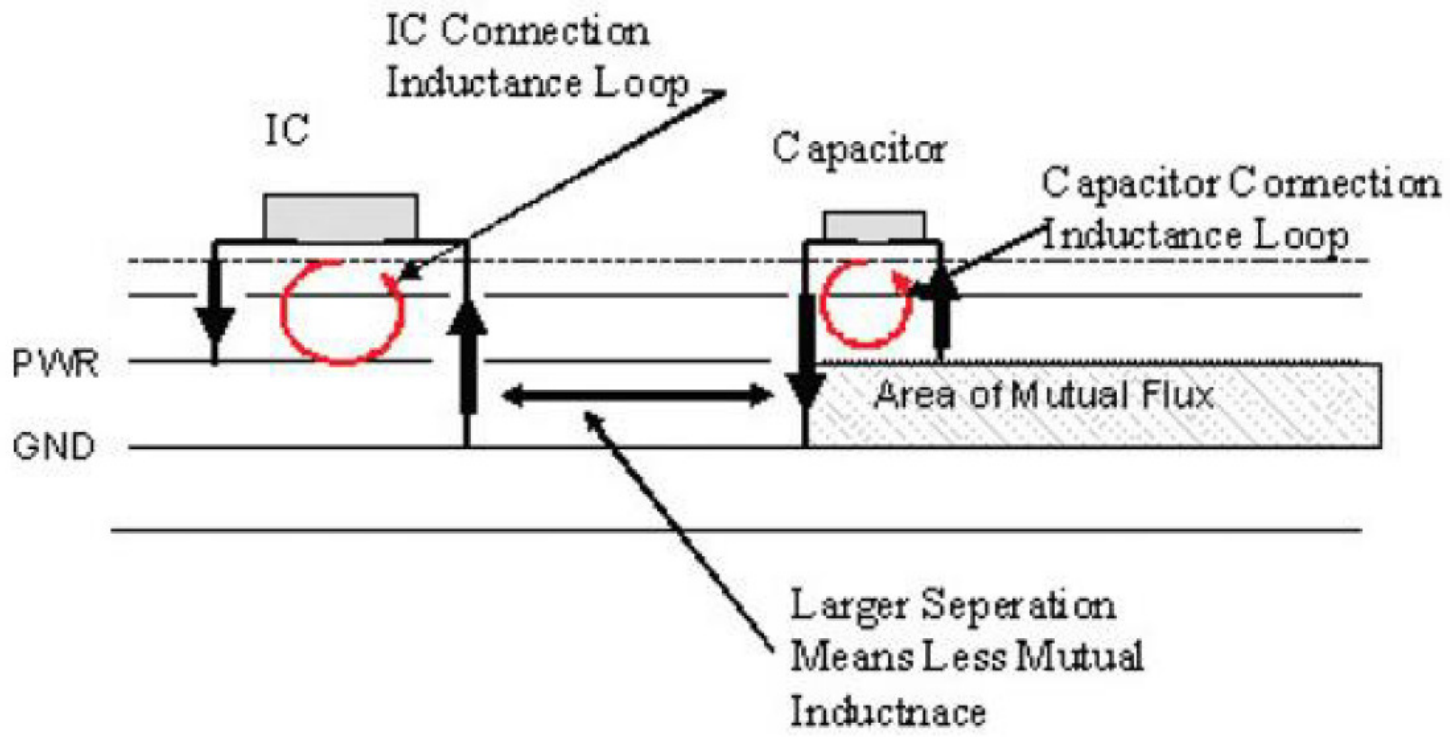
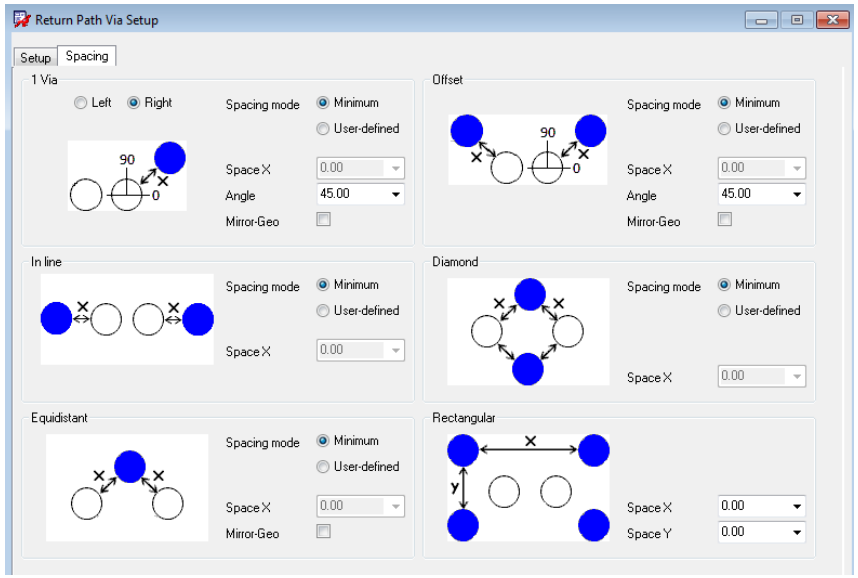


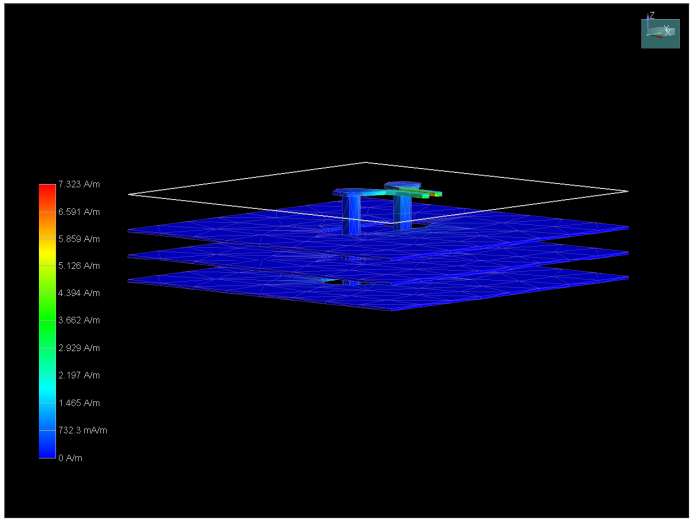
Figure 6. Mutual inductance between decoupling capacitor and IC.

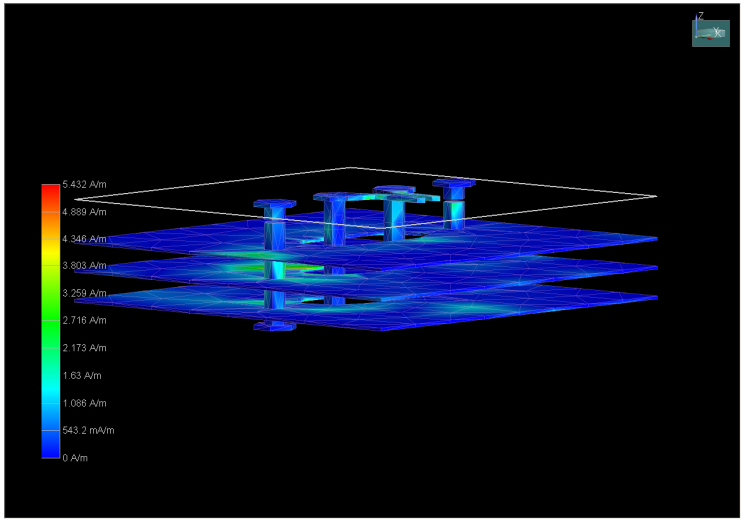
Return Path Vias



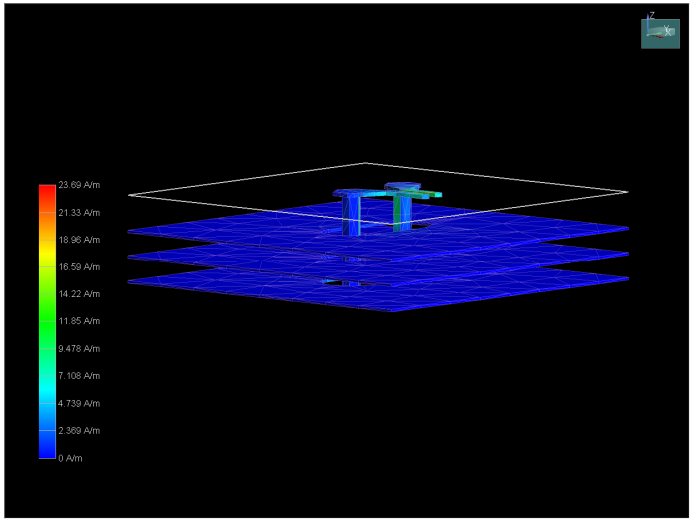
Differential and Single Ended
Parametric using design guidelines
Most popular common patterns
Not simulation driven
Show video of them being added and moved

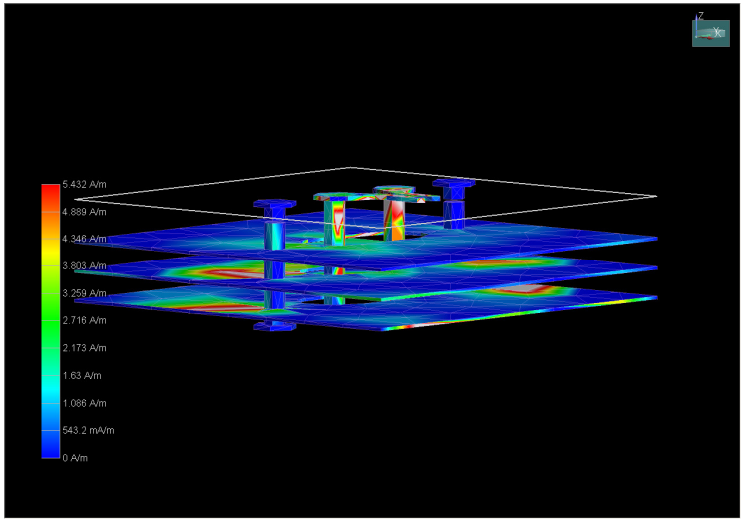
H Field @1GHz



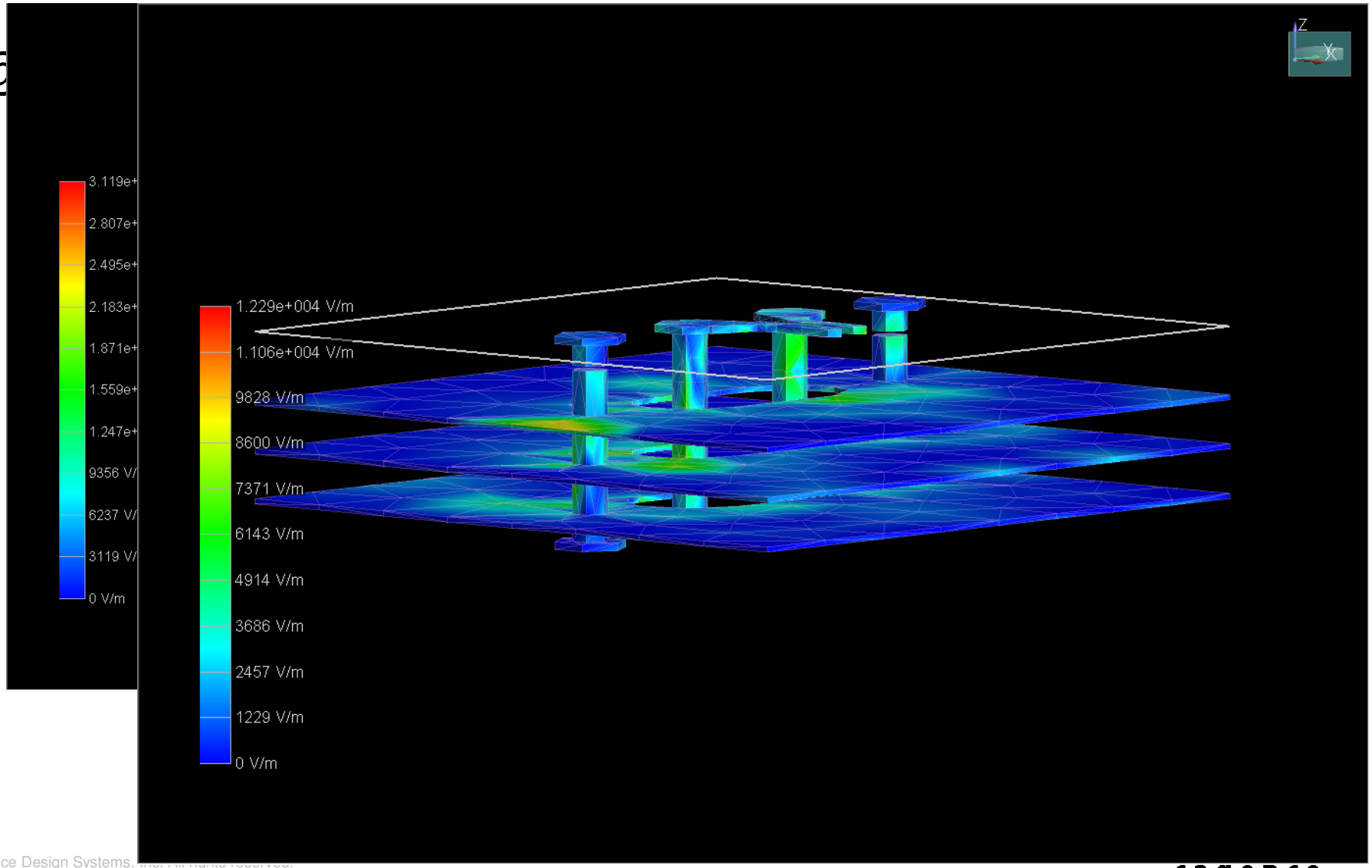


J Field @1GHz

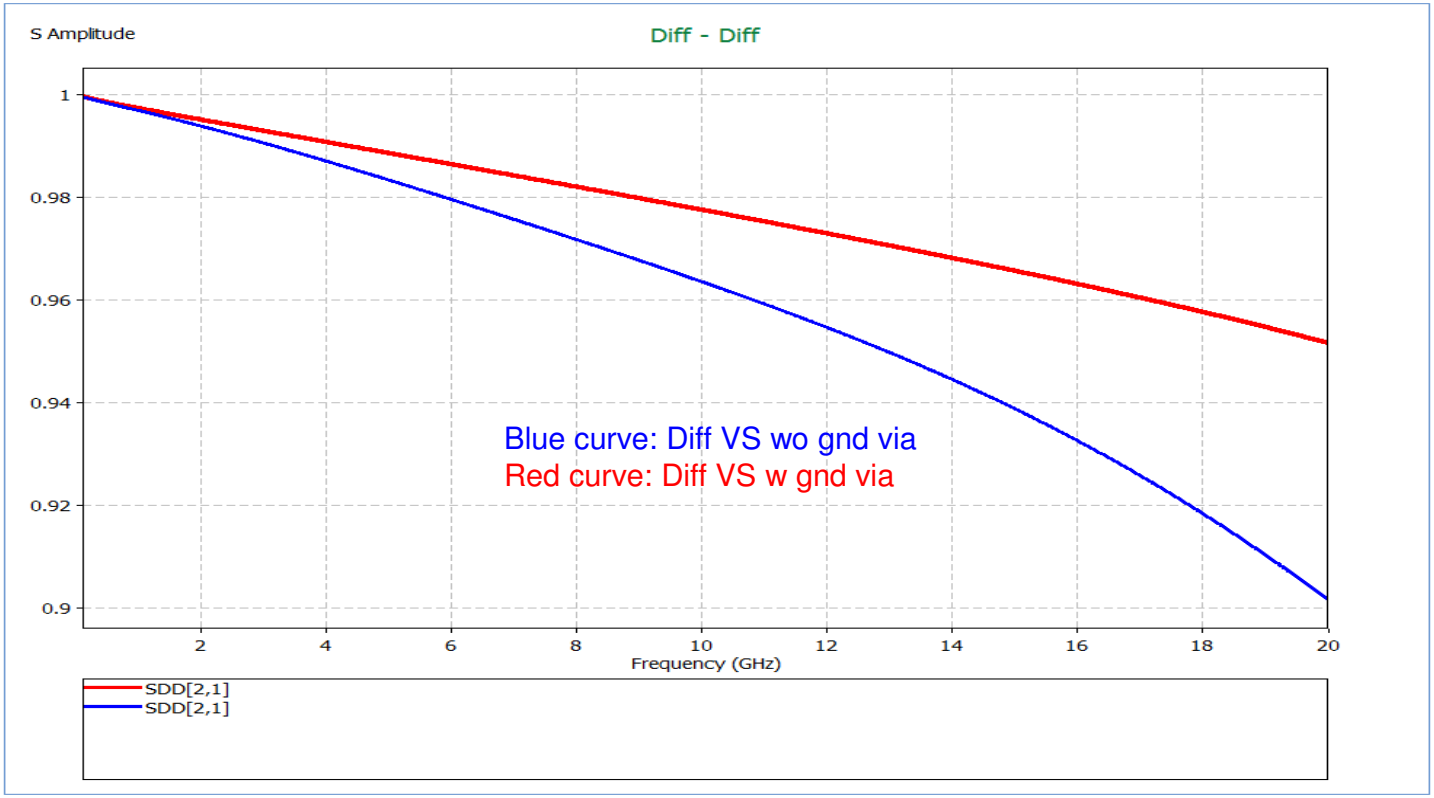


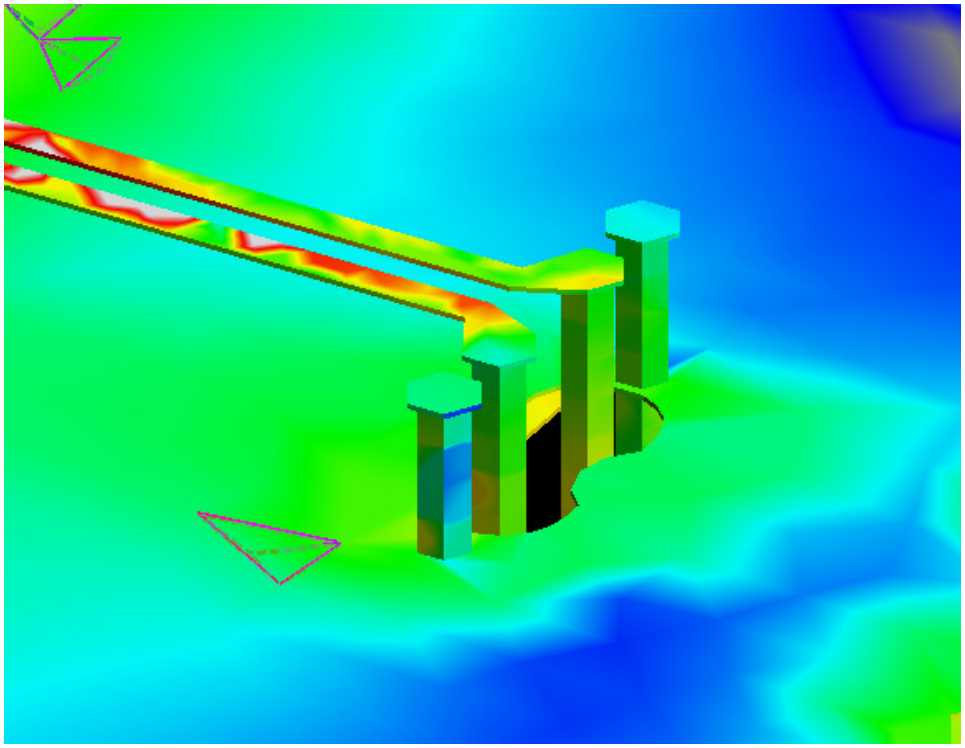


E Field @



Differential Insertion Loss





What to use for via current?

- The cross-sectional area of a via should have at least the same cross-sectional area as the conductor or be larger than the conductor coming into it.

- For plating thickness of 1mil, the cross-sectional area of a via of size:
  - *10mil* = $\frac{\pi*10^2}{4} - \frac{\pi*8^2}{4}$ = *28.27mil²*
  - *12mil* = $\frac{\pi*12^2}{4} - \frac{\pi*10^2}{4}$ = *34.56mil²*
  - *16mil* = $\frac{\pi*16^2}{4} - \frac{\pi*14^2}{4}$ = *47.12mil²*
  - *20mil* = $\frac{\pi*20^2}{4} - \frac{\pi*18^2}{4}$ = *59.69mil²*
  - *30mil* = $\frac{\pi*30^2}{4} - \frac{\pi*28^2}{4}$ = *91.11mil²*

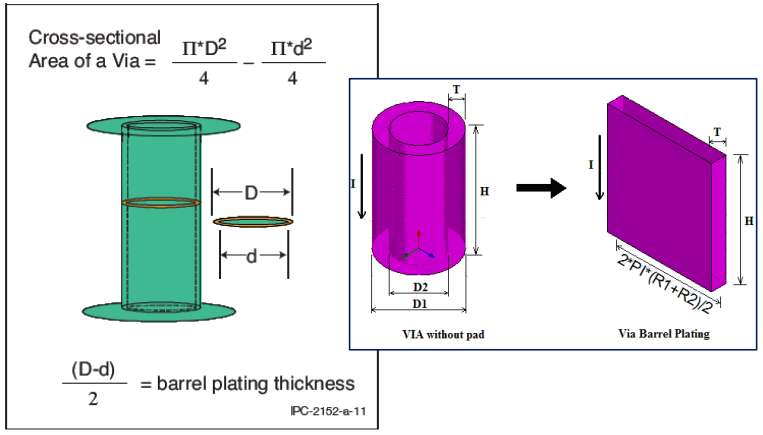
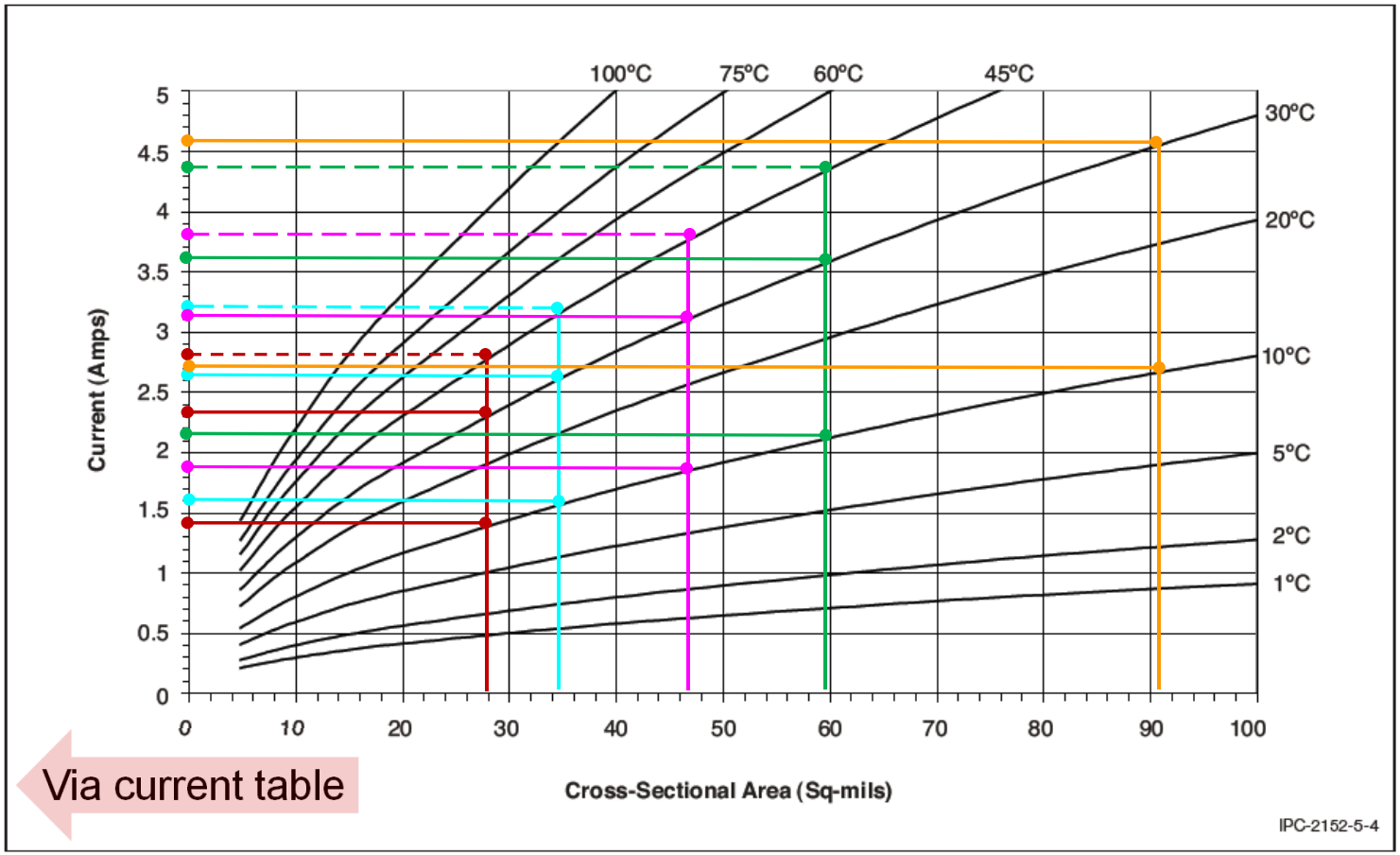


Figure A-11 Via Cross-sectional Area

Courtesy of IPC-2152

Via current guideline (Chart)



Via current table

Figure 5-4 Internal and External Conductors (Still Air) (5-100 Sq-mils)

Courtesy of IPC-2152

Note: The previous chart represents copper conductors in a polyimide or FR4 epoxy resin based PCB that is 70mil thick, without copper plane layers.

Via current guideline (Table)

Via size (mil)	Current for *10°C* temp rise (A)	Current for *30°C* temp rise (A)	Current for *45°C* temp rise (A)
8	1.2	2	2.3
10	1.4	2.3	2.8
12	1.6	2.6	3.2
16	1.8	3.1	3.8
20	2.1	3.6	4.3
30	2.7	4.6	5.7
40	3	5.5	6.8

- *Note: The previous chart represents copper conductors in a polyimide or FR4 epoxy resin based PCB that is 70mil thick, without copper plane layers. If copper planes are present, then temperature rise will be lower.*