Highly Reliable HDI

Blind & Buried Vias
Via-In-Pad & Laser Microvias

Basic Design Rules for Reliable PCBs

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The Goal of This Presentation

To provide modern PCB designers with a review of robust rules and methods that will allow them to design a highly reliable printed circuit board with the lowest cost, most commonly used features, and least number of manufacturing issues (that may result in a no-bid, engineering questions, placing the job on hold, or negatively impact the final yield).

During the writing of his book A Brief History Of Time the publisher told Stephen Hawking that if he included even one equation in the book it would effectively cut his prospective readership in half!

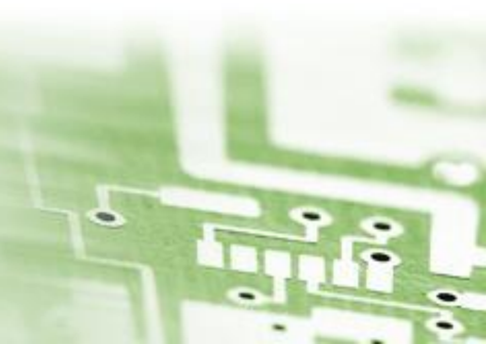
So in that spirit I will leave the equations to others that wish to use them in their own presentations.

I promise to keep it simple and to the point.

The Contents of This Presentation

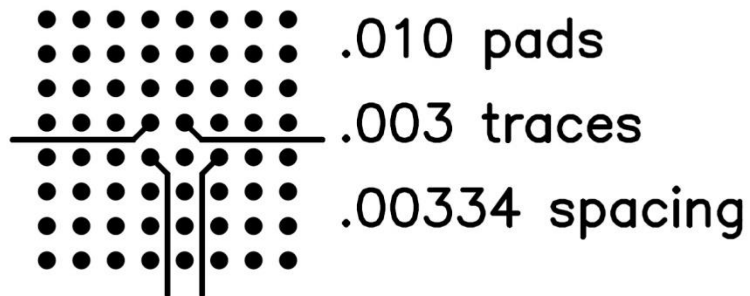
There are specific design rules available from the individual packaging suppliers (ex: Xilinx, Altera, Texas Instruments, Motorola, etc.) for device footprint layout metrics. We will not provide pad diameters, trace widths, spacing, etc. for each ball land pitch (0.5mm, 0.4mm, 0.3mm, etc.) as they are readily available from the manufacturers online.

Here we only wish to provide the minimums that if adhered to will provide the designer with a highly reliable physical PCB.

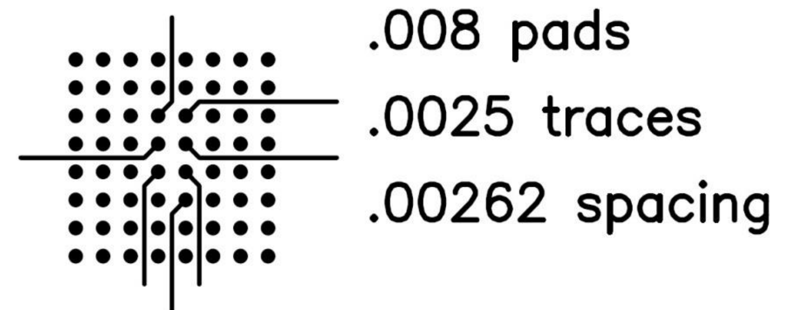


Rather than provide specific routing examples such as those below I would prefer to focus on design minimums as these boundaries are routinely pushed or broken in modern PCB design…

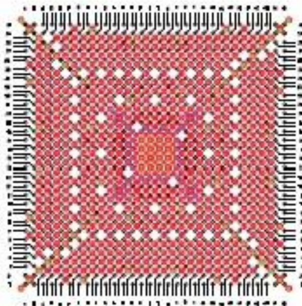
.5mm BGA=.01968



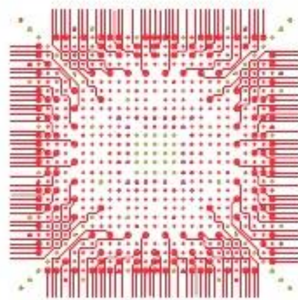
.4mm BGA=.01574



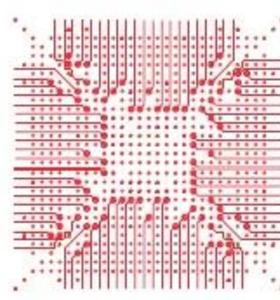
An Example of Readily Available Footprint Design Assistance



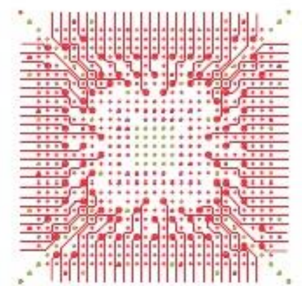
Top Signal Layer



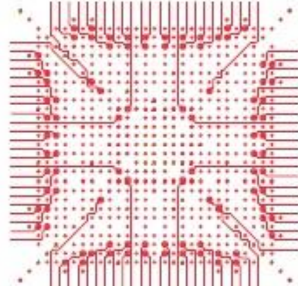
Second Signal Layer



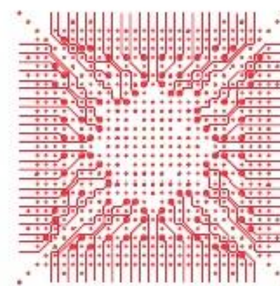
Third Signal Layer



Fourth Signal Layer



Fifth Signal Layer

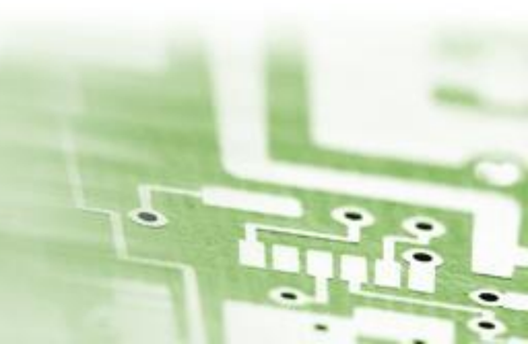


Sixth Signal Layer

Table 5-3: **Recommended PCB Design Rules (Dimensions in mm), Section 1**

	FT64 FTG64	FT256 FTG256	FG256 FGG256 FG320 FGG320 FG324 FGG324	FG400 FGG400 FG456 FGG456 FG676 FGG676 FG484 FGG484	FG680 FGG680	FG860 FGG860	FG900 FGG900	FG1156 FGG1156	EF668 EF672 FF668 FFG668 FF672 FFG672 FF676 FFG676	FF896 EF1152 EF1704 FF1704 FF1148 FFG1148 FF1152 FFG1152	FF1513 FFG1513 FF1517 FFG1517	SF363 SFG363
Component land Pad Diameter (SMD)[1]	0.40	0.40	0.45	0.45	0.50	0.50	0.45	0.45	0.53	0.53	0.53	0.40
Solder Land (L) Diameter	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.45	0.45	0.45	0.33
Opening in Solder Mask (M) Diameter	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.55	0.55	0.55	0.50
Solder (Ball) Land Pitch (e)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	0.80
Line Width Between Via and Land (w)	0.05 min.	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance Between Via and Land (D)	0.35 min.	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.56
Via Land (VL) Diameter	0.30	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.61	0.50
Through Hole (VH) Diameter	0.15	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300	0.300

BGA Footprint & Matrix Diagrams Courtesy of Xilinx Corporation

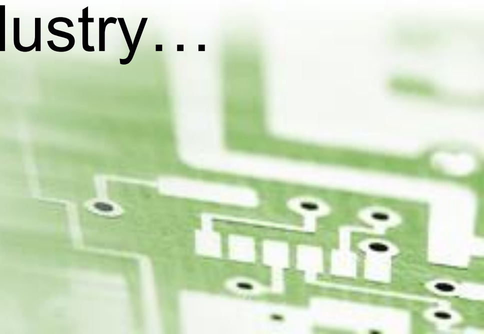


A Paradigm Shift in Technology

Today we are faced with a rapid reduction of PCB feature sizes due to the need for reduced form factor with fine pitch BGAs and small surface mount devices, and reduction or elimination of legacy components (replaced with ever smaller and denser packages).

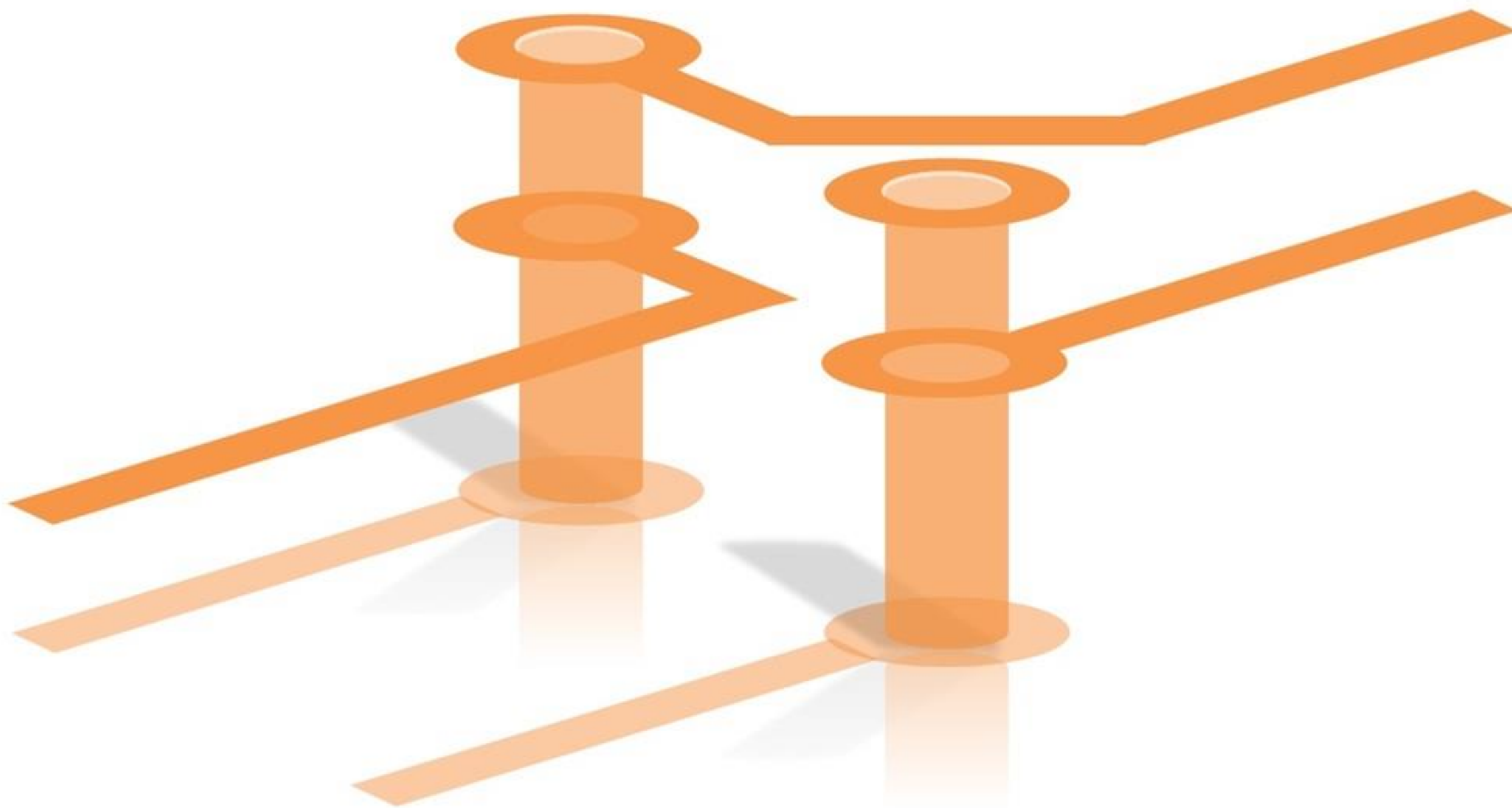
Add to this an increasing number of designers entering the workforce without experience in required design technologies (blind & buried vias, sequential lamination, via-in-pad, laser microvias, etc.).

This combination is a growing concern in the industry…

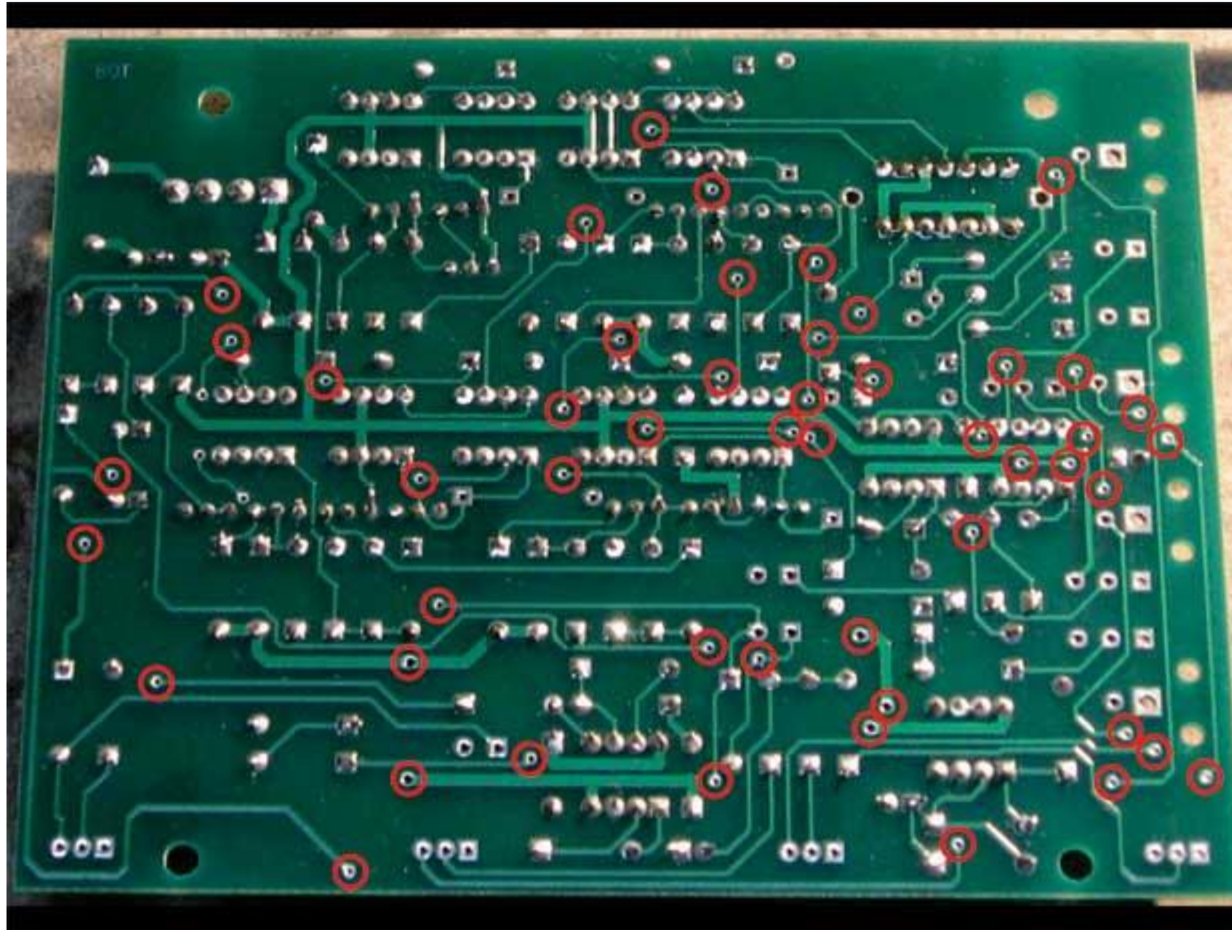


But First:

Some simple PCB review. Let's get back to basics to lend perspective to today's presentation…

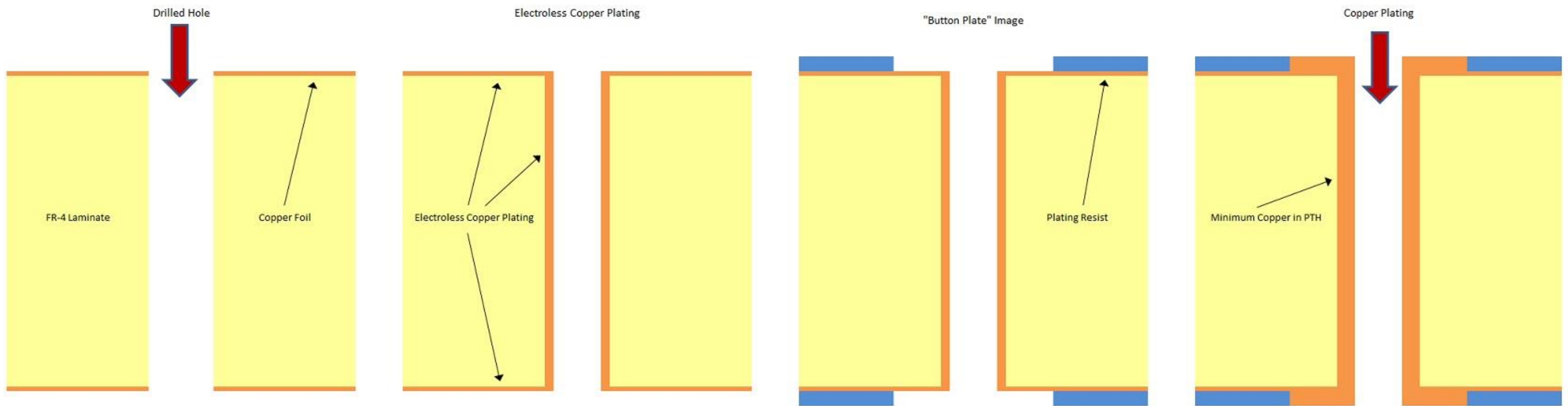


In their most basic form, via holes are used to connect traces from one board layer to another. Generally it enables a direction change (in the X or Y axis) in order to bypass device footprints and route signals from one end of the PCB to the other.



In this photo of a simple 1980’s PCB, the via holes are circled in red in this photo to distinguish them from the soldered component holes, which were mainly for DIPs.
There were very few hole sizes required—plated component and via holes, and non-plated tooling hole diameters.

Creating a Through Via Hole – Simplified Process Step Review



- Drill Hole in Laminate
- Electroless Copper Plating
- Image with Photoresist
- Electrolytic Copper Plating

Aspect Ratio of a Drilled Via Hole: Depth to Diameter (Example: 10:1 A/R)

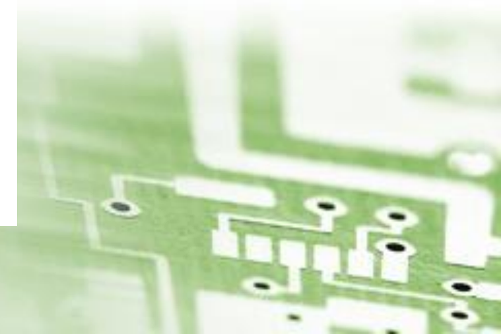
Aspect Ratio

Depth to Diameter Example: 10:1

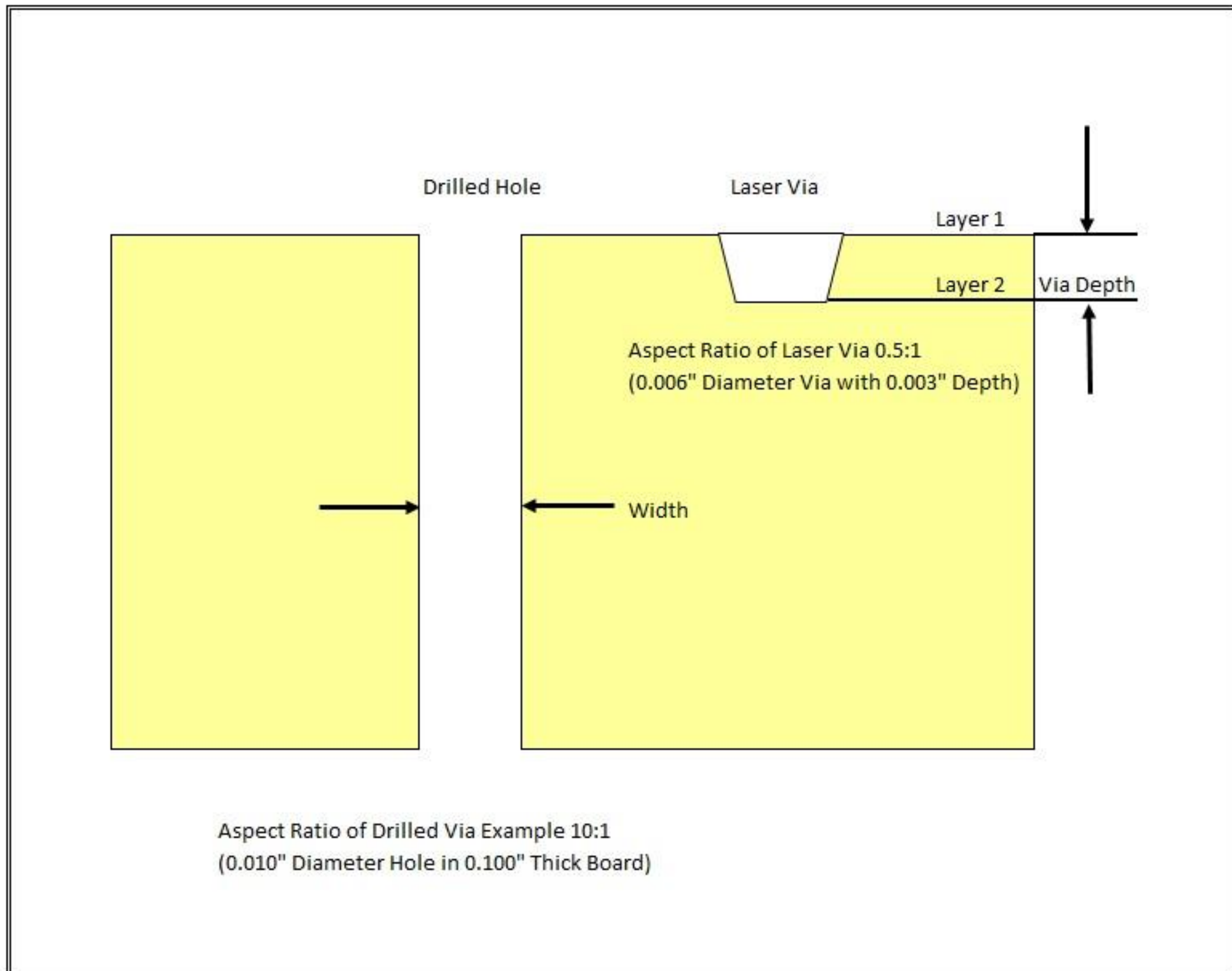
Aspect Ratio for Drilled Via

Depth
0.100"

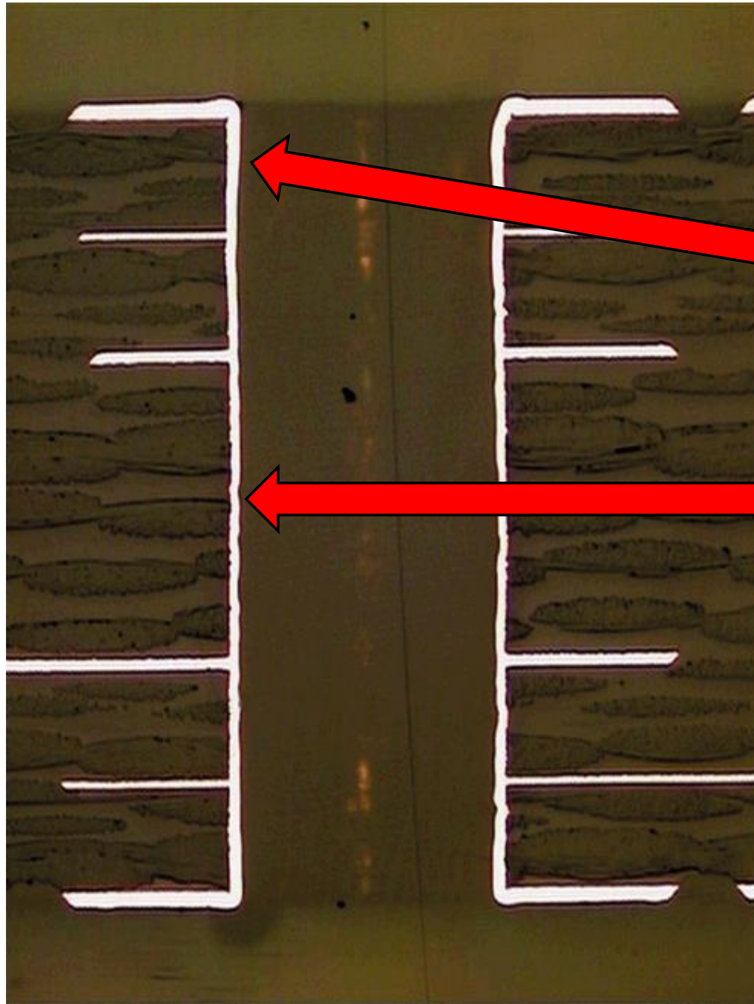
Diameter
0.010"



Aspect Ratio – Mechanically Drilled Via vs. Laser Microvia



Plated Through Hole - Microsection



Copper Plating at Knee

Copper Plating in Center

Copper plated component and via holes must be plated evenly from the “knee” to the center of the PTH. The outer areas of the hole generally plate faster which creates a “dog bone” plating profile in the PTH.

Plated Through High Aspect Ratio Hole Microsection

Higher aspect ratio holes require increased copper plating “throw” to plate evenly in the center of the PTH. This is accomplished with special plating processes such as reverse pulse plating.

Via-In-Pad

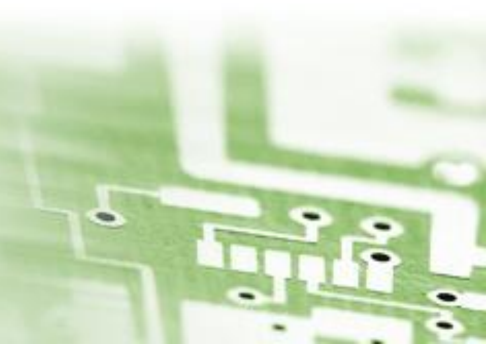
Definition:

A via interconnect hole that resides in a solderable pad, where the requirements are for a flat, planar surface that does not contribute negatively to the placement or orientation of the soldered component.

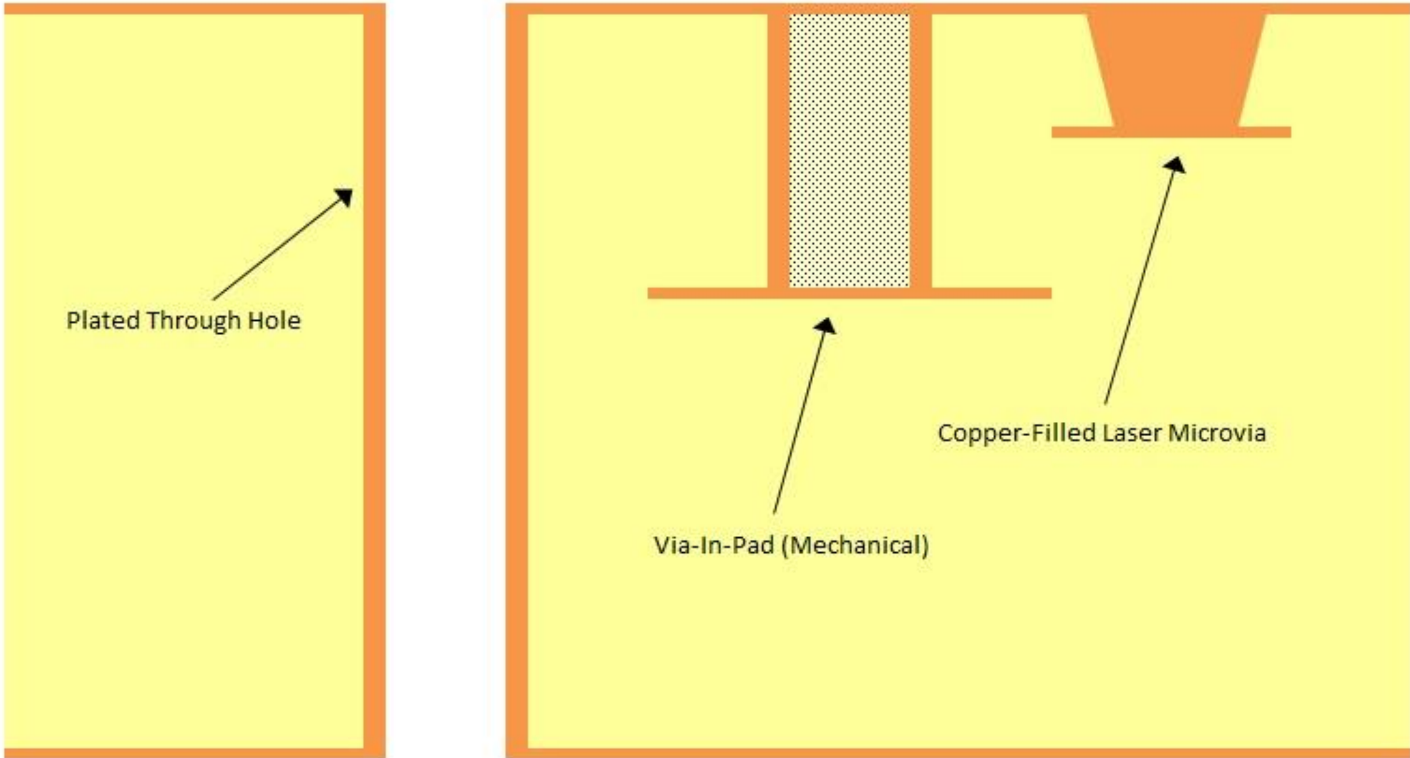
Common Method of Creating Via-In-Pad:

1) Using mechanical drills, the via spans one or several dielectrics and conductive layers, and is filled (post-plating) with a conductive or non-conductive epoxy material that is void-free and facilitates a planar surface to create the surface pad that a device will be soldered to.

2) Using laser ablation, the microvia spans a single dielectric and connects the surface layer to the next layer down in the stackup (except variable-depth microvias). The subsequent microvia is fully copper plated and planarized to create a flat surface pad that a device will be soldered to.



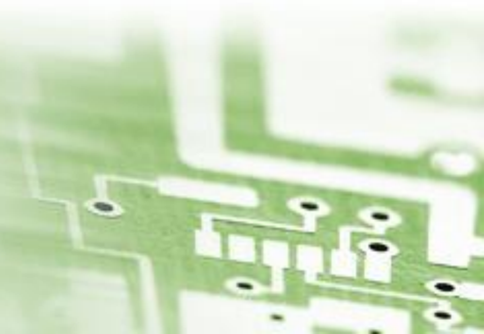
Via Illustration – PTH, Mechanical VIP, Microvia



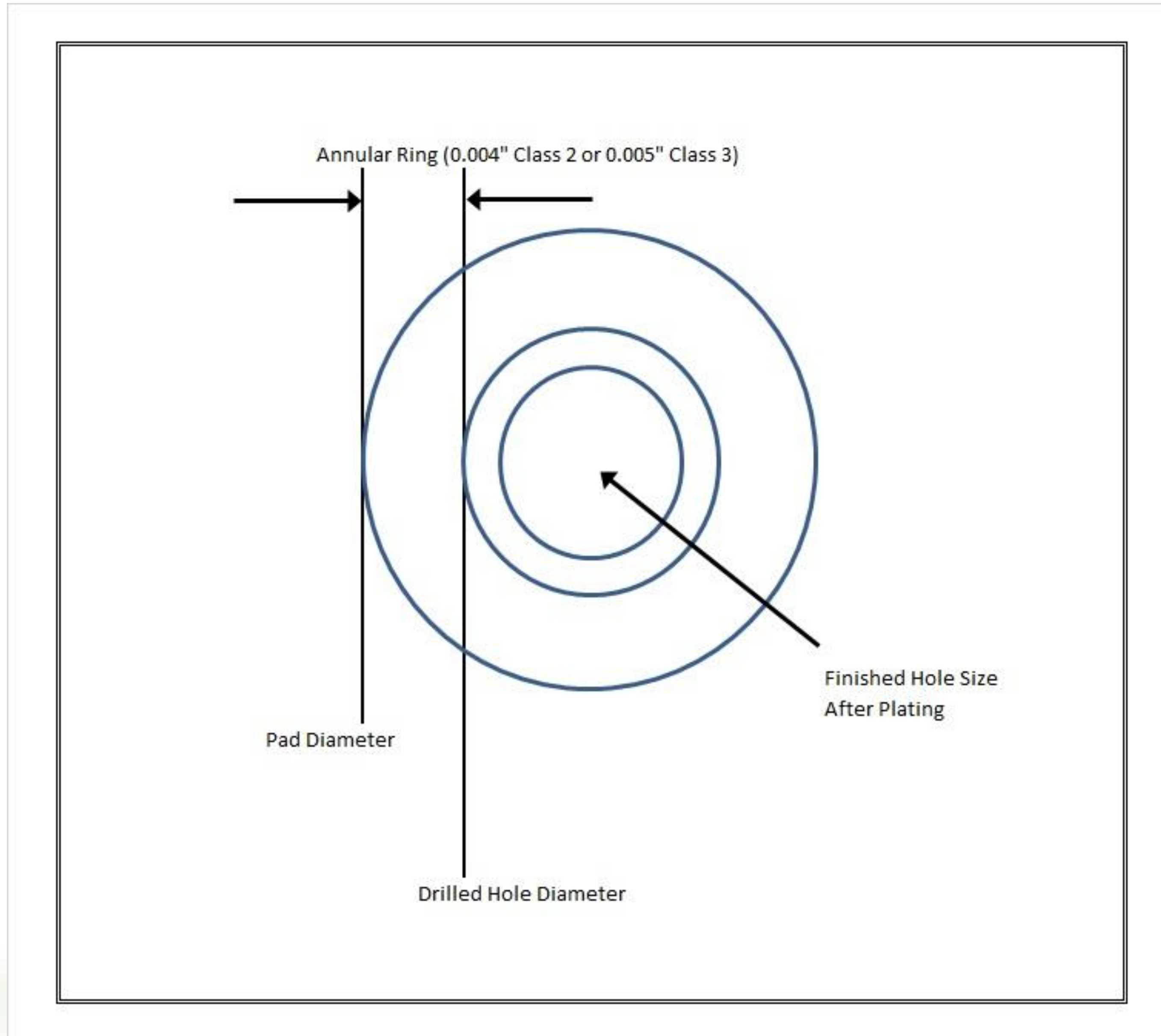
Next:

We will define some minimum design rules that should be considered in order to build a reliable physical printed circuit board.

Note that these rules are broken every day, and in some cases for good reasons. But they are proven to assure reliability.



Designed Annular Ring for Mechanically Drilled PTHs.



IPC Class 2 Commercial & Class 3 High Reliability Minimums

Epoxy Filled Mechanically Drilled VIP
Minimums & Maximums for >/= 97% Fill Requirements

Minimum:

The minimum finished hole size (FHS) after plating is 0.008”

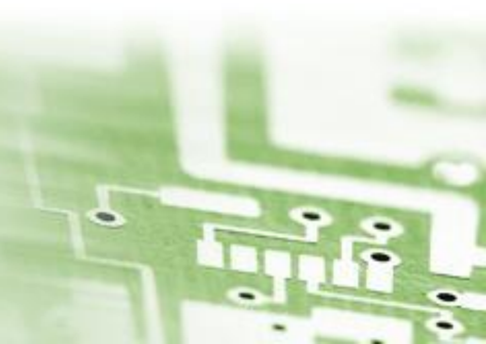
Maximum:

The maximum finished hole size (FHS) after plating is 0.018”

Reason:

FHS smaller than 0.008” are too small to reliably guarantee a complete epoxy fill using a single pass process (due to PTH plating profiles, hole wall irregularities, etc. present in 0.006” or smaller drilled vias).

FHS larger than 0.018” are typically too large to contain the epoxy fill material (without running out of the hole due to viscosity) prior to thermal curing. Aspect ratio plays a large part in this.



Epoxy Filled Mechanically Drilled VIP
Minimum Pad Diameter

Minimum Pad Diameter:

Designed to meet minimum IPC Class 2 or 3 acceptability after manufacturing.

IPC Class 2: Drill Diameter + 0.008” (0.004” Annular Ring)

IPC Class 3: Drill Diameter + 0.010” (0.005” Annular Ring)

Laser Drilled VIP
Minimum Pad Diameter

Minimum Pad Diameter:

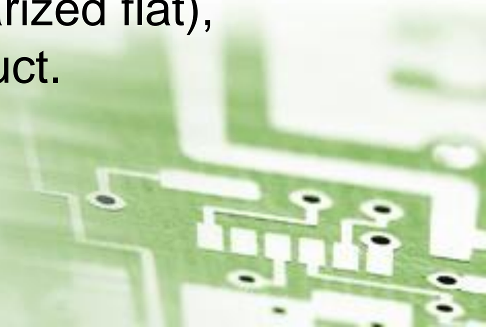
Designed to meet minimum IPC Class 2 or 3 acceptability after manufacturing.

IPC Class 2: Drill Diameter + 0.004” (0.002” Annular Ring)

IPC Class 3: Drill Diameter + 0.004” (0.002” Annular Ring)

Why is this?

The laser hole pattern registers to the sub-layer and scales accurately to match it in X/Y, so less A/R is required. Also, because laser microvias are fully copper filled (plated completely from bottom to top and planarized flat), there is no visible annular ring on the outer layer of the final product.



Mechanically Drilled Via Hole Epoxy Materials

Example: Two of Each Type Commonly Used

Conductive Epoxies (ex: Silver Coated Copper Particulates):

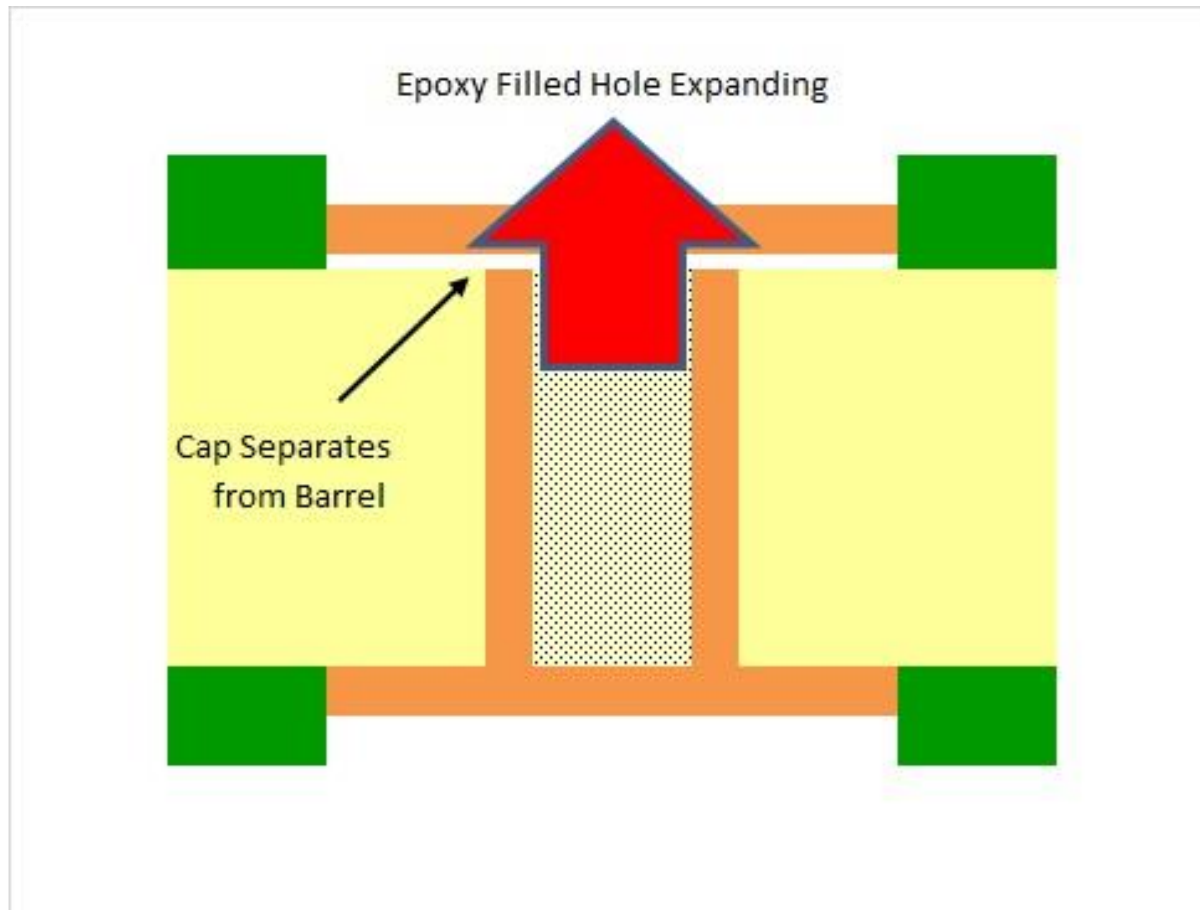
- DuPont CB-100
- Tatsuta AE3030

Non-Conductive Epoxies:

- San-Ei Kagaku PHP-900 IR10F
- Peters PP2795

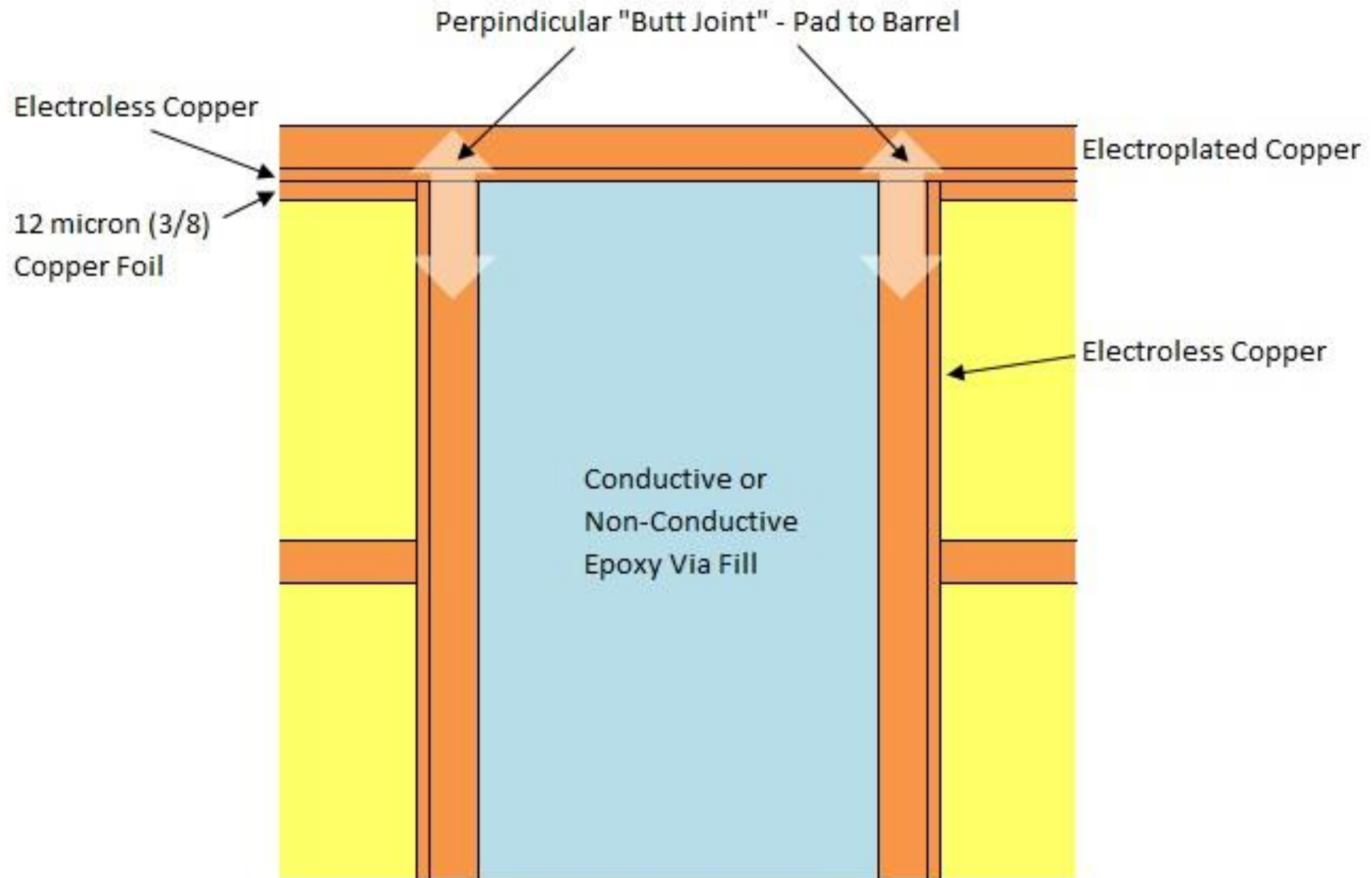
Basic Illustration of CTE in the PCB – Early Via Structure

Example: The Weak Link at the Cap

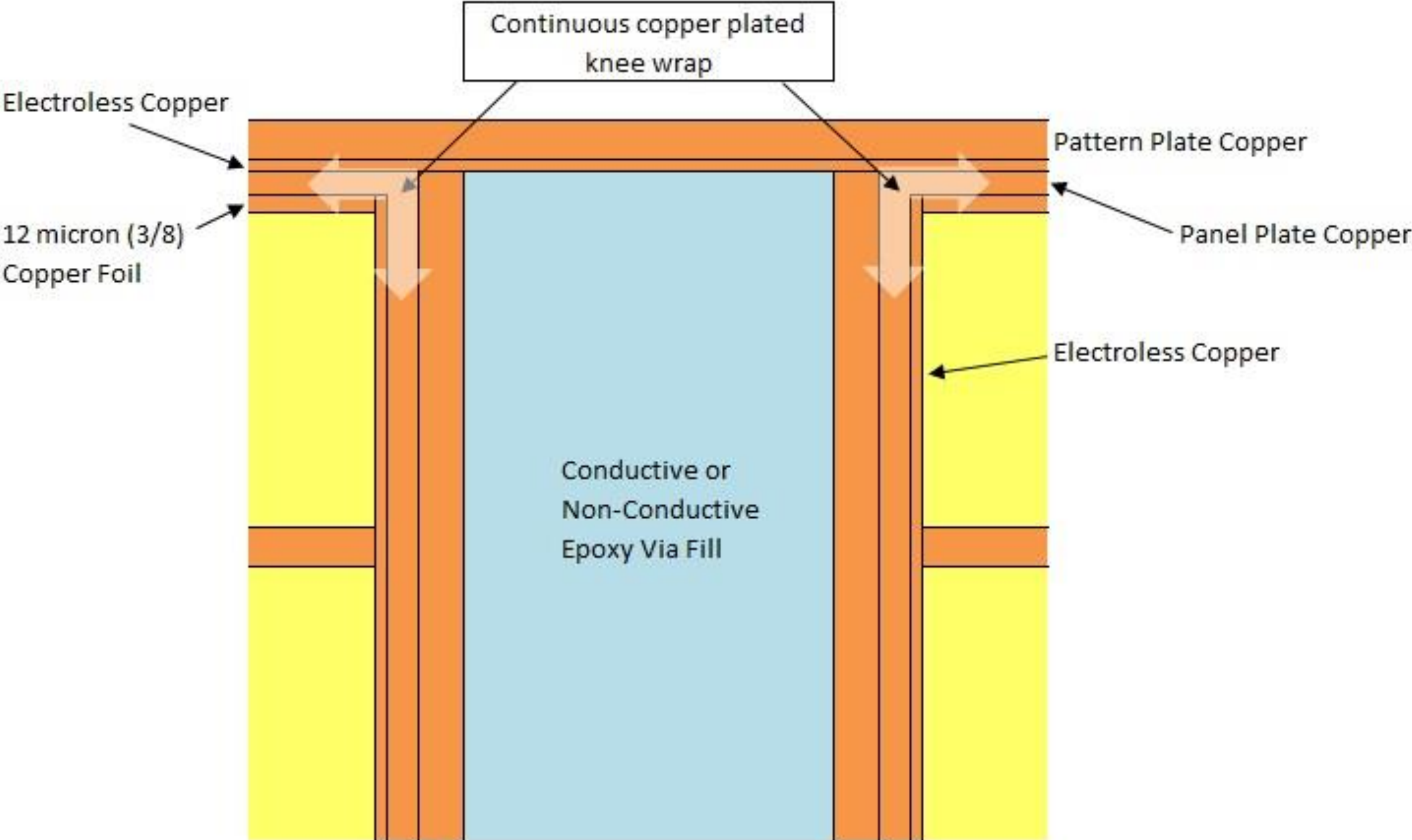


Remember this? It has been well over a decade since it first began…

Pre IPC-6012B Filled Via Hole Cross-Section



Post IPC-6012B Filled Via Hole Cross-Section



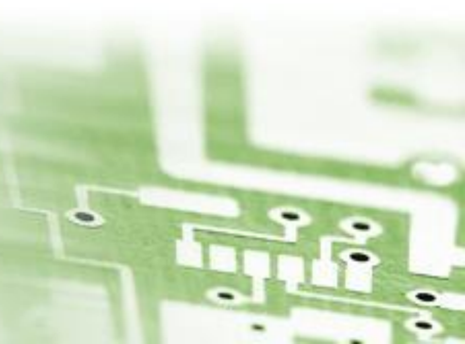
IPC-6012B Via-In-Pad Wrap Requirements

IPC-6012 Class 2:

A minimum of 0.0002” plated copper is required at the knee of the hole extending a minimum of 0.001” on to the surface (within the associated pad).

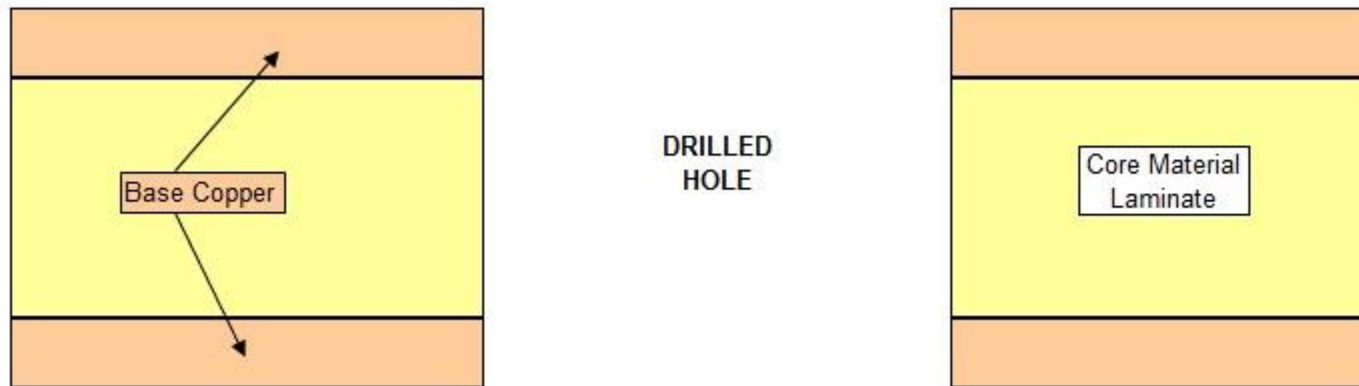
IPC-6012 Class 3:

A minimum of 0.0005” plated copper is required at the knee of the hole extending a minimum of 0.001” on to the surface (within the associated pad).



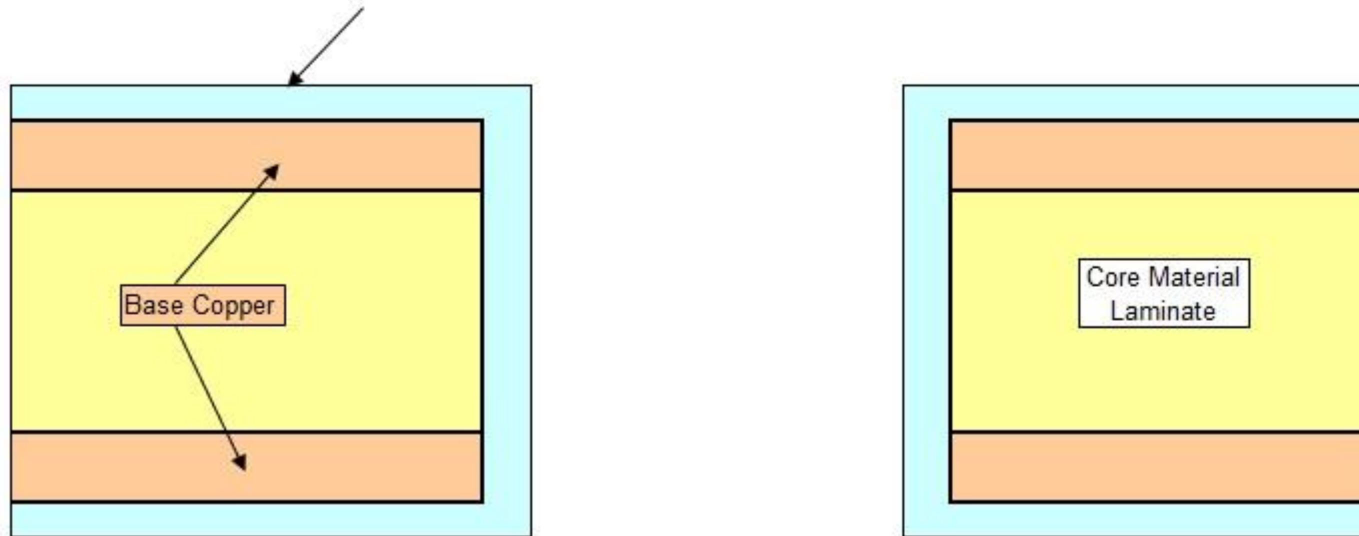
Sequence Diagrams Show PCB in PTH Microsection Profile

Perpendicular to Surface



First step of the sequence – the laminated board is drilled with the bit diameters that will produce the correct finished hole size after the plating operations.

PTH Wrap Process – Step 1

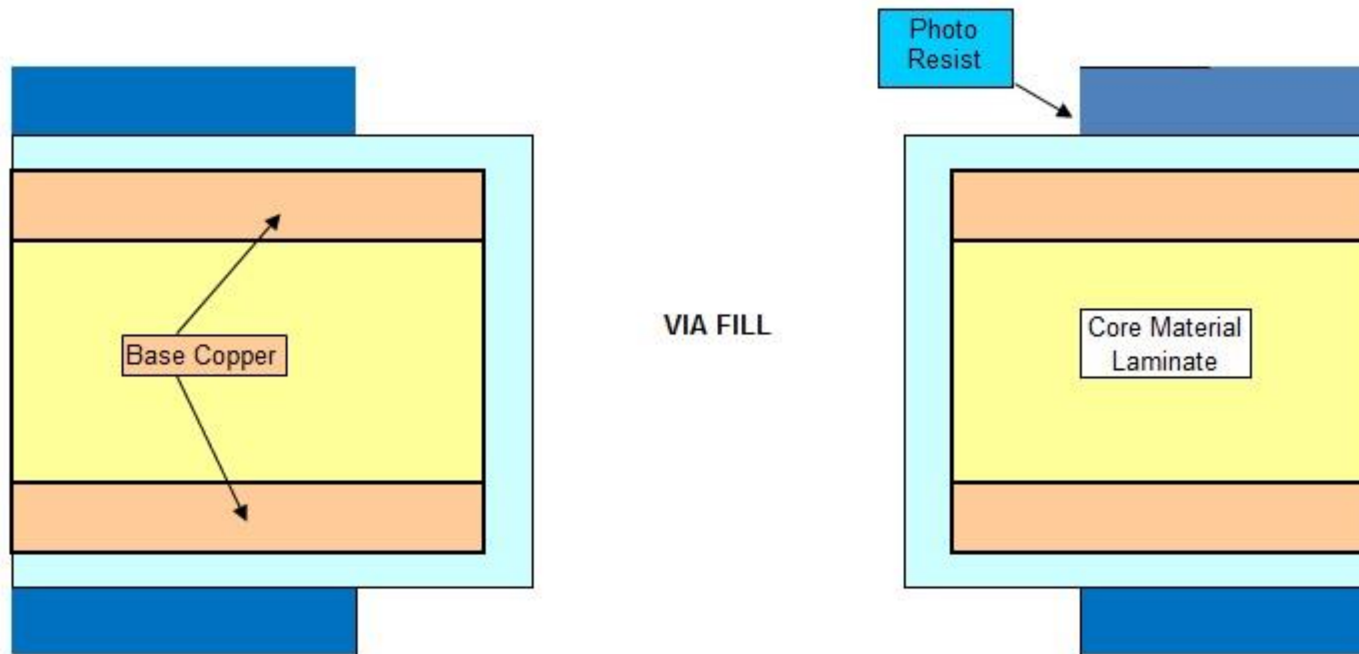


Second step of the sequence – the drilled board is panel plated to produce the minimum plated wrap thickness:

IPC-6012 Class 2 = 0.0002” minimum

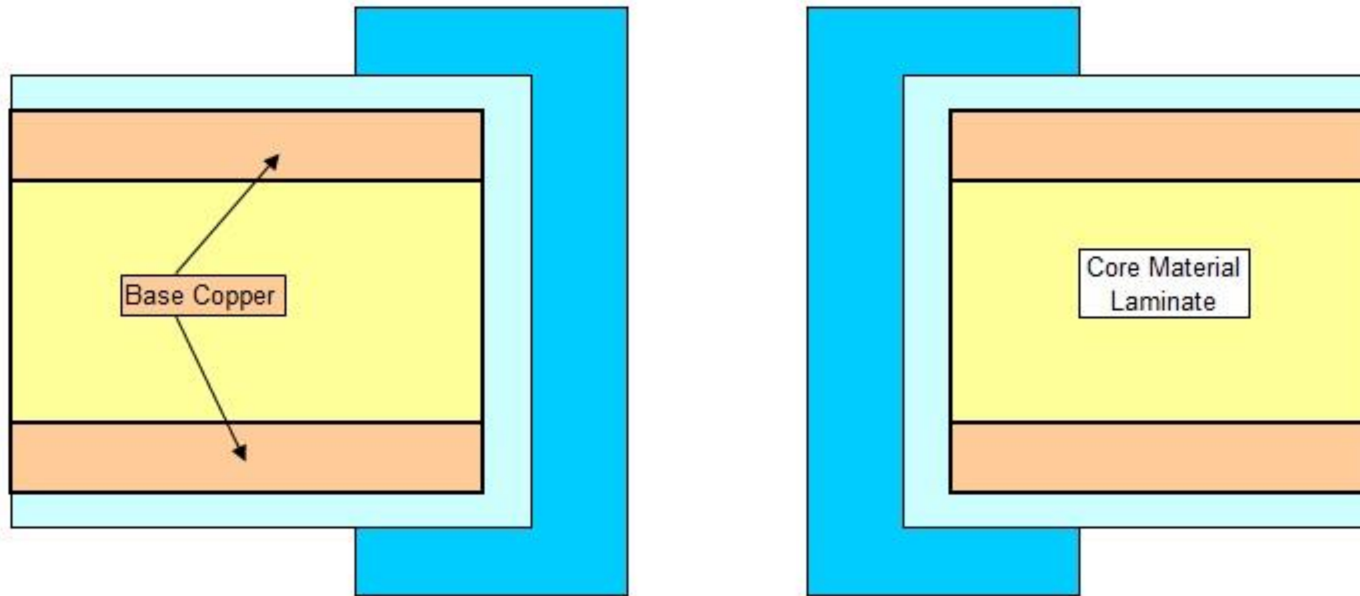
IPC-6012 Class 3 = 0.0005” minimum

PTH Wrap Process – Step 2



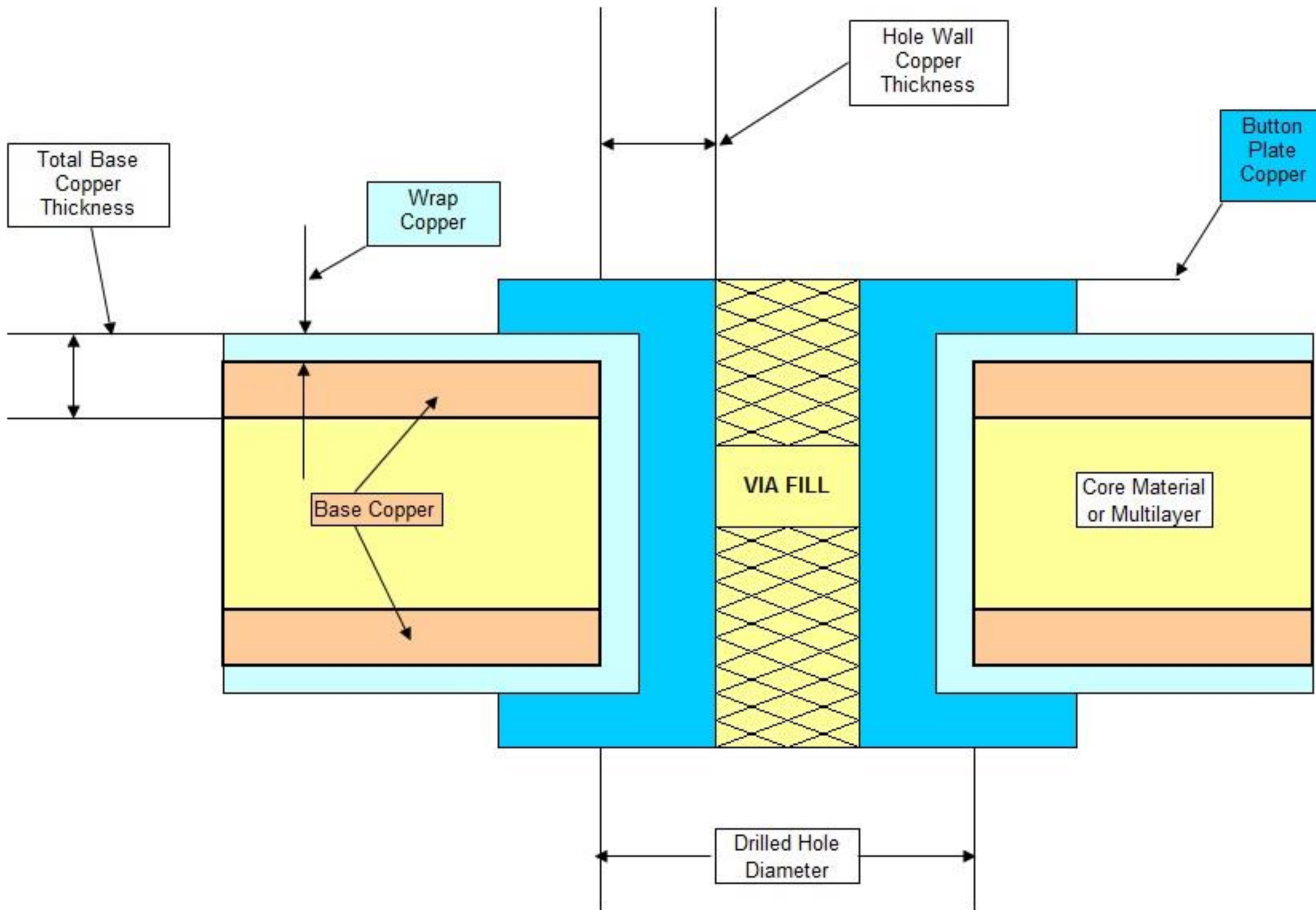
Third step of the sequence – the board is imaged and developed with a "button" that will produce a plated hole pad around the via hole.

PTH Wrap Process – Step 3



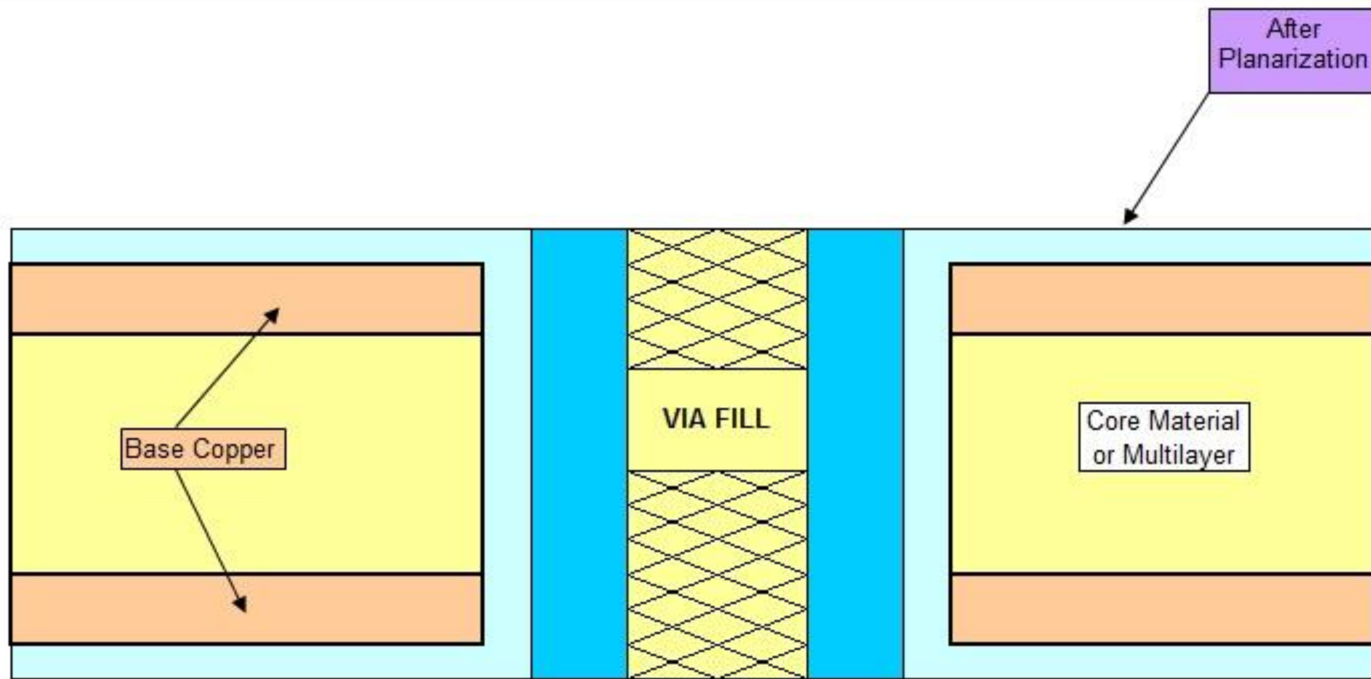
Fourth step of the sequence – the hole is pattern plated to produce the minimum thickness copper plating in the hole per IPC-6012 Class 2 or Class 3. The photo resist is then stripped leaving the plated “button” pad surrounding the plated through hole.

PTH Wrap Process – Step 4



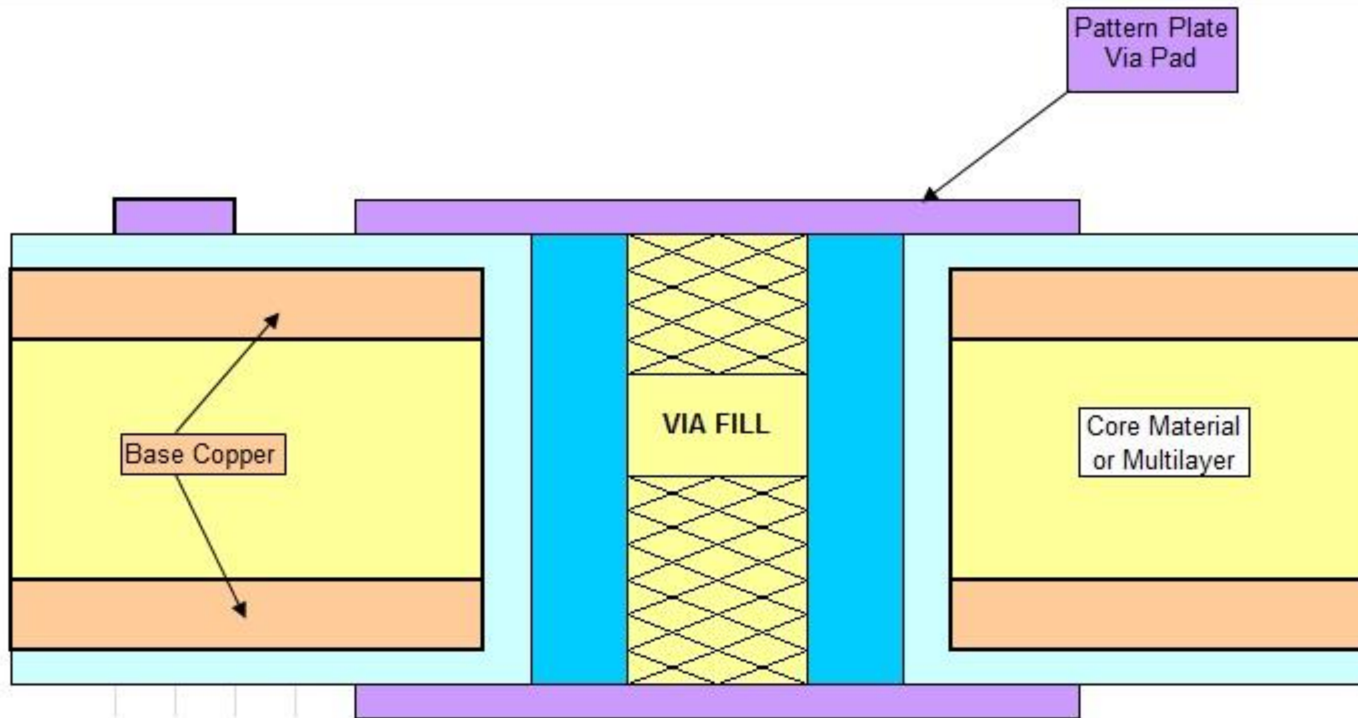
Fifth step of the sequence – the plated hole is filled with conductive or non-conductive via hole fill material and then thermally cured.

PTH Wrap Process – Step 5



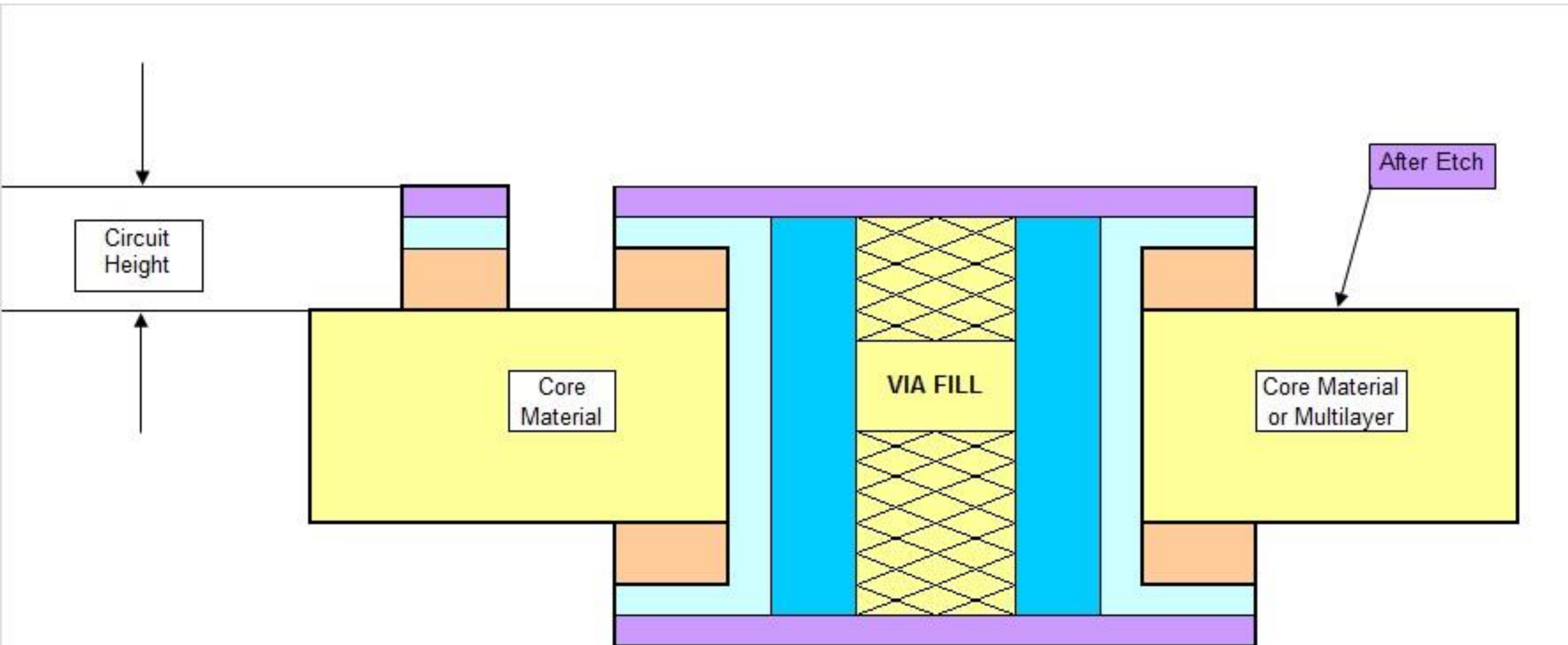
Sixth step of the sequence – the excess via fill material along with the plated “button” is planarized back to the wrap copper surface.

PTH Wrap Process – Step 6



Seventh step of the sequence (combined processes) – the panel has been processed through electroless copper (to metallize the via fill material), a subsequent flash plate to “cap” the hole, and finally the pattern plate image and plating operation to produce the final features. This simplified diagram shows the circuit image prior to final etch.

PTH Wrap Process – Step 7



Eighth step of the sequence – the board is etched to produce the final pattern. Note the cross-section of the circuit and pad sections: The final thickness is based on the minimum wrap thickness plus minimum hole plating thickness to meet IPC-6012 Class 2 or Class 3. This combined copper thickness may limit the finished line width due to etch limitations.

PTH Wrap Process – Step 8

How Wrap Requirements Determine Trace Width / Space

The required minimum copper thickness specifications of both the IPC-6012 wrap plating and final plated through hole thickness becomes the limiting factor for trace and space widths. For example, if the specification is IPC-6012 Class 3 then the minimum copper thickness is determined by the following:

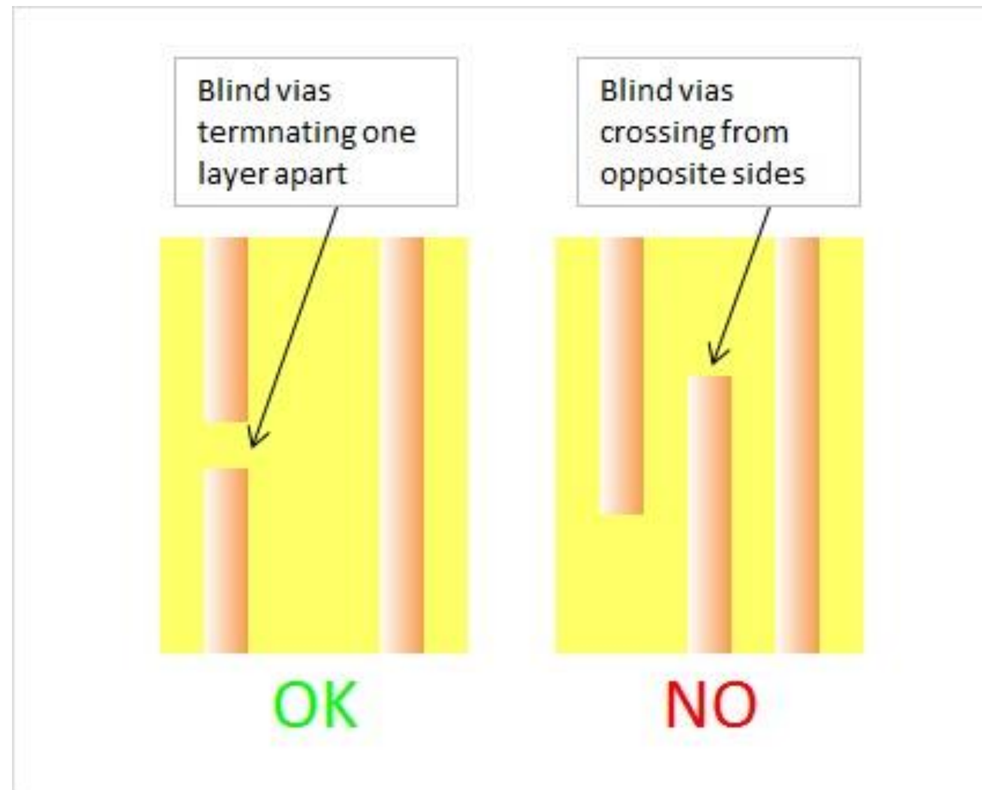
Minimum Class 3 wrap thickness: 0.0005”
Minimum Class 3 plated through hole thickness: 0.001”

Add to that:
Base copper foil thickness: 3/8 ounce aka 12 micron (0.000525”) or 0.5 ounce (0.0007”)

Also consider slightly more thickness (0.0002” typ.) added at each plating operation to assure that minimums are met.

Combine all of the plating steps with the base copper thickness and the sum will be the amount of copper that will determine the MINIMUM trace width and spacing that can be achieved.

“PCB 101” Via-In-Pad Design Rules (Mechanically Drilled Holes)



When designing a stackup the basic rule of mechanically-drilled blind vias is to:

1) Vias originating on opposite sides of the board must terminate at least one layer apart. They cannot terminate on the same layer.
2) Vias originating on opposite sides of the board must not cross each other (see rule #1).

Next: Microvias – Laser Formed Plated Via Interconnects

"Input1": port 1

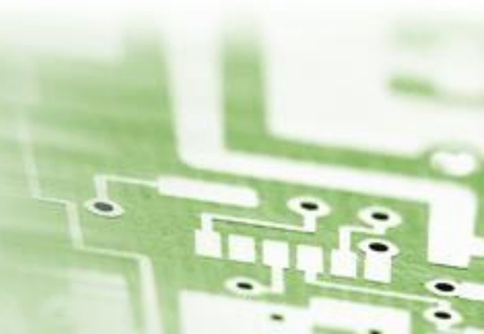
"Input2": port 2

21 Dec 2006, 19:38:39, Simberian Inc.

Image Courtesy of Polar Instruments

Microvias

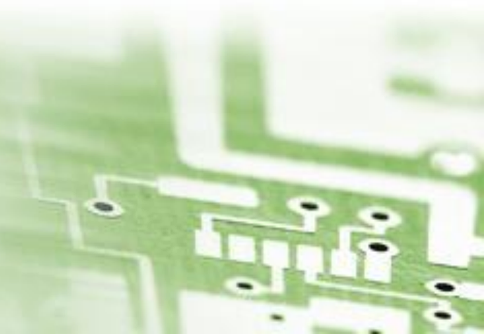
“With the introduction of the Ball Grid Array (BGA), board feature dimensions began dropping from fractions of an inch to thousandths of an inch until it became clear that the traditional manufacturing technologies had reached a point where they could no longer do the same things in the same ways, only smaller. A new revolution was upon the industry, one dubbed the *Density Revolution,* and it continues today. It has officially become the High-Density Interconnect (HDI) Revolution.” *The HDI Handbook*



Microvias

IPC-2226 1.5.2 HDI Types (I, II, & III of VI)

- TYPE I – (1 + n + 1) – Laser Microvias on Both Sides of the Board.
- TYPE II – (1 + n + 1) – Laser Microvias on Both Sides of the Board, with Buried Vias in the Core.
- TYPE III – (2 + n + 2) – Laser Microvias on Both Sides of the Board—may Have Buried Vias in the Core.



Microvias – Type I

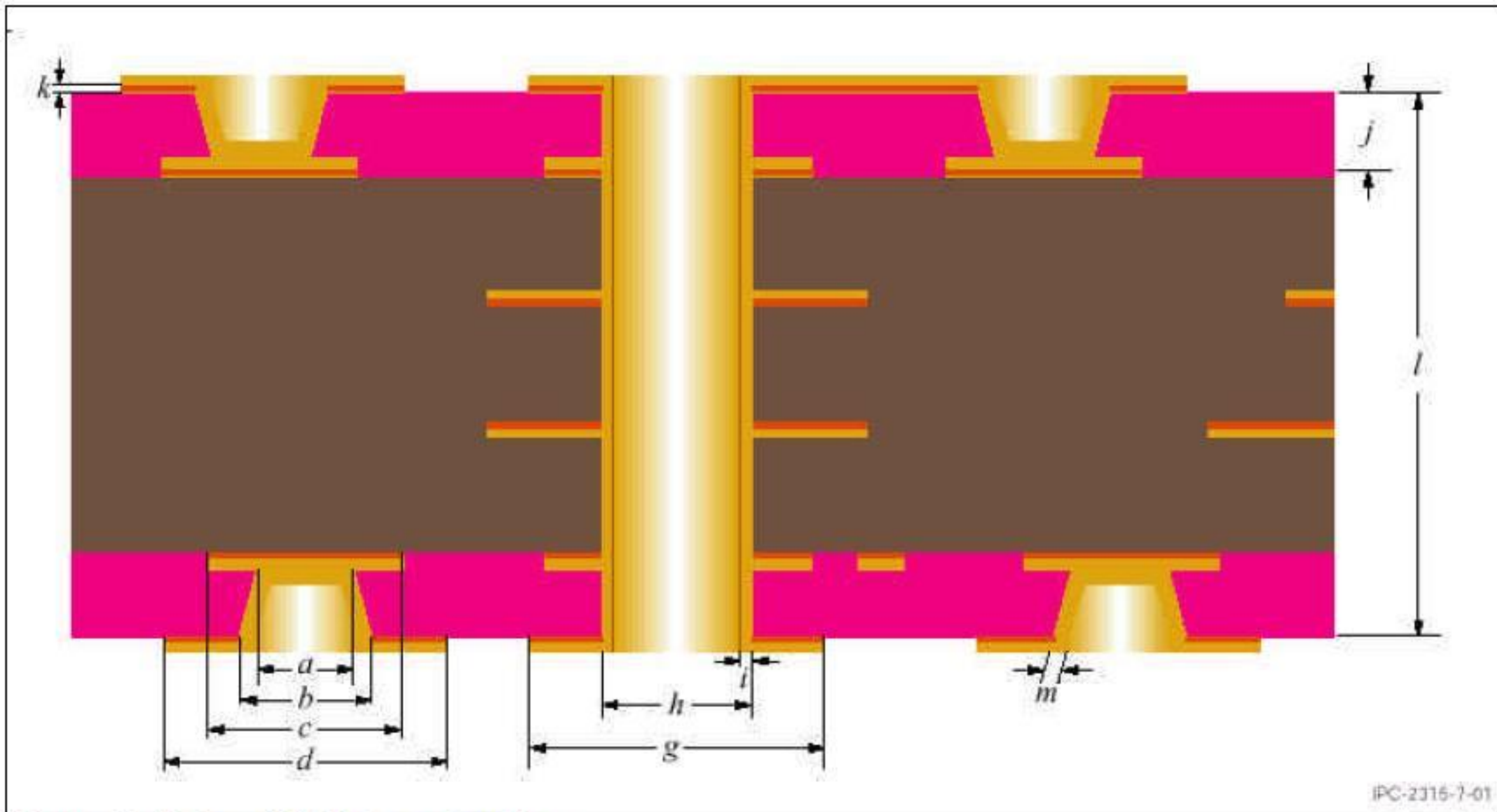


Figure 5-1 Type I HDI Construction

Microvias – Type II

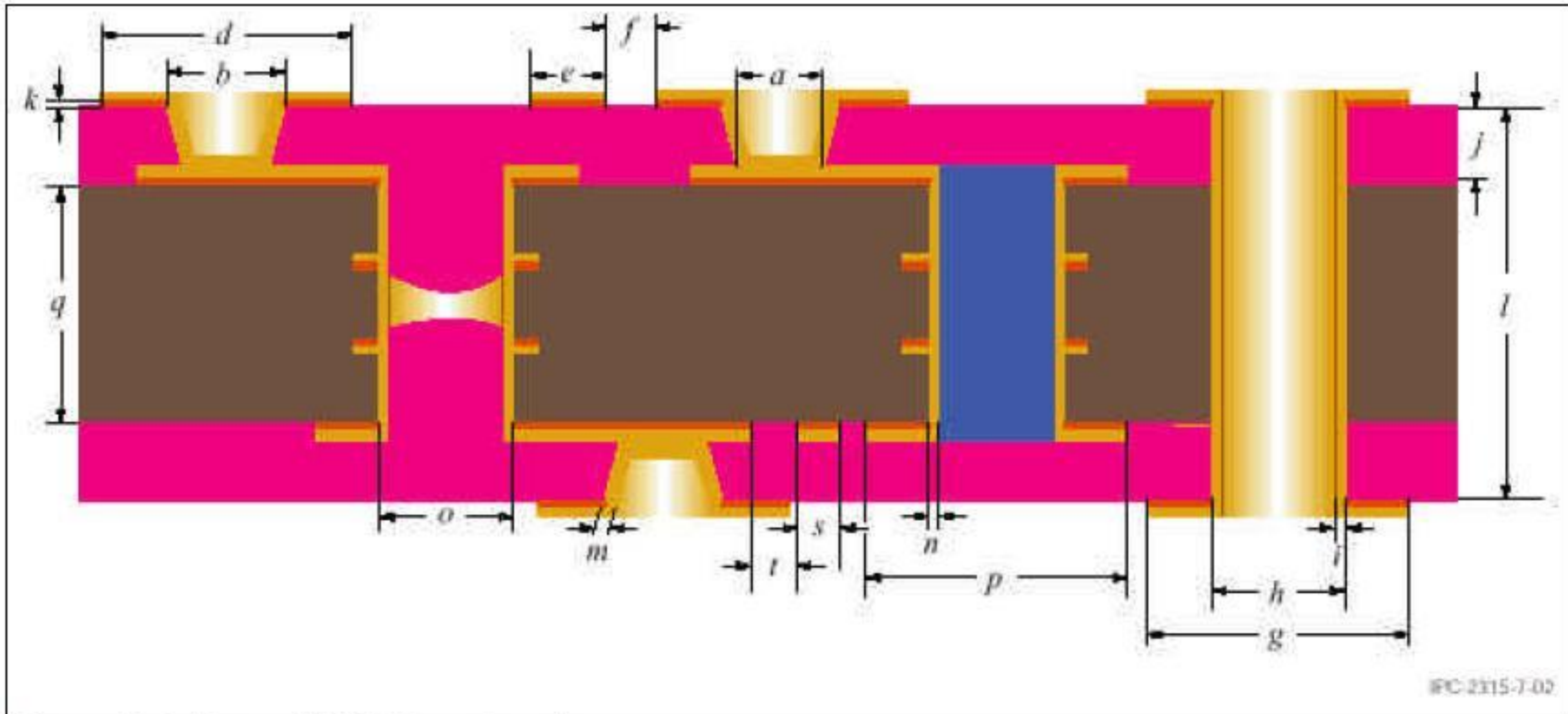


Figure 5-2 Type II HDI Construction

Microvias – Type III

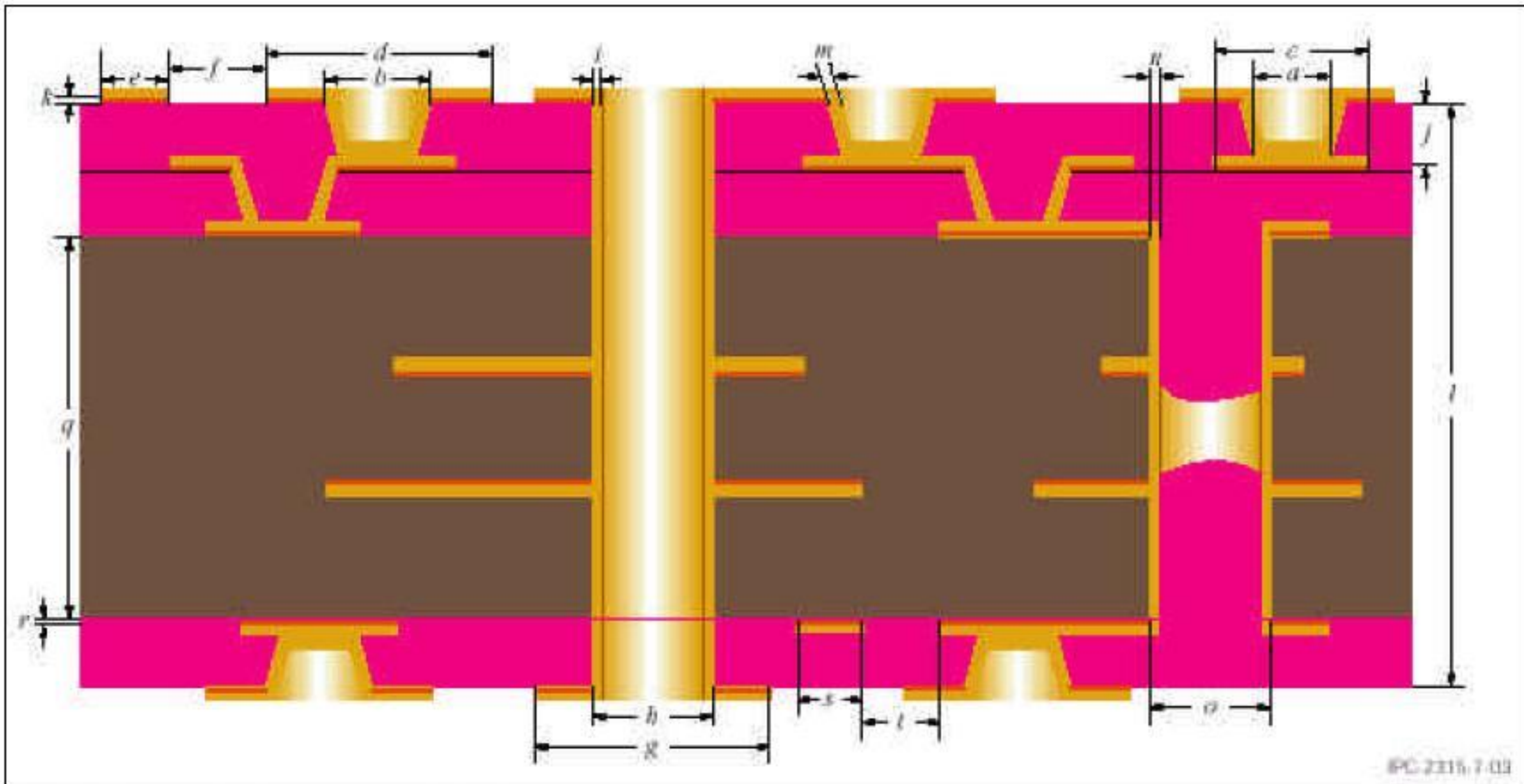


Figure 5-3 Type III HDI Construction

Microvias – Type III Stacked

Figure 5-4 Type III HDI Construction with Stacked Microvias

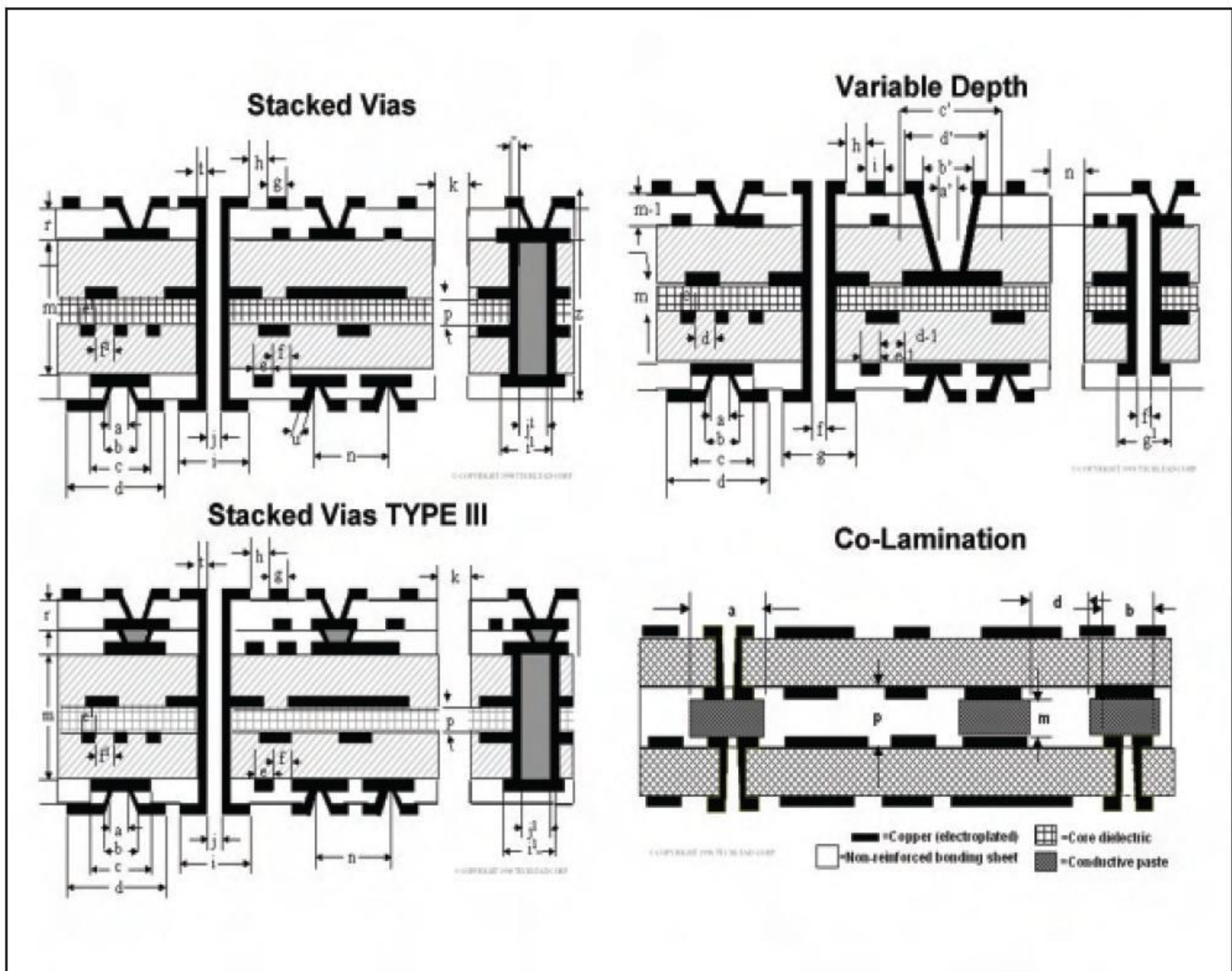
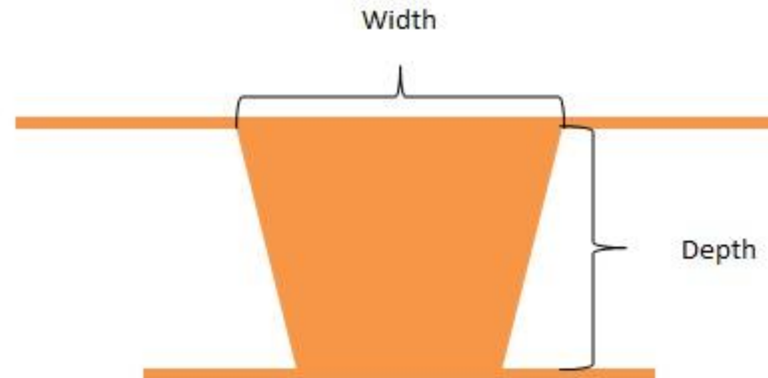


FIGURE 5: Additional HDI structure diagrams from IPC-2315[1]

Microvias – Aspect Ratio

Microvias - Aspect Ratio Diagram



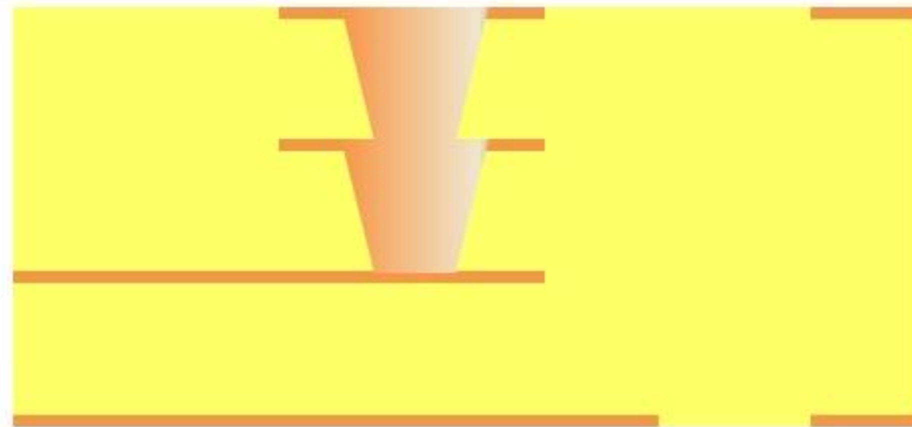
Aspect Ratio is defined as depth-to-width ratio.

So an aspect ratio of 1:1 denotes equal depth and width.

An aspect ratio of 0.5:1 denotes a depth one-half of the width.

Aspect Ratio is very important in microvia formation. The current standard remains a most manufacturable 0.5:1 aspect ratio.

Microvias – Stacked Microvias



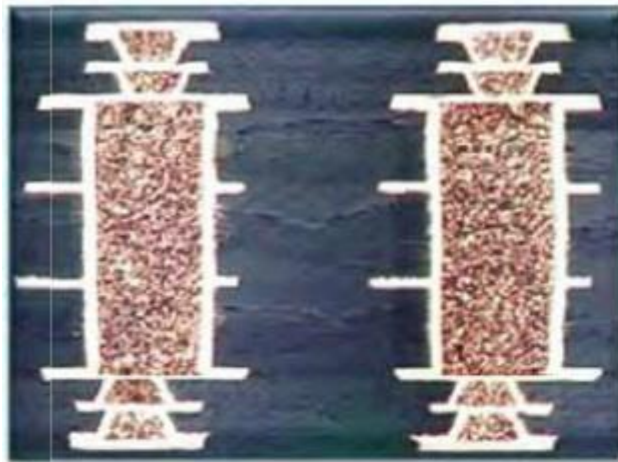
With the advent of fine-pitch BGAs with many more rows of interconnects it is necessary to stack microvias to route surface signals to multiple layers below. Due to the tight spacing a single track between pads may not be feasible (due to greatly decreased line widths) so the ability to drop down another layer to fan out the signal is mandatory.

The flip side of this is the increased CTE mismatch between the solid copper microvia structure and the surrounding laminate. Laminate/copper stress cracks are more likely in stacks exceeding a 3 high structure (with typical PCB microvia diameters). Note that the CSP world has been doing this for many years successfully stacking 5 high +, but at much smaller diameters and dielectrics on different substrates.

CTE & Stacked Via Structures

CTE plays a key role in the reliability of filled vias, and an even more critical factor when via structures are directly stacked.

In the microsection photo below, the CTE mismatch between fill, plating and laminate become amplified by the increased Z-axis of the stacked microvia structures directly on top of the buried/filled via.

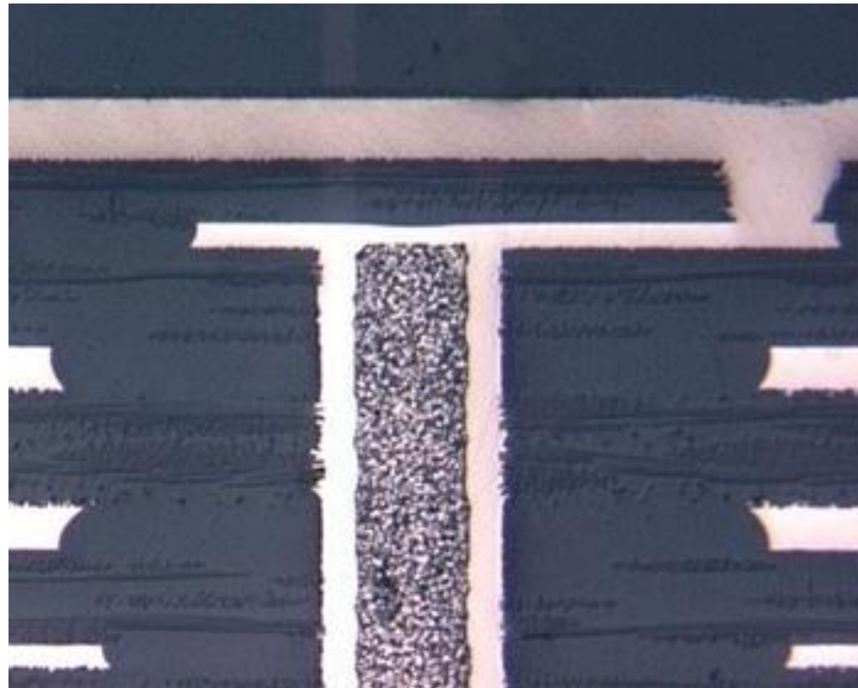


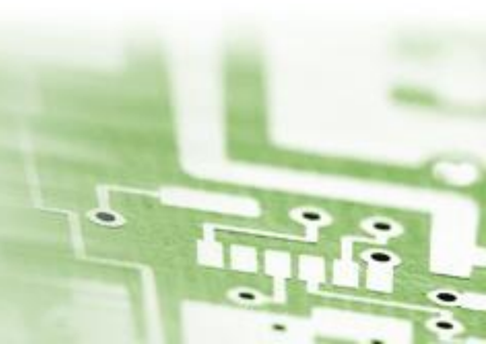
2-4-2 Build-up Multilayer

This is an older industry photo showing epoxy filled microvias but still serves to illustrate stacked microvias over filled buried vias.

CTE & Stacked Via Structures

When stacked microvia on buried/filled via structures are required, it is a better practice to offset the microvia structure from the buried/filled via. This allows both structures to expand and contract, but lessen the probability of a stress crack propagating within the padstack intersections.





Okay, so where is this all going?

The packages are getting smaller every day, which necessitates smaller pad diameters resulting in two distinct issues:

1) Pads </= 0.006” have reduced adhesion.
2) Smaller microvias require thinner dielectrics.

Remember RCC (RCF)?

It was a boon for cell phone designs and a clean laser-drilled microvia was easy with a thin dielectric that did not have e-glass. But this lack of e-glass created its own set of issues, particularly X/Y dimensional stability.

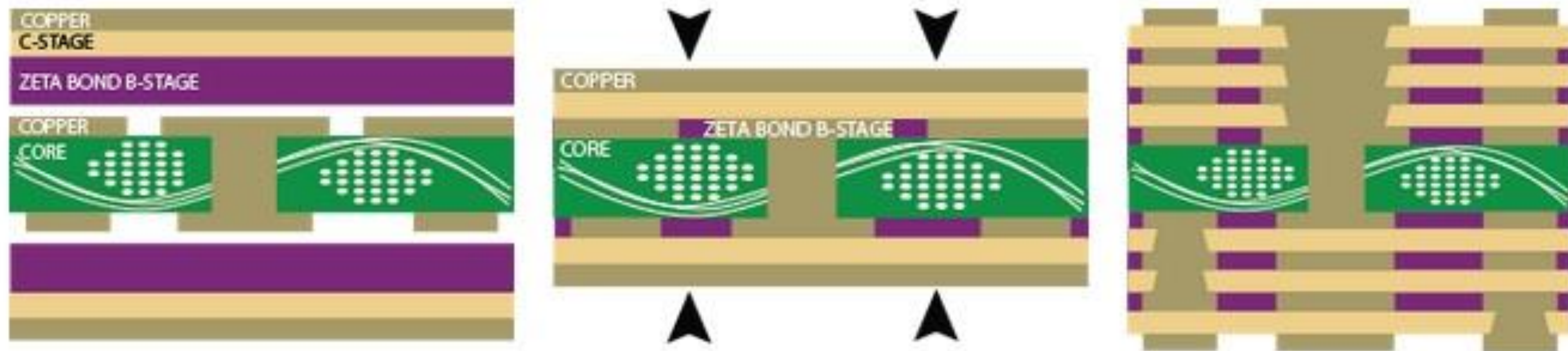
So Welcome to the Next Generation of Microvia Dielectrics!

Integral Technologies Zeta materials (particularly ZetaLam HDI dielectric) provides better adhesion of small diameter pads along with a thin non e-glass dielectric layer for excellent hole formation.

ZETA® LAM

| Print | Email

To create **Zeta® Lam**, Zeta® Cap is attached to a B-stage bonding film capable of filling circuits and vias for ultra-thin HDI build-up structures with improved transmission line performance.



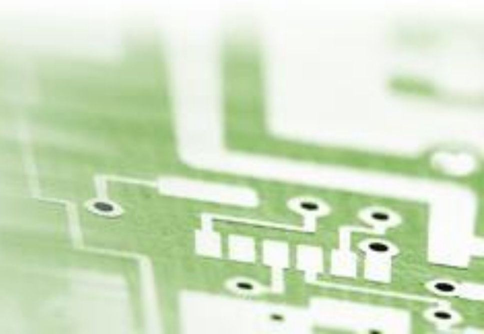
Zeta® Cap's unique liquid cast polyimide film is bonded to copper foil in a high temperature furnace not found in PCB factories. This C-stage layer is laminated to a proprietary B-stage bonding film called **Zeta® Bond**. The C-stage polyimide film acts like the glass dielectric in conventional prepreg. It provides an ultra-thin, guaranteed copper-to-copper Z-axis standoff as thin as 12 microns with no glass. Zeta Bond's high flow and leveling characteristics allow it to fill vias and between traces without adding to overall package thickness. Zeta Lam's bonding film is unlike traditional film adhesives. It has a low CTE, high Tg and high Td, which makes it suitable for sequential lamination cycles and higher layer HDI structures.

Okay, so what is possible now?

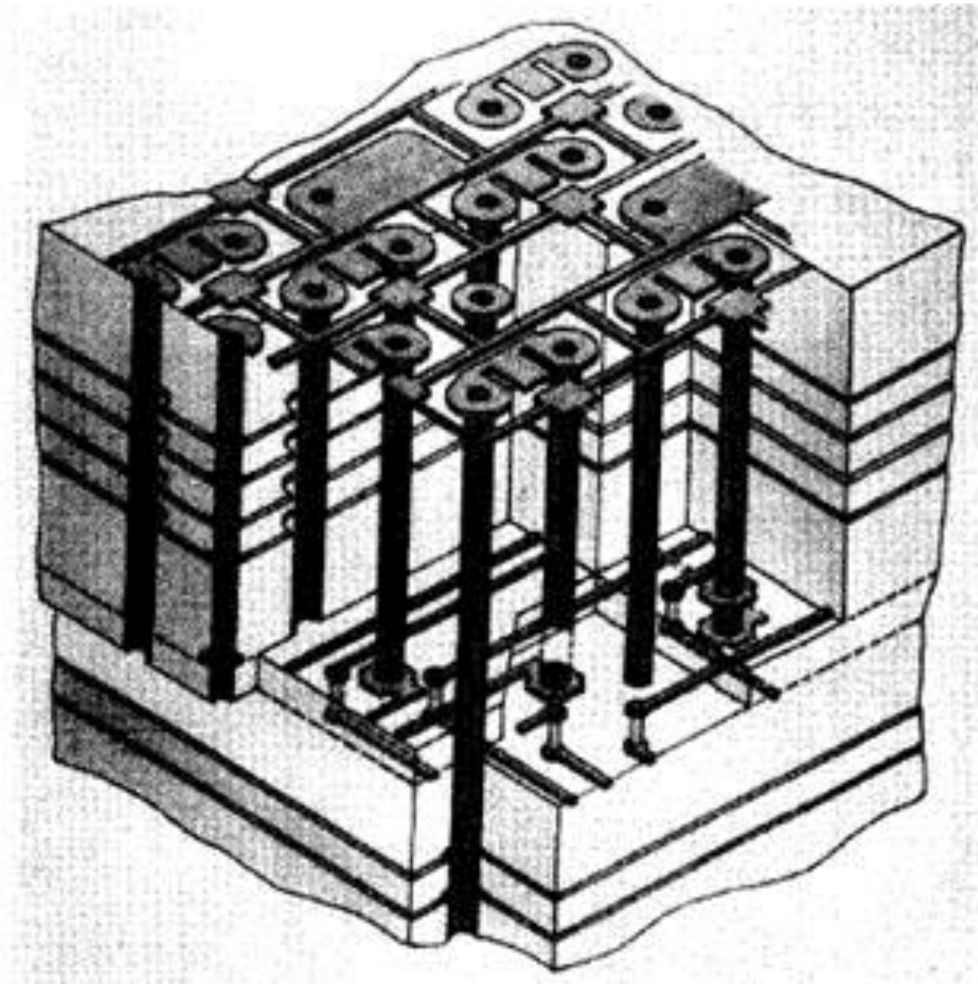
Microvias of 0.002” diameter with an aspect ratio of much less than 1:1 are possible with ZetaLam.

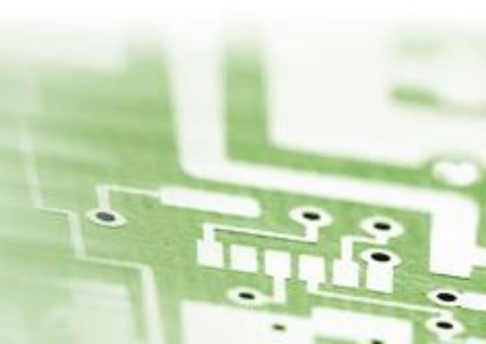
1) Pads of 0.006” diameter have adhesion and avoid “pad cratering” at assembly.
2) Smaller microvia aspect ratio is possible due to the thin dielectrics.

High Reliability is Maintained!



Follow-Up Q&A





About Advanced Circuits, Inc.

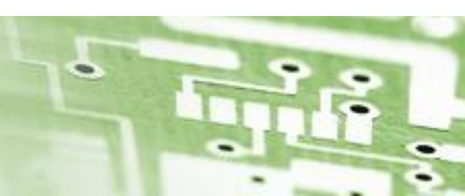
- Founded in 1989
- 3rd Largest PCB Manufacturer in North America
- 100% US Based Manufacturing – ***Made in the USA!***
- 3 Manufacturing Locations Totaling Over 200,000 sq. ft.
  - Aurora, Colorado – Corporate Headquarters
  - Tempe, Arizona – Advanced Technologies
  - Maple Grove, Minnesota – Advanced Technologies and Specialty Products
- Over 500 Employees, 3 Shifts, 24 Hours per Day, Monday-Saturday
- Military/Aerospace/Defense Supplier for Over 15 Years
- ISO 9001, AS9100, MIL-PRF-31032, MIL-PRF-55110, ITAR Registered
- Expedited Leadtime Specialists
  - SAME DAY and WEEKEND TURNS available for some technologies
  - No minimum orders or lot sizes
  - Industry's best on-time shipping record
- Industry Innovation/Pioneering
  - 2002: FreeDFM.com – Pre-order file review with automated feedback report
  - 2007: PCB Artist Layout Software – #1 free downloaded PCB layout software

Advanced Circuits Locations

Advanced Circuits
Tempe Division
229 S. Clark Drive
Tempe, Arizona 85281
25,000 sq.ft.

Advanced Circuits
Maple Grove Division
8860 Zachary Lane North
Maple Grove, Minnesota 55369
50,000 sq.ft.

Advanced Circuits
Aurora Division
Corporate Headquarters
21101 E. 32nd Parkway
Aurora, Colorado 80011
162,000 sq.ft.



Certifications and Approvals

Aurora Division
ISO 9001:2008
AS9100:2009C
MIL-PRF-55110G Types 1, 2 and 3
ITAR Registered
UL Registered

Tempe Division
ISO 9001:2008
AS9100:2009C
MIL-PRF-31032
MIL-PRF-55110G Types 1, 2, and 3
ITAR Registered
UL Registered

Maple Grove Division
ISO 9001:2008
AS9100:2009C and AS9104A
MIL-PRF-31032
MIL-PRF-55110G Types 1, 2, and 3
JCP Registered
ITAR Registered
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DOD Contracts

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