



**How your choice in components
drives Design, Materials &
Manufacturing**

Streamline Circuits Facility



Located in Silicon Valley

- **Manufacturing all levels of technology**
 - Time sensitive prototyping through production
- **The facility was established in 1982**
 - New management team installed September 2003
- **56,000 sq ft PCB manufacturing facility**
 - Complete manufacturing process under one roof
- **1 mile from the San Jose Airport**
 - Delivery convenience for out of state customers
- **Located in Silicon Valley**
 - Short car ride away for pick up & deliveries
- **Financially secure in current market conditions**
 - Low cost infrastructure

The Team & Their Experience

- **Chuck Dimick- CEO | Founder**
 - Over 33 years of experience in PCB manufacturing. Former CEO of Dynamic Details Inc. and founder of the company's predecessor, Dynamic Circuits Inc. (1991)
- **Greg Halvorson- President | Founder**
 - Over 31 years of experience in PCB manufacturing. Former VP of Operations of Dynamic Details Inc. and Dynamic Circuits Inc.
- **Tom Doslak-Vice President of Sales & Marketing | Founder**
 - Over 23 years of industry experience. Former Director of Sales for Braztek Intl. and Western Regional Sales Manager for Dynamic Details Inc.
- **Ed Pitney- Operations Manager**
 - Over with 32 years of PCB manufacturing experience. Ed spent his early career with NTI Inc. as a Director of Manufacturing Operations later purchased by DDI Global Inc.
- **Steve Morris – Director of Engineering**
 - Over 27 years of PWB Design & Engineering experiencing. Former VP of Advanced Technology for Multek (a division of Flextronics) and a key member of the HP PWB Corporate commodity team.
- **JR Ramirez- Production Manager | Founder**
 - Over 32 years of experience in the industry. Former Production Manager for both Dynamic Details Inc. and Dynamic Circuits Inc.
- **Lorraine Hook - Director of Quality**
 - Over 43 years of industry experience. Former Director of Quality for many successful companies including DCI and DDI. She has held dual positions as Corp. Quality Systems Manager.

A Full PCB Solution

- **Multilayer Rigid / Rigid- Flex / Flex**
- **50 + Layers**
- **28:1 High Aspect Ratio**
- **3.23 Mils Hole to Copper**
- **Buried / Blind Vias**
- **9 Sequential Laminations**
- **13+ Stacked Vias**
- **1 Mil Trace & Space**
- **Cavity Constructions**
- **6 oz. + Copper Thickness**
- **Copper Filled Micro Vias**
- **+/- 5% Controlled Impedance Tol.**
- **AS9100 Rev. C / ISO 9001**
- **Mil-Spec 55110 / ITAR**
- **RoHS & Halogen Free Materials**
- **IPC 6012 Rigid / 6013 Flex / 6015 MCM / 6016 HDI / 6018 High Frequency**
- **4 Mil Mechanical Drills**
- **24" x 30" Oversize Panel**
- **2 Mil Laser Drill Vias**
- **Up to 345 Mils Board Thickness**
- **Via Under Pad (Conductive & Non-Conductive Filled)**
- **40+ Materials (Hybrid Constructions)**

Today's Component and Packaging Descriptions

- **BGA Pitch:** 1mm, .85mm, .65mm, .5mm, .4mm, .25mm
 - Very high pin count
 - Lead Free
 - Combined Pitch on Interposer Designs
 - Filled Via, Micro Via
- **Chip on Board**
 - Wire Bond Chipsets
 - Combining Bonding and Soldering Requirements
- **Ultra Thin Packaging**
 - Cavities
 - Ultra thin dielectrics
 - Ultra thin copper layers
- **High Speed Low Loss, Combined High Speed, RF Technologies**
 - Material Limitations
 - Cost restrictions
 - Reduced tolerances for etching and dielectrics

Current Technology US Industry

	<u>75% Board shops</u> <u>Standard</u>	<u>15% Board shops</u> <u>Emerging</u>	<u>10% board shops</u> <u>Advanced</u>
Layers	6	12	18 & up
Trace/Space	5	4	2 & Below
Min PLT Hole (Mech)	11	8	4
Aspect Ratio	10:1	14:1	28:1
Min Laser Hole size	No Equip	4	2
Mult Lam Cycles	2	4	8 & up
Fastest Turn (14 Layers)	7 Days	4 Days	24 Hours
LDI Imaging	No Equip	60%	100%

Current Status of the US Industry

- Approximately 230 shops left in the country
 - Estimates say there will be less than 150 by 2014
- Most are using out dated equipment and need to modernize
 - They rely heavily on industry Veterans (John, The X-Factor) for key processes, limiting productivity
 - (Industry Veterans are very expensive, if you can find enough of them)
- Feel pressure from offshore competition, eroding prices

The Decision time is approaching

- As a business owner, “What Do I Do ???”
 - A: Look for new market segments, Military, ITAR, Flex Rigid
 - » All are costly changes to make, require Capital investment
 - B: Close down the business

Removing the X factor

How Do You Remove X-Factor?

People – Process - Equipment

- **Must use advanced equipment, automation, and technology to manufacture today's printed circuit board requirements**
 - **The future in PCB manufacturing is about equipment and automation (allows for 24/7 operations)**
- **Trained equipment operators = lower Labor costs**
 - **Remove John, industry veteran from the floor**
- **Build low, medium and high tech to balance shop loading**
- **Reinvest into the future: 10% of sales per year minimum capitalization, Investing into shops future**



Incorporating HDI Solutions



Via Capabilities

Smallest Mechanical Via - .004"

Smallest Laser Via- .002"

Stacked Vias (Any layer)

Flip Drill for legacy Designs

Positional Tolerance .0005

Benefits of HDI



**Creating a Technology Platform for
Current & Future Fine Pitch Devices**

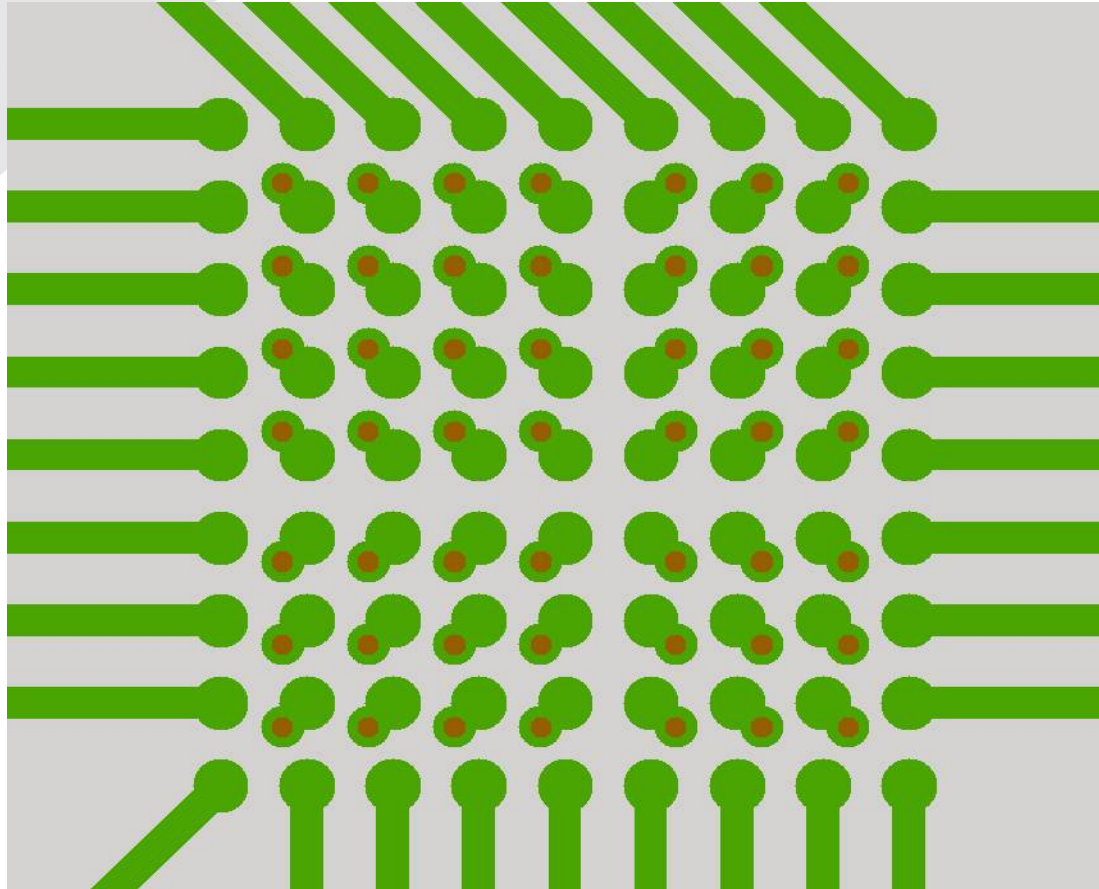
**Provide Designers Additional
Options**

**Reliable/Robust Mfg.
Process**

Improved Quality

Improved Route Channels

Teardrop Vias

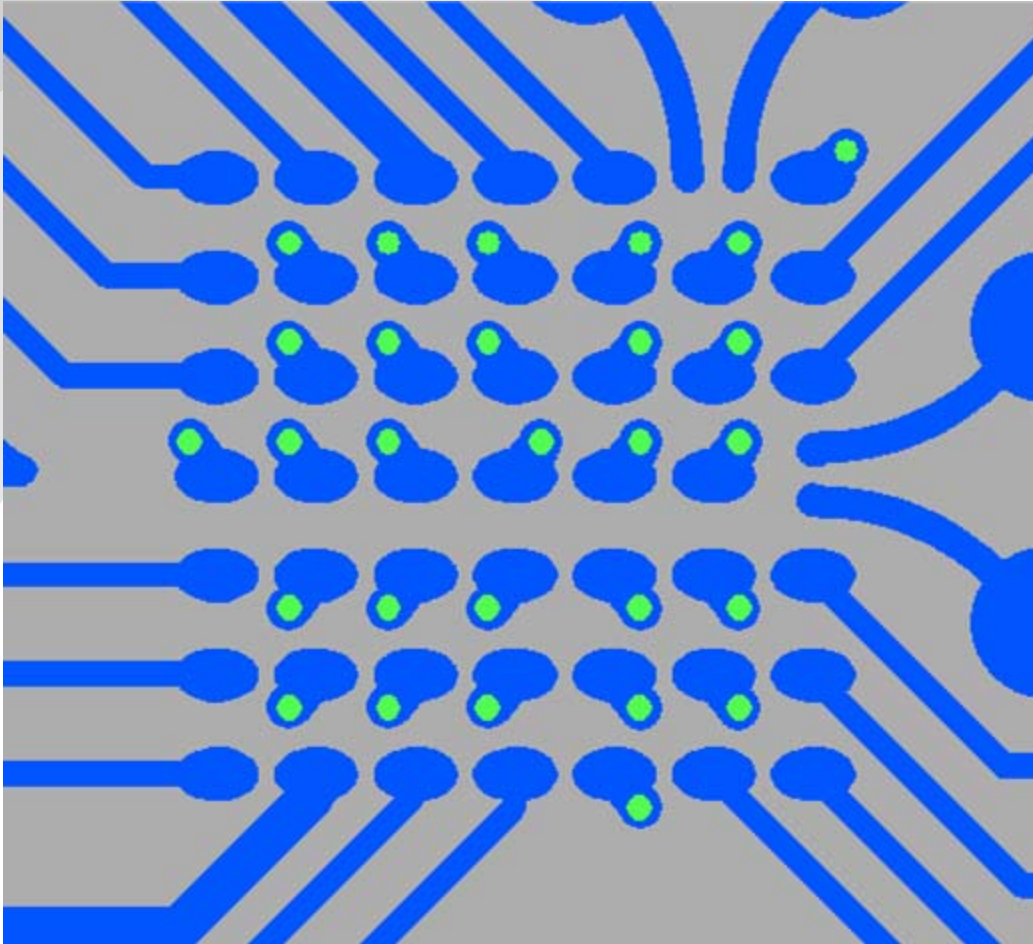


Contact Pad
.25mm/.0098"

Via Pad
.2mm/.008"

Line width
.15mm/.006"

Snap Shot Actual .4mm



Outer Layer With Quadrant
Dog bone

DUT Pad .25mm

Via Pad .2mm

Laser Via .125mm

Trace

.1mm, .125mm, .175mm

Conclusions

Stacked Vias or Dog Bone

Increase DUT Sizes & Sites

Wider Conductors

Wider Space

Reliability / OTD

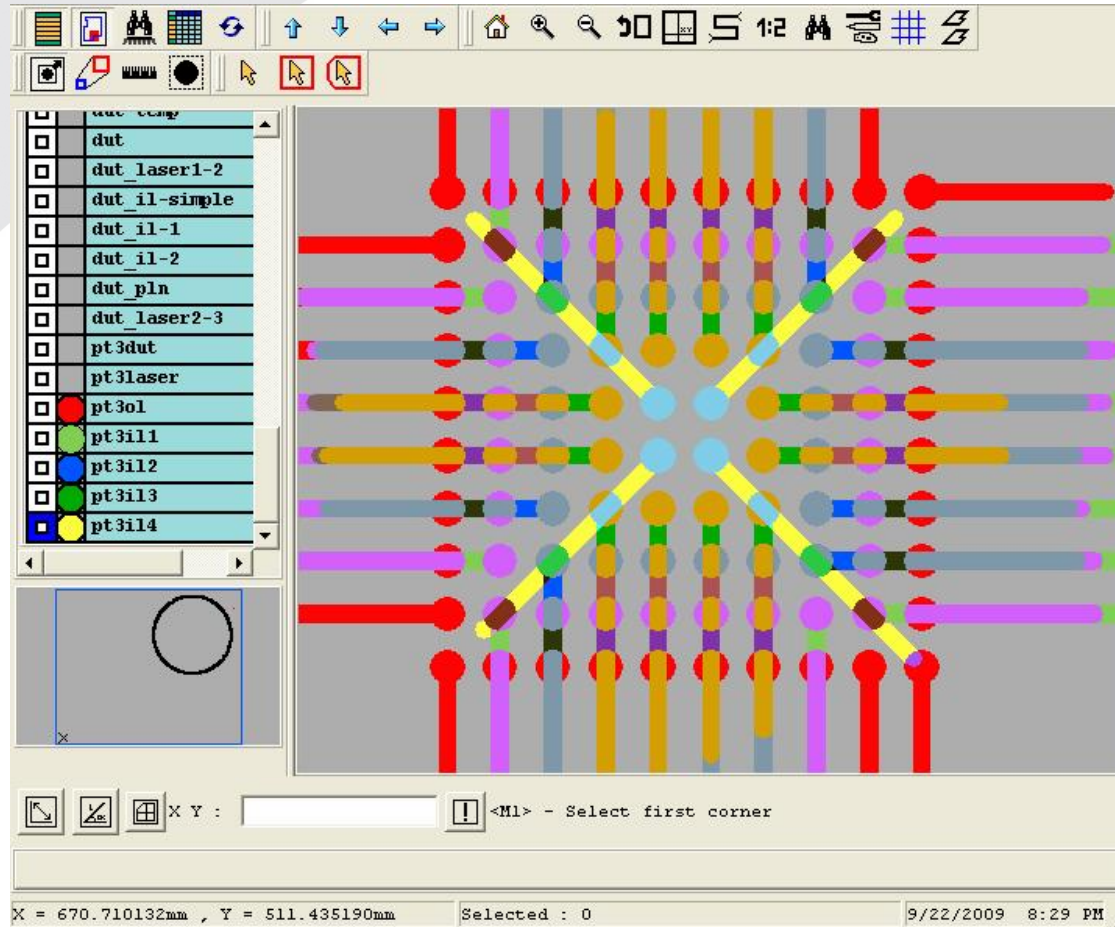
.3mm DUT

Outer Row Routing Only

Stacked Laser Vias

No Mechanical Drill (In DUT)

All Routes for .3mm Device



Advanced Technology

.19mm Design for Manufacturability
.0075mils center to center

Recommended pad sizes, line widths and laser drill sizes

- External pad size .005
- Internal pad size .005 - .004
- Internal line widths .0019 - .0015
- Laser drill size .002 - .0034

Cross Section Pictures
Device pin count 2500
.225 mm pitch device

Outer layer cross section view

Surface finish ENIPIG

Laser drill finished hole size

0.00342 in

Laser via copper filled

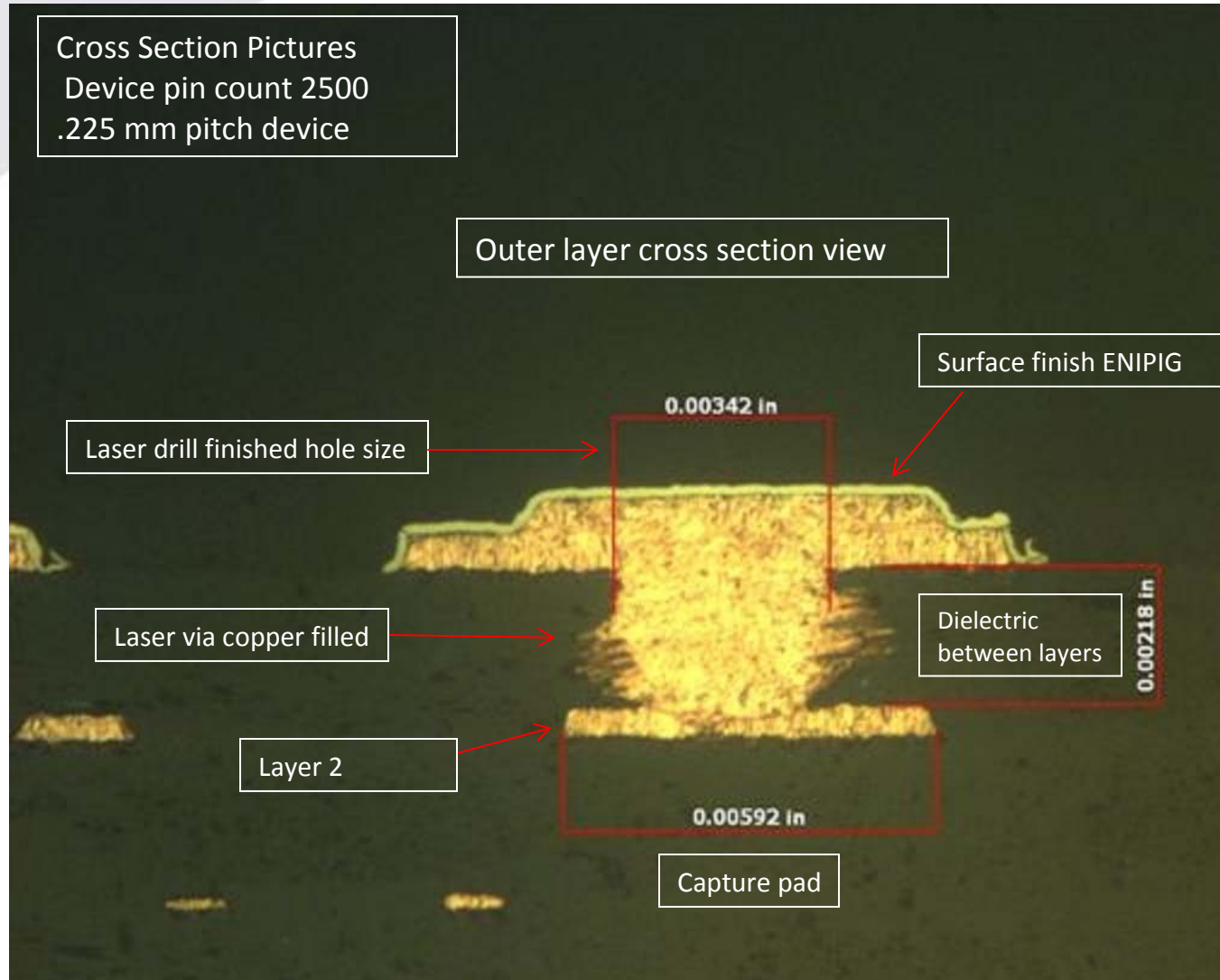
Layer 2

Dielectric between layers

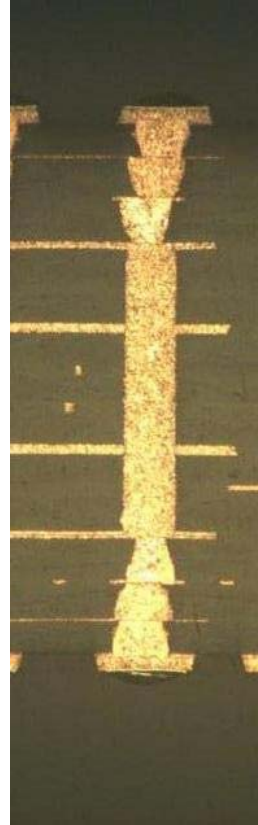
0.00218 in

0.00592 in


Capture pad

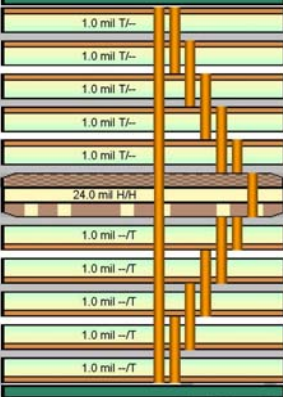


Copper Plated Vias



*** Valued Customer: If this stackup is accepted, please add this PDF to the production data package. ***

Job number: 88372_SAMPLE	Material: Mixed, MEGTRON-57	External Stackup Report 
Part number:	Impedance: Yes	
Customer: STREAMLINE CIRCUITS	Date: 31-Jul-2013	
Panel size: 12X18	Created by: Dennis McLaurin	

Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment	Glass Style	Material Family	Dielectric constant @ 1GHz	Thickness After lamination (mil)
Soldermask										
1	Signal	T	11	1.0 mil T/-		RCF	ZTC2	ZETA	3.40	0.80
2	Mixed	T	73	1.0 mil T/-		RCF	ZTC2	ZETA	3.40	1.45
3	Plane	T	74	1.0 mil T/-		RCF	ZTC2	ZETA	3.40	1.00
4	Plane	T	74	1.0 mil T/-		RCF	ZTC2	ZETA	3.40	0.65
5	Signal	T	8	1.0 mil T/-		RCF	ZTC2	ZETA	3.40	1.00
6	Mixed	H	22	24.0 mil H/H		Core	5-2116	MEGTRON-5775	3.71	1.20
7	Signal	H	7			24.0 mil H/H	Core	5-2116	MEGTRON-5775	3.71
8	Signal	T	6	1.0 mil -/T		RCF	ZTC2	ZETA	3.40	1.20
9	Plane	T	74	1.0 mil -/T		RCF	ZTC2	ZETA	3.40	1.00
10	Mixed	T	60	1.0 mil -/T		RCF	ZTC2	ZETA	3.40	0.65
11	Plane	T	71	1.0 mil -/T		RCF	ZTC2	ZETA	3.40	1.00
12	Signal	T	17	1.0 mil -/T		RCF	ZTC2	ZETA	3.40	0.65
Soldermask										

Specification (Over mask on plated copper):	mil
Overall Board Thickness:	52.0
Tolerance:	+5.2/-5.2
Min-Max Board Thickness:	46.8-57.2

Anticipated Board Thickness:	mil
After lamination:	42.50
Over mask on plated copper:	46.10

Grain in 18" Dimension

Impedance Table

Layer	Impedance Requirement [ohms]	Tolerance [ohms]		Type	Upper Reference	Lower Ref	Designed Line Width [Mil]	Designed Spacing [Mil]	Finished Line Width [Mil]	Finished Spacing [Mil]	Impedance Simulation [ohms]
		+	-								
2	100	10	10	Differential	4	3	4.875	5.13	4.5	5.50	54.348
5	104	10.4	10.4	Differential	4	9	2.25	2.75	2.25	2.75	78.085
5	99	9.9	9.9	Differential	4	6	2.75	7.25	1.75	8.25	71.052
6	112	11.2	11.2	Differential	4	9	2.375	2.63	2.375	2.63	100.616
7	112	11.2	11.2	Differential	9	4	2.375	2.63	2.375	2.63	100.616
8	104	10.4	10.4	Differential	9	4	2.25	2.75	2.25	2.75	78.085

Remarks

* Any targeted thickness .0046" and greater shall have a minimum tolerance of +/- .001 after lamination.
 * Any targeted thickness .0045" and below shall not be held to the minimum dielectric .0035429" as specified in IPC-6012 section 3.6.2.15. Unless agreed upon in writing from Streamline Circuits Inc. The minimum thickness per this exception shall not be less than .0009839" per IPC-6012 section 3.6.2.15.

**PWB INTERCONNECT SOLUTIONS.
RELIABILITY TESTING**

IST TEST RESULTS

23 June 2013

Job Number j13_4334
Lot Number Tool # 00372
Customer Integral Technology
Cage Code # N/A
Coupon Rec 4
Customer Req 4

Test Cycles 1000
Test Temp 150°C
Coupon Type Stacked MV
Test Vehicle # SL12042A
Incoming Tested 4
Part # P12230A

Precon Cycles 6
Precon Temp 230°C
Test Runs 1
Date Code: 2113
Coupons Passed 4
WO # N/A

Conclusions:

Coupons proved to be very robust under set IST test parameters.
 Capacitance measurements reveal no material degradation.
 Recommend performing a microsection to verify these findings.

TEST RESULTS

Coupon ID	Pwr Cycles	Pwr %	Sen Cycles	Sen %	Results
1	1000	1.7	1000	1.8	Accept
2	1000	1.1	1000	1	Accept
3	1000	1.2	1000	1	Accept
4	1000	2.1	1000	2	Accept
					Cus Spec
Mean	1000	1.5	1000	1.5	N/A
Std Dev	0	0.5	0	0.5	N/A
Min	1000	1.1	1000	1	N/A
Max	1000	2.1	1000	2	
Range	0	1.1	0	1	

RELIABILITY TESTING

IST TEST RESULTS

20 June 2011

Job Number Zeta	Test Cycles 500	Precon Cycles 3
Lot Number	Test Temp 150	Precon Temp 220
Customer	Coupon Type Zeta 2+2+2	Fail Method: A and B
Cage Code #	Test Vehicle #	Date Code: 1811
Coupon Rec 2	Incoming Tested 2	Coupons Passed 2
Customer Req N/A	Part # 600-2019-142 A	WO #

TEST RESULTS

Coupon ID	Pwr Cycles	Pwr %	SenseA Cycles	SnsA %	SenseB Cycles	SnsB %	Results
08-17	500	-0.4	500	-0.4	500	-0.4	Accept
09-17	500	-0.5	500	-0.6	500	-0.4	Accept
							CusSpec
Mean	500	-0.4	500	-0.5	500	-0.4	N/A
Std Dev	0	0.1	0	0.1	0	0	
Min	500	-0.5	500	-0.6	500	-0.4	N/A
Max	500	-0.4	500	-0.4	500	-0.4	N/A
Range	0	0.1	0	0.2	0	0	
Coef Var	0%		0%		0%		N/A

PREScreen RESULTS

Coupon ID	Power	SenseA	SenseB
08-17	1130	455.6	539.7
09-17	1128	438.5	514.1
Mean	1129	447	527
Std Dev	1	12	18
Min	1128	438	514
Max	1130	456	540
Range	2	17	26
Coef Var	0%	0%	0%



Advanced Materials

High Speed Materials Website Page



The screenshot shows a web browser window displaying the 'High Speed Materials' page on the Streamline Circuits website. The browser's address bar shows the URL www.streamlinecircuits.com/Materials/high-speed-materials.html. The website header features the Streamline Circuits logo and a red call-to-action button that reads '~ CALL TODAY ~ 1-877-264-0343'. A navigation menu includes links for Home, Company, Capabilities, Engineering Support, Customer Support, Request a Quote, and Contact Us. The main content area is titled 'High Speed Materials' and 'Next Generation'. It features three product sections: **ARLON** (with sub-sections AD250C, AD255C, and CLTE-XT), **EMC** (with sub-sections EM-355(D), EM-828, and EM-888), and **ITEQ** (with sub-sections IT-150DA and EM-828). Each section includes technical specifications like Dielectric Constant (DK) and Dissipation Factor (DF), and a 'Product Summary' link. A 'More' link is provided for each section. On the right side, there is a 'TECH SUPPORT' sidebar with links for 'Request Stackup', 'Request Info', 'Request a Quote', and 'Contact us'. The Windows taskbar at the bottom shows the Start button, open applications (Microsoft Outlook, Presentations, High Speed Materials...), and the system tray with the time 4:23 PM.

High Speed Materials | Materi x

www.streamlinecircuits.com/Materials/high-speed-materials.html

Pyralux® TK 185018R - DK: 2.5, DF: 0.002 Product Summary
Pyralux® TK 187518R - DK: 2.3, DF: 0.002 Product Summary
Pyralux® TK 1810018R - DK: 2.5, DF: 0.002 Product Summary

[More](#)

MCL-HE-679G/THETA C - DK: 3.9, DF: 0.0009 Product Summary

[More](#)

Zeta Cap - DK: 3.0, DF: 0.005 Product Summary

[More](#)

I-SpeedIS - DK: 3.3, DF: 0.006 Product Summary
I-TeraMT - DK: 3.0, DF: 0.0035 Product Summary
IS680-280 - DK: 2.8, DF: 0.0025 Product Summary

[More](#)

9208 - DK: 2.08, DF: 0.006 Product Summary
9217 - DK: 2.17, DF: 0.008 Product Summary
9220 - DK: 2.20, DF: 0.009 Product Summary

[More](#)

start | Microsoft Outlook | Presentations | My Pictures | High Speed Materials ... | top of HSM pg - Paint | 4:25 PM

Panasonic

Megtron4/ R-5725 - DK: 3.8, DF: 0.005 Product Summary
Megtron6/ R-5775 - DK: 3.7, DF: 0.002 Product Summary
Megtron6/ R-5775(N) - DK: 3.4, DF:0.0015 Product Summary

[More](#)



RT/duroid 5870 - DK: 2.33, DF: 0.0012 Product Summary
RT/duroid 5880 - DK: 2.20, DF: 0.0009 Product Summary
RT/duroid 5880Z - DK: 1.96, DF: 0.0027 Product Summary

[More](#)

TACONIC

TLA - DK:2.62, DF: 0.0012 Product Summary
TLX - DK: 2.45, DF: 0.0015 Product Summary
TLY - DK: 2.20, DF: 0.0009 Product Summary

[More](#)



Taiwan Union Technology Corporation

ThunderClad 2 - DK: 3.8, DF: 0.0065 Product Summary
TU-872 LK Sp - DK: 3.5, DF: 0.008 Product Summary
TU-872 SLK Sp - DK: 3.5, DF: 0.008 Product Summary

[More](#)



VT-464 - DK: 3.35, DF: 0.012 Product Summary
VT-464(M) - DK:3.35, DF: 0.012 Product Summary

[More](#)

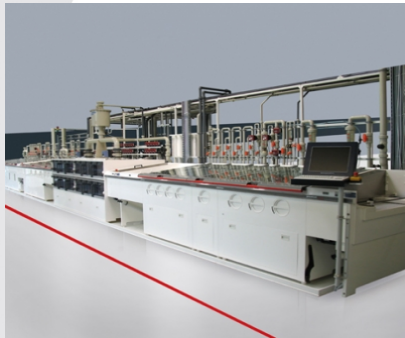
Equipment Mix Required for Today's Technology



Laser Direct Imaging



Cuposit & Electroless Line



DES Inner Layer Stripline

Fabricators must:

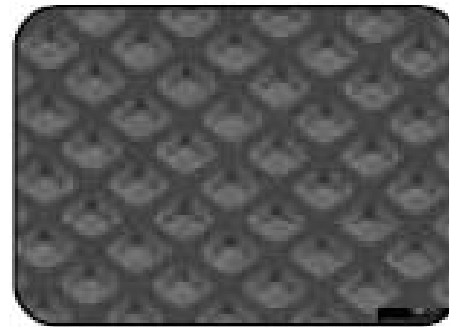
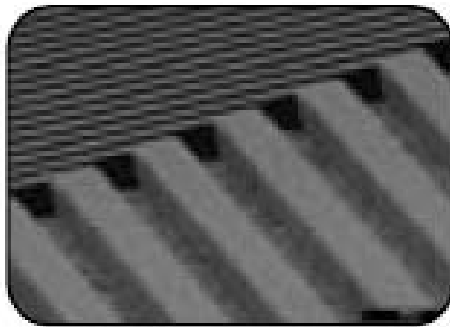
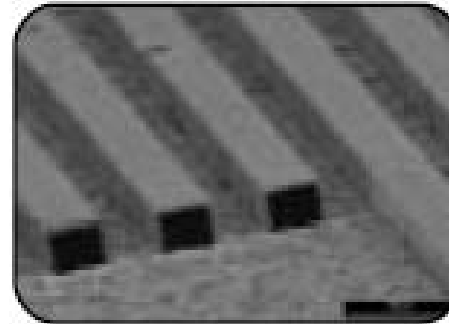
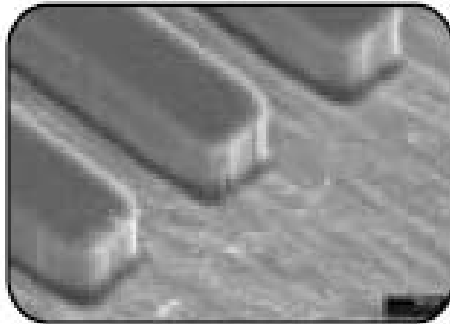
- Use advanced equipment technologies to manufacture today's printed circuit board requirements
- The future in PCB manufacturing is about technology and automation
- Hire and Train specialized equipment operators
- Retain a high percentage of engineering personnel and staff level technicians

LDI (Laser Direct Imaging) Orbotech Paragon SM20



LDI Imaging Systems

**Example of 25 micron
(.001" Trace and Space)**



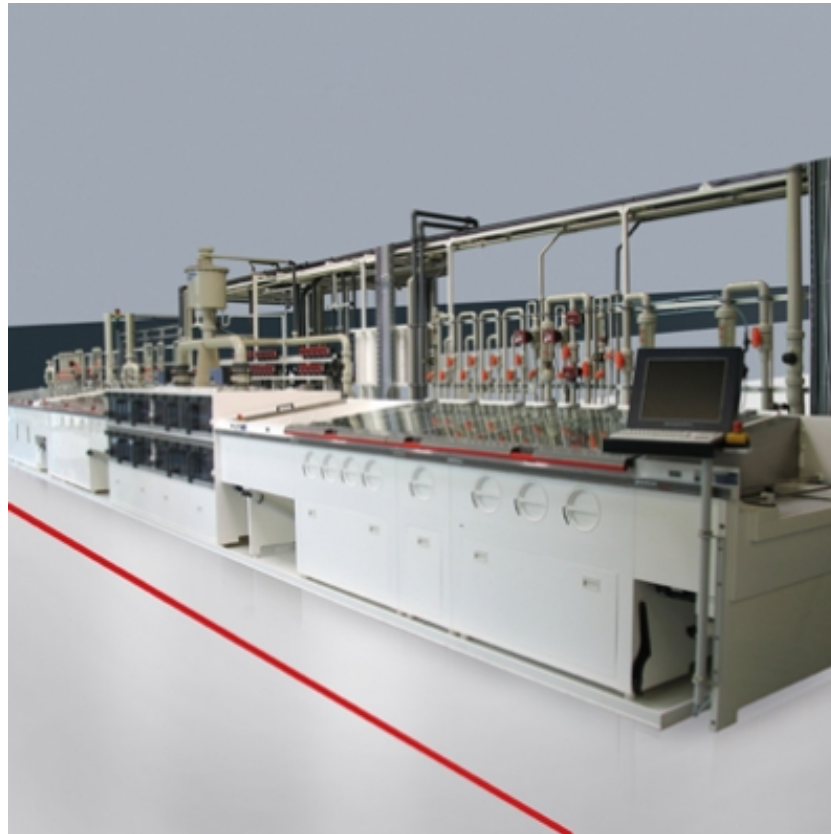
25 μ m features exposed by Paragon

LDI Imaging Systems:

- **100% Laser Direct Imaging (LDI)**
 - Repeatabile process, computer controlled
 - 24/7 consistent imaging regardless of shift
 - No film means lower tooling costs
 - No repeating defects
- **Consistent trace width**
 - Tighter impedance control (+/- 5 %)
 - ¼ Mil Accuracy .0008 Min Line/.0005 Space
 - Layer to layer registration within .0004”
 - No film growth due to heat expansion

Streamline is currently one of two companies in North America with 4 installations in-house

SCHMID Precision DES Line (Develop – Etch – Strip)



Inner Layer Develop Etch Strip:

- January 2013 state of the art Schmid DES line Installed
 - Computer controlled for consistent product
 - Full automation removes human element (X-Factor)
 - 2 Micron variation over panel
 - 1 mil core capability for substrate, HDI, and Rigid flex
 - 4,000 Cores per day capacity based on current copper mix
 - Tripled capacity upon installation
 - Positions Streamline for future technologies

Precision Laser Drilling

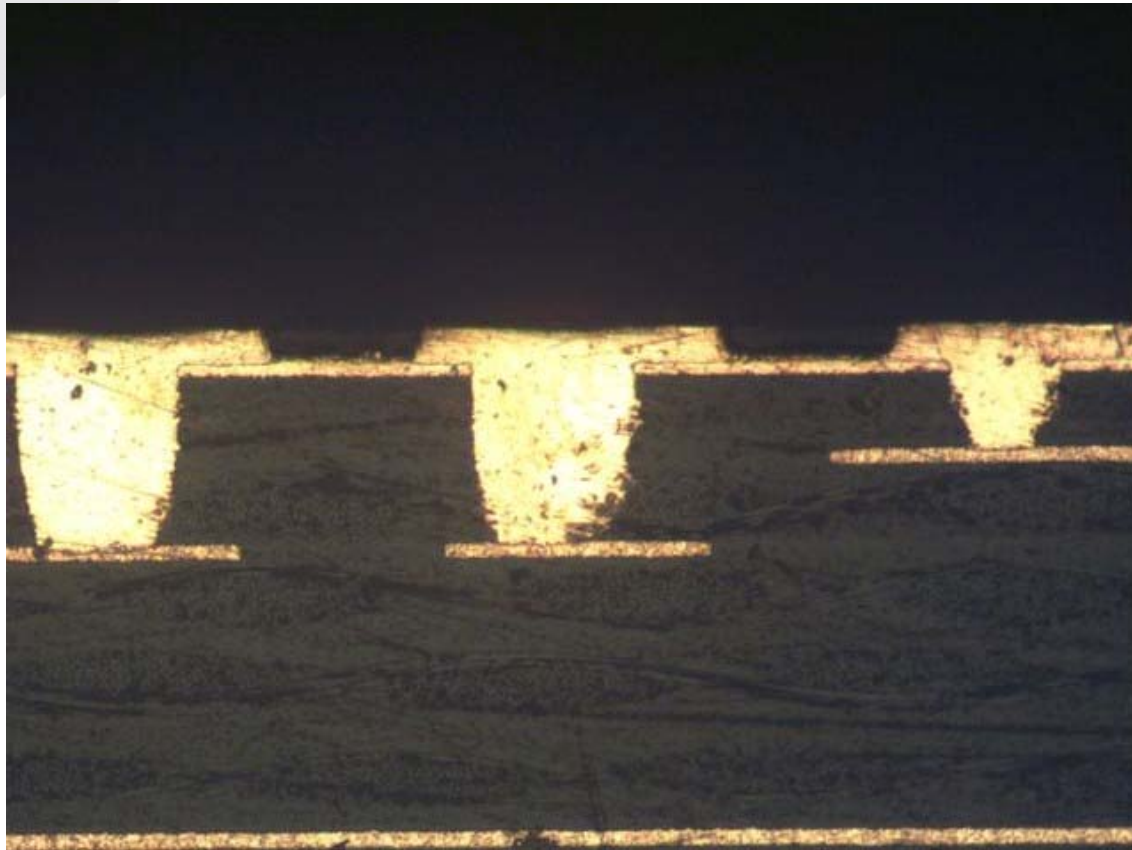
6 High Speed Laser Drills



Laser Drilling

- 6 Laser drills in house (7th has been purchased)
 - Daily processing 4-N-4 of means experience
 - Higher stacks available
 - .0014” Hole, .004” Pad advances technology window
 - Aspect Ratio: 3:1
 - Positional Accuracy for Hole Location +/- .0005”

Via formation, Aspect ratios and Stacked vias for Increased Densities



IPS Automatic Electroless Plating Line



Electroless Processing:

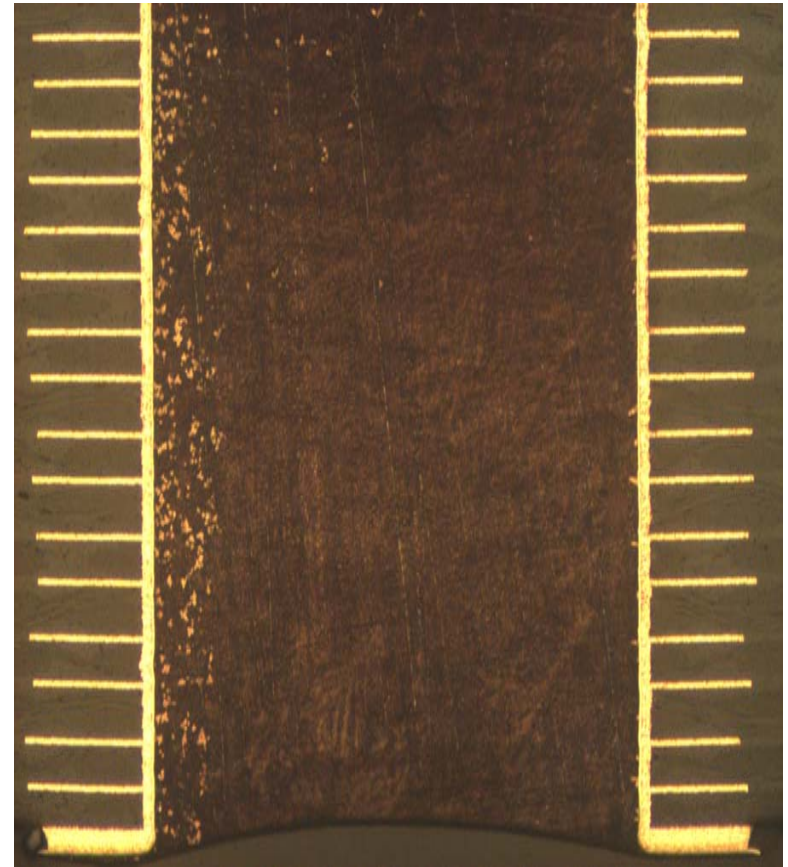
- Completely Automated Line installed January 2012
 - Industry leading 28:1 Aspect Ratio: allows for higher density designs
 - Bar coded processing removes operator errors (X-Factor)
 - Dwell times established in planning for speed & efficiency, translating to consistent product (X-Factor)
 - Ultrasonic, knife edge agitation, vibration & thumper
 - 36 stations, Oversized tanks (24" x 30" Panels)
 - High volume throughput capability

Pluritec Inspecta X-ray Registration System



Internal Registration

- In unison with “Xact Software” for scaling
- Internal Registration is one of the key attributes in being successful
- X-Ray allows verification in real time
- X-Sections Verify X-Ray



Xact Scaling Report

Work Order: None Tool Number: None User Name: None Batch Code: 101067-01.02 Batch Date: Sep 12, 2012 03:49:00

Pass

OK to drill without modification

X-Ray Machine

Minimum Land (mil)

Drill To Copper (mil)

Remaining A/R Req'd (mil)

Drill Diameter

Nominal Drill Compensation

Symbols

Post-Etch Punch

Top Left (mil)

Top Right (mil)

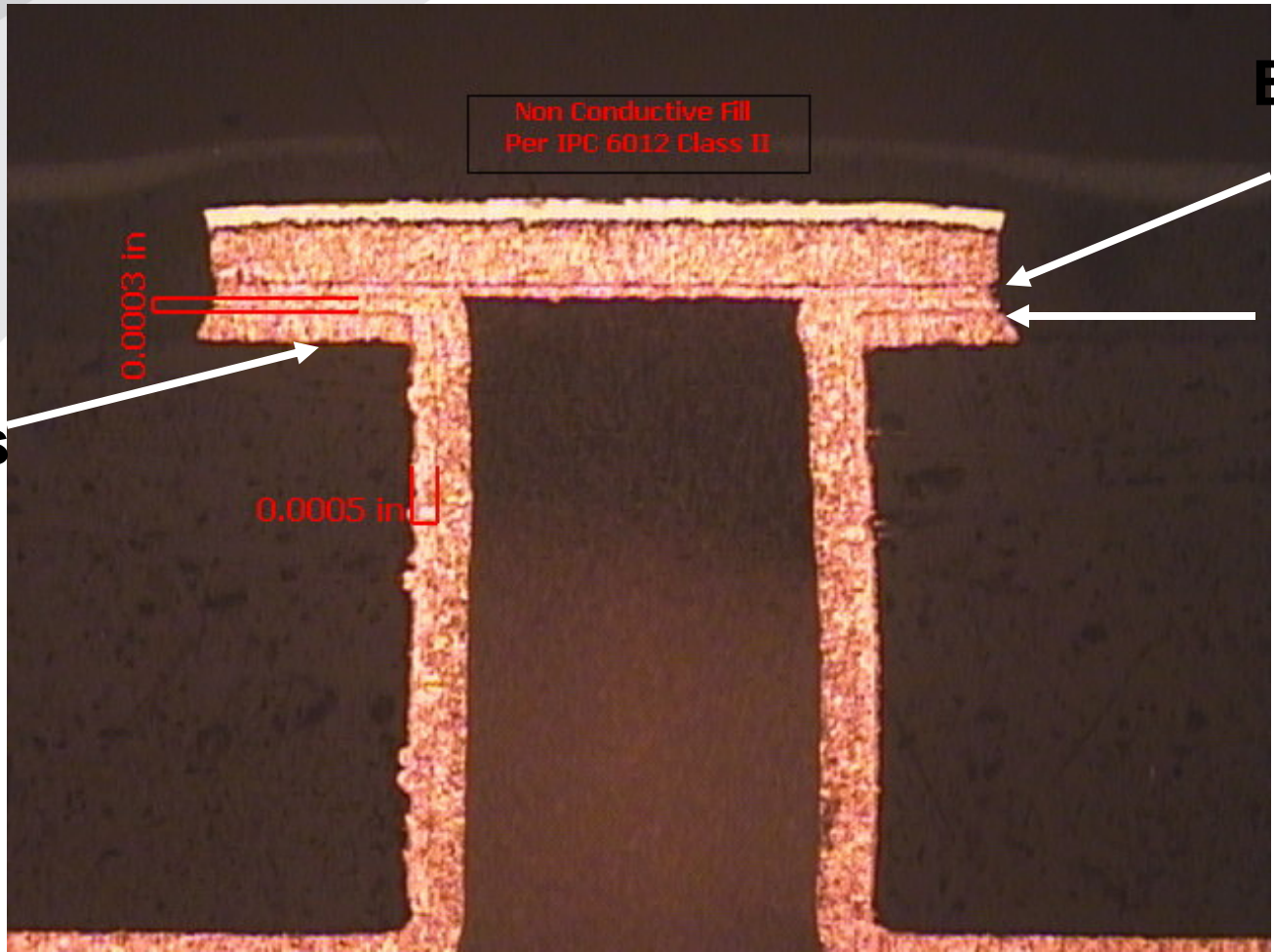
Bottom Left (mil)

Bottom Right (mil)

Drill Compensation | Panels | Layers

Scale Errors (mil/inches)		
All	Short	Long
■ Common	0.073	0.203
▲ L02	0.091	0.223
▼ L03	0.079	0.251
● L04	0.087	0.178

Non Conductive Filled Via Wrap Per IPC 6012 Class III

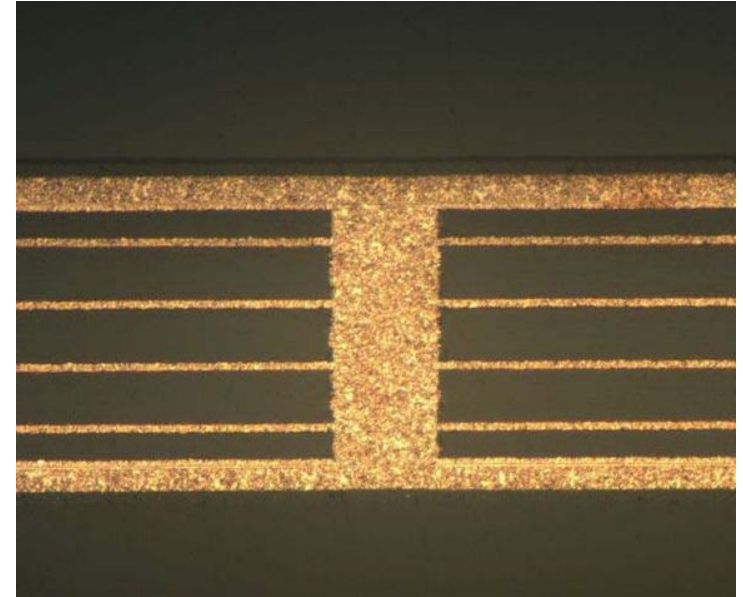
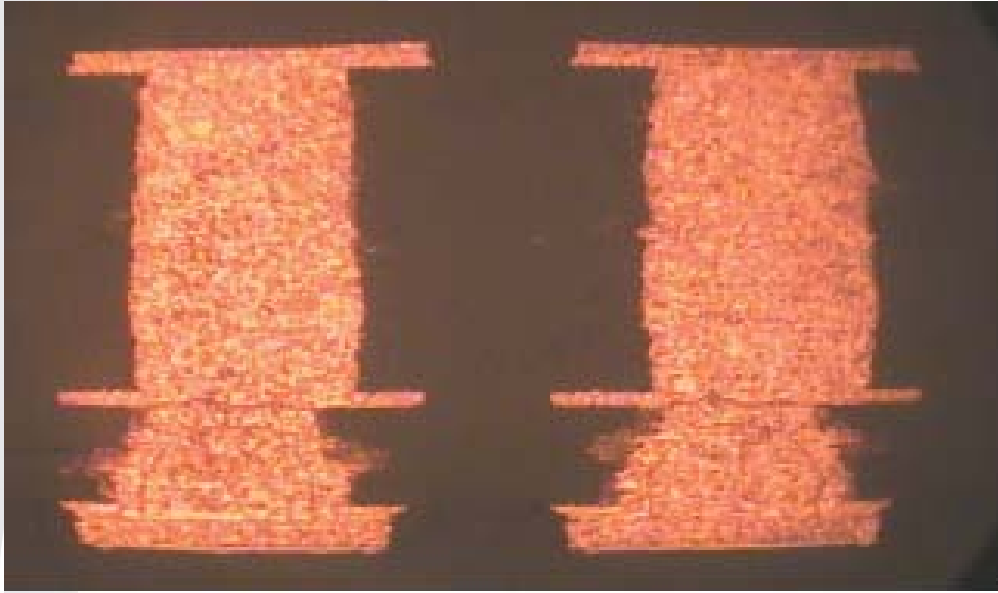


**Electroless
Wrap**

**Smooth
Copper**

**Dendrites
(Teeth)**

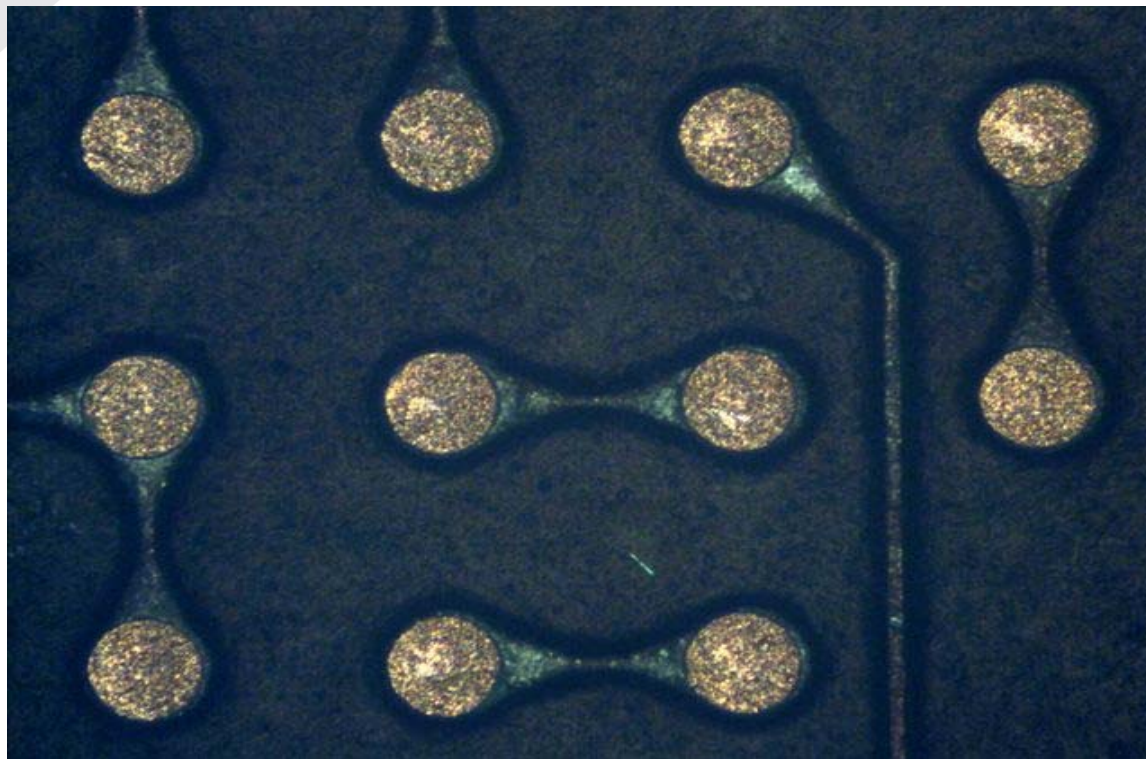
Copper Fill Laser Vias & Through Hole Solid Copper Vias



Thermal Via Farms for Thermal Management

Chip Scale Packaging

- **Chip Scale Packaging Requires Streamlines Equipment Sets for
Success-100% LDI**



LSMDP

Laser Solder Mask Defined Pad Using the LDI's

- Precise Imaging to .0005” clearance
 - Allows reduced solder mask clearance sizes
 - May reduce layer count
 - Maximize geometry
 - Using laser solder mask defined pad (LSMDP)
 - You can define a “Pad” on top of a pad

Ink Jet Silkscreen Orbotech Sprint-8™



Ink Jet Silkscreen

- **“Now Engineers can actually read to debug!”**
 - Ultra Fine Crisp Lines, Down to 3 mil
 - Serialization on the fly, BAR Code & QR codes
 - Applied over partially cured mask providing for the mask and legend to be cure simultaneously to reduce cycle time
 - Combination inkjet and laser technology
 - Dries the ink as it is applied

Everret Charles Flying Probe Testing



Test Capabilities:

- **100% Flying probe testing (8 Systems)**
 - **Flexibility, no fixtures, less cost**
 - **Allows for testing sub chapters before final book**
 - **Everett Charles Eliminator for faster testing**
 - **Every board 100% Net List Tested**

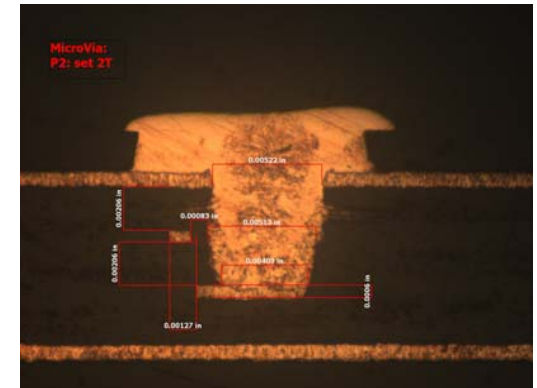
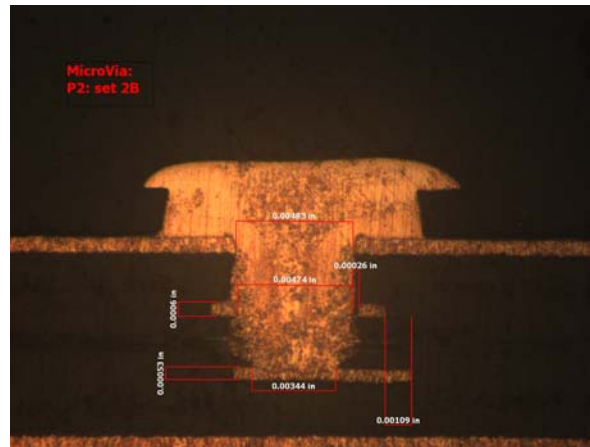
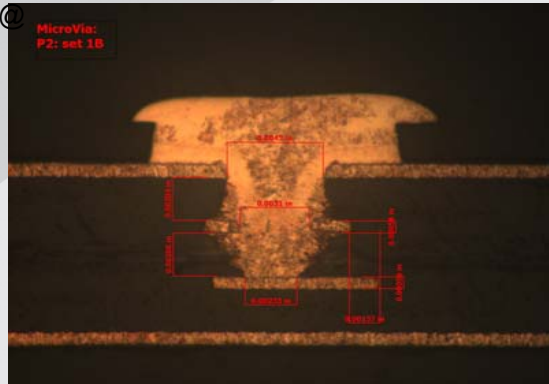
Surface Finishes:

- **HASL: Hot Air Solder Level**
- **ENIG: Electroless-Nickel Immersion Gold**
- **IS: Immersion Silver**
- **ENEPIG: Electroless-Nickel Electroless-Palladium Immersion Gold**
- **OSP: Organic Solder Preservative**
- **Soft Gold**
- **Hard Gold**
- **IT: Immersion Tin**

Developing Technologies for Speed and Cost

- New Via Formation Manufacturing Techniques
- Film Based Materials
- Conductive Pastes for Filling and Interconnects

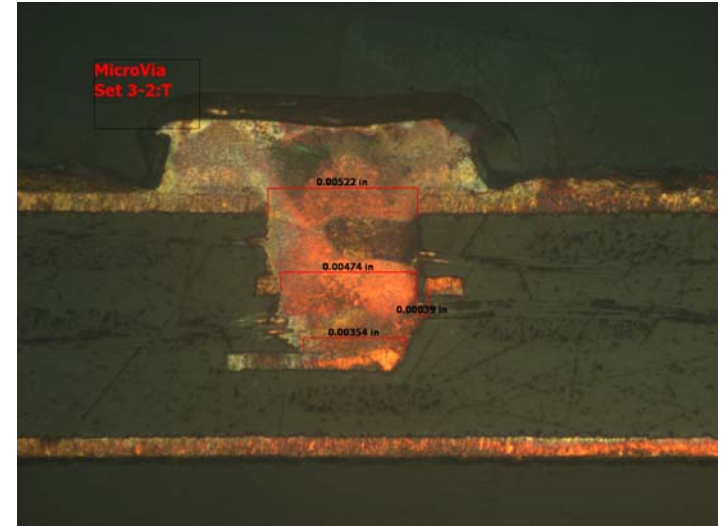
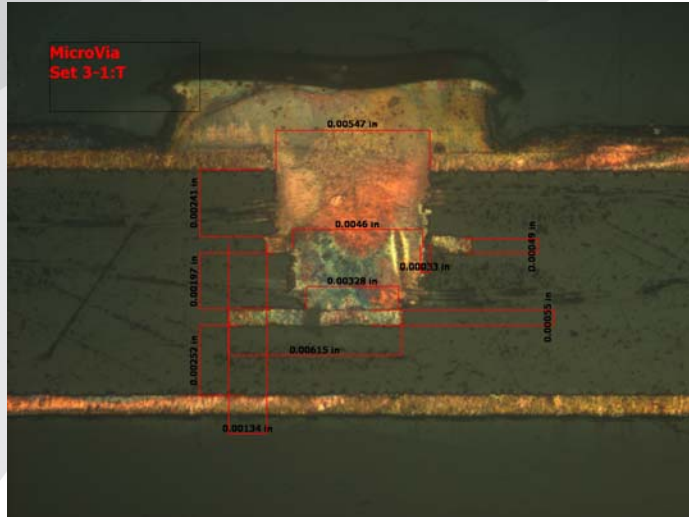
Type 1: Solid .008 pad



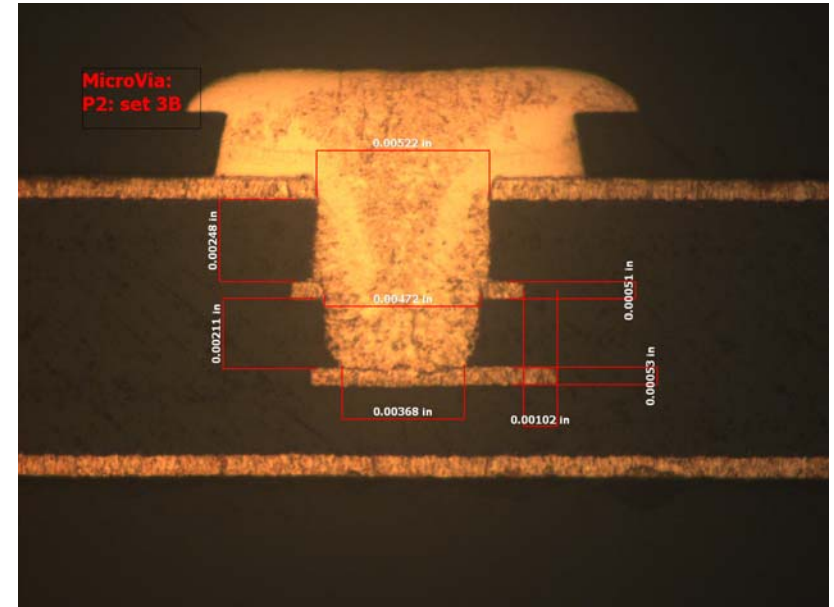
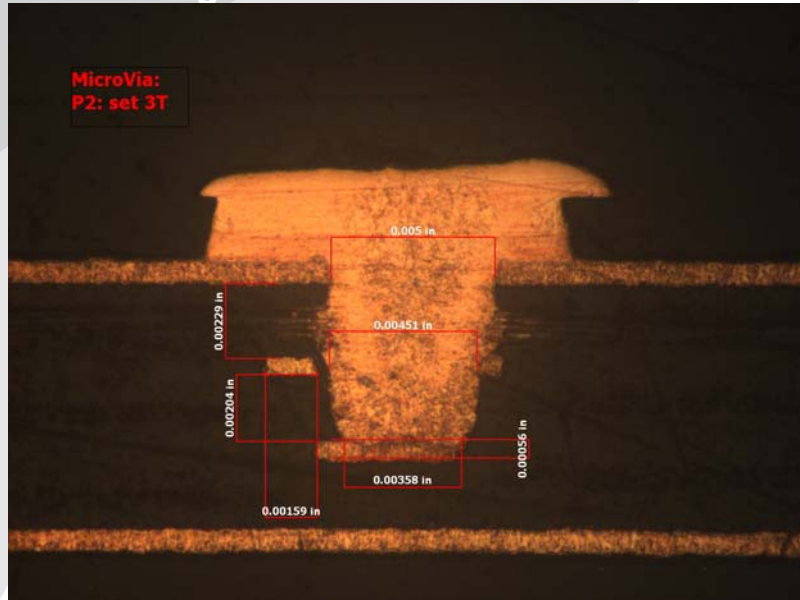
The laser beam was able to penetrate through the solid copper on layer 2; however the amount of energy it took to through the second layer began to reflect off the layer itself which in turn began to vaporize. As a result, the resin around layer 2 was removed and the via formation appeared balloon shaped. Thus, the via formation was borderline in acceptability.

**PATENT
PENDING**

Type 2: .008 x .0045



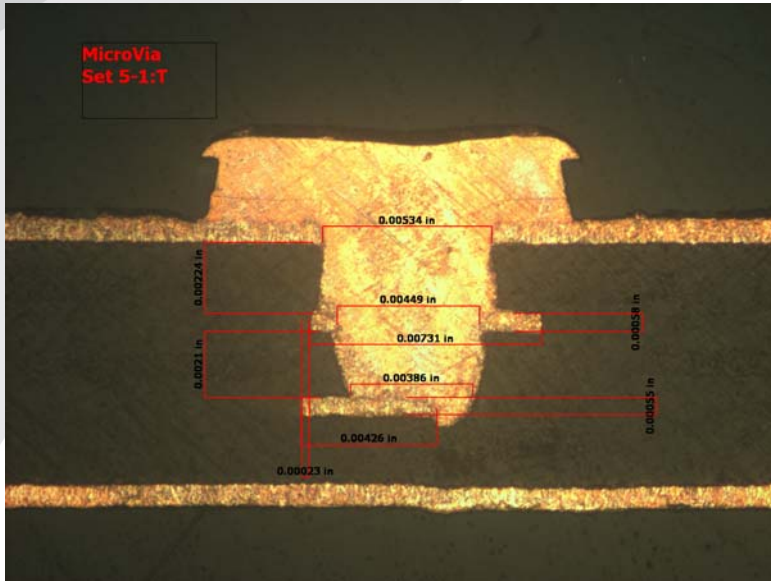
**PATENT
PENDING**



The laser beam was able to penetrate through the partial copper on layer 2; however the formation of the via was unacceptable because there was a visible gap between the edge of the via to the edge of the pad on layer 2. The gap could be attributed to etching of the inner and/or the registration between the laser and pad.

**PATENT
PENDING**

Type 4: .008 x .0035



**PATENT
PENDING**

Film Based Dielectrics

- Thinner layer to layer spacing
- Smoother copper foil...
 - Better fine line etching
 - Better signal performance
- High dielectric withstanding down to 12 microns
- No glass fabric...
 - Better signal performance
 - Better controlled impedance
 - Better laser via formation

Zeta Materials

- Film based dielectrics for thin PCB structures
- Thin copper foil/C-stage/B-stage combination
- Halogen free
- High temperature and lead free solder capable
- UL listed 94-V0
- Dk – 3.0, Df – 0.005
- Dielectric with standing 4900 v/mil
- Copper foil roughness – 2.5 microns
- Z-axis CTE – 19 ppm/°C
- Z-axis dielectric spacing down to 12 microns

Ormet Low Temperature Sintering Paste

- Connects PCB layers in the Z-axis
- Forms a metallurgical bond within the paste and the PCB copper layers
- Paste will not re-melt
- Reduces lamination steps, cycle time

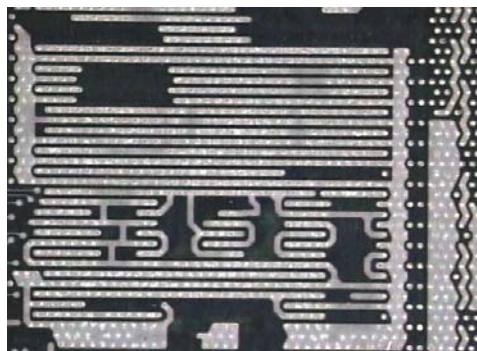
Ormet Paste Properties

- Copper/Thin alloy
- Electrical resistivity – 0.00005 ohm/cm
- Thermal conductivity – 25 W/mK
- Lap shear to copper – 1300 psi
- CTE – 22 ppm/°C
- Sintering temperature – 165 to 210°C
- Re-melt temperature - 415°C



Test Case(s) with Defined Equipment Sets

Sample Case #1



Highlights:

1/1 Trace Space

**4 N 4 Stacked Micro
Vias**

.225 mm 1300 Pin BGA

1.6 Mil Via – 4 Mil Pad

.020 Thick

Sub Panel Test

Equipment Set:

LDI, DES

Laser, Inspecta, LDI

LDI, Inspecta, LDI S/M

**LDI, Laser,
Electroless**

LDI, DES, Inspecta

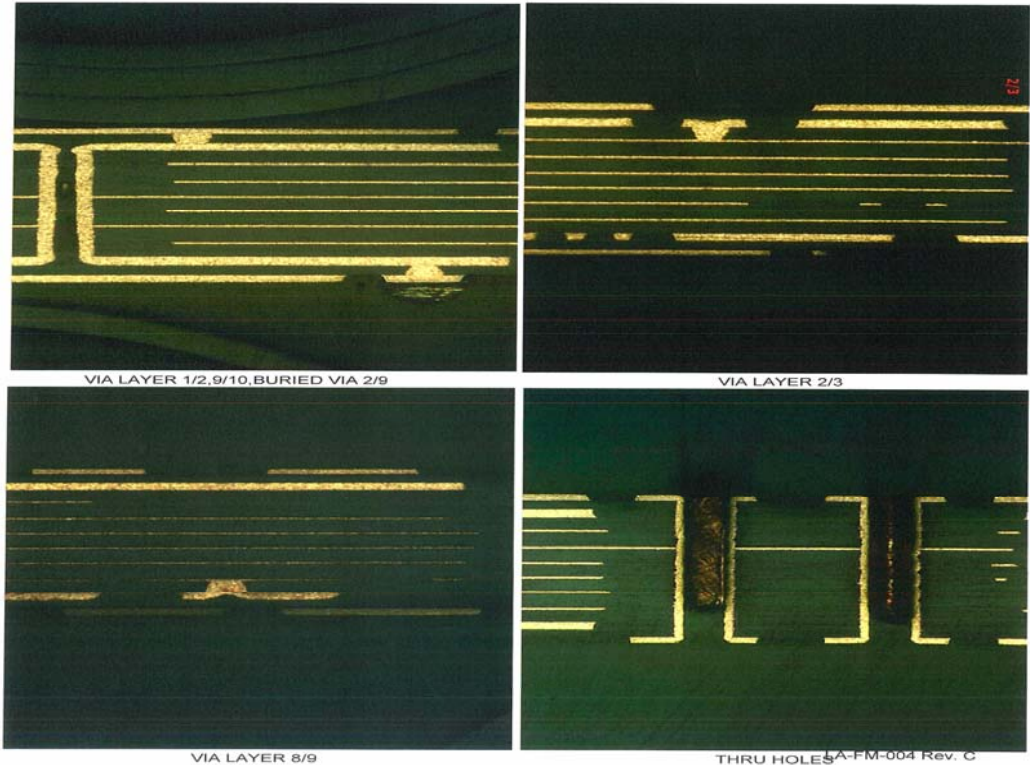
Flying Probe

Sample Case #2

Speed Test:

- 800ea 10 layers
 - 2 Lamination cycles
 - Buried vias, 2-9
 - Laser Micro Blind 2-3, 8-9
 - Laser Micro Blind 1-2, 9-10 with via in pad
 - 3/3 trace and space
 - 6.5 PTH to Copper
- Delivered in 4 Days**

Streamline Circuits: IPC 6012 Report



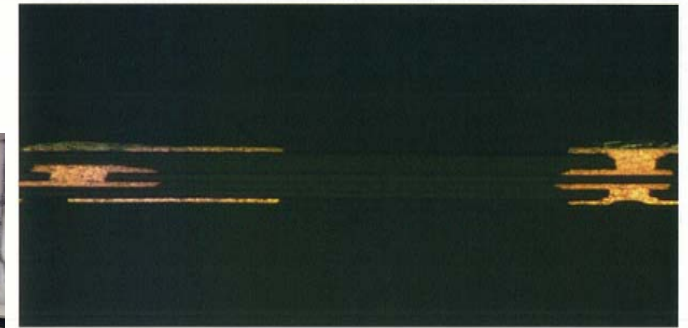
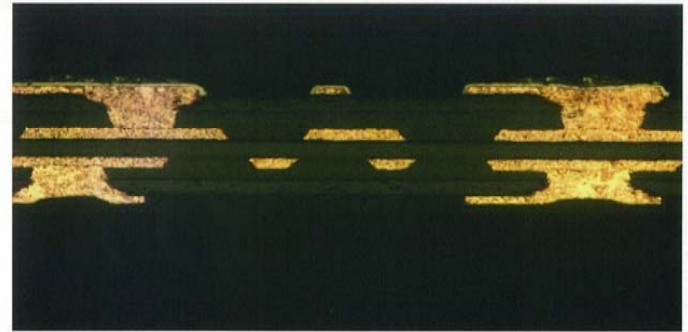
Extremely Thin:

- 4 Layer Buried vias 2 -3
- 2 Lamination cycles
- Laser Micro Blind 1-2, 3-4
- Finished thickness .0054
- Equipment set:



Sample Case #3

Streamline Circuits: IPC 6013 Report



CUST: [REDACTED]
P/N: [REDACTED]
W/O: 99056-01
T/N: 83512
REV: D
D/C: 2612-01

BACK

LA-FM-004 Rev. C



Thank You

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