IPC Designers Council Orange County Chapter

Improving Power Delivery Networks (PDNs) Using Polyimide-based Thin Laminates

2017. 7. 19.

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2. Thin laminates: material choices and applications
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Embedded passives technology

Embedded Passives Drivers

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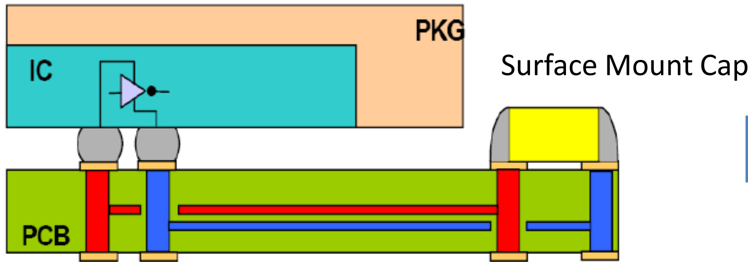
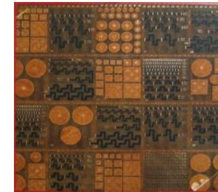
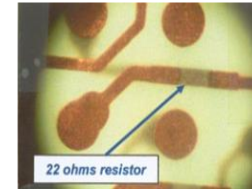
Component density
is reaching its limit.



NEMI roadmap

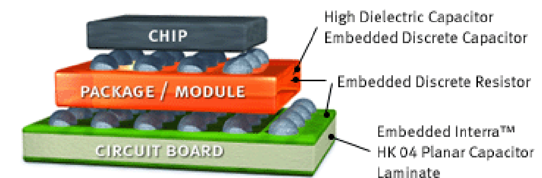




Mounting space limitation
Larger current loop
Vias and traces are inductive

Integrated capacitor has less parasitic inductance!
→ Field cancellation caused by opposing current
→ planar and in-plane, current loop is much smaller

Prof. Richard Ulrich



Embedded Component Classificiation

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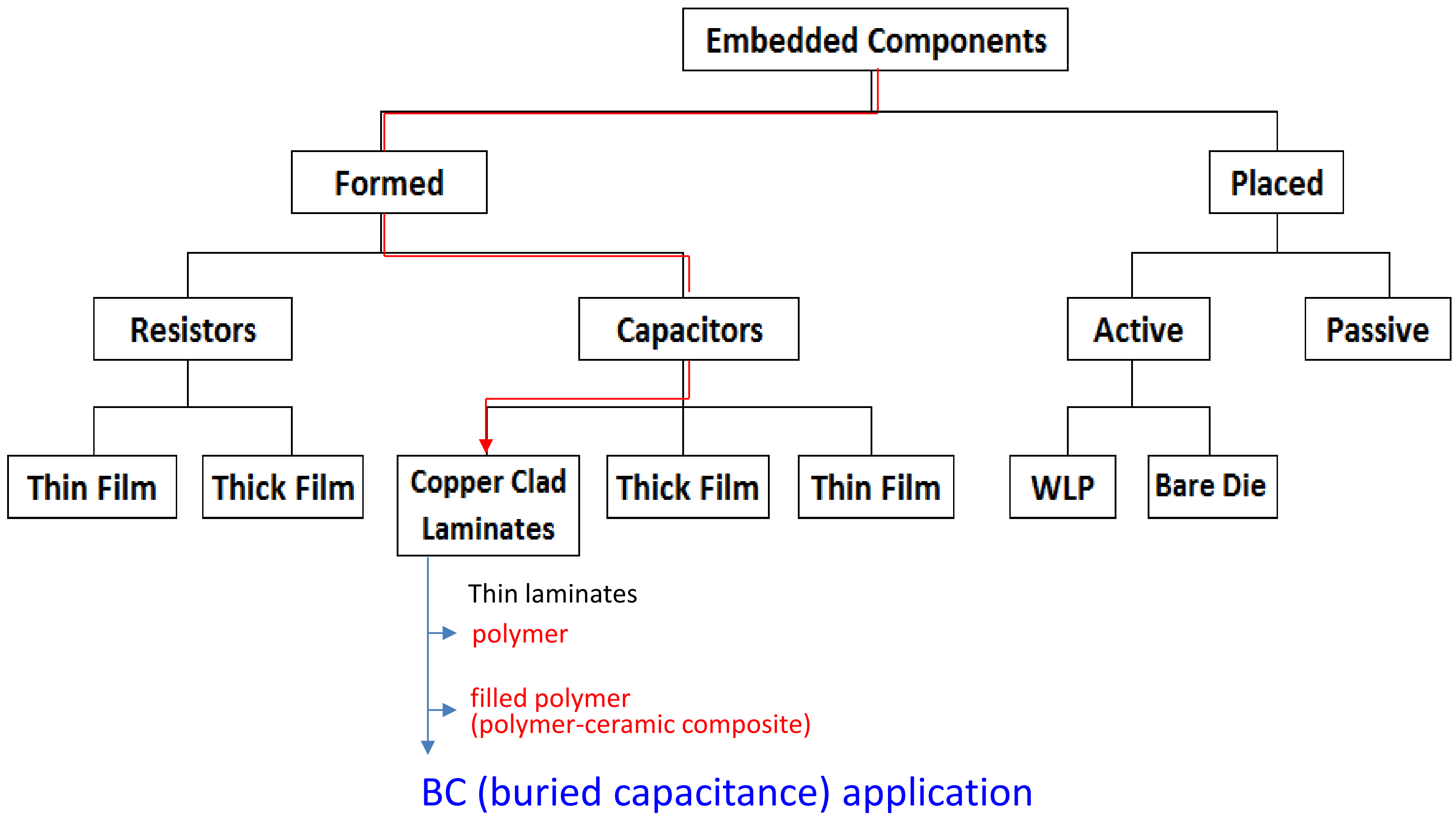
: A discrete or active component that is fabricated or inserted as an integral part of a printed board.



from 2013 IPC International Technology Roadmap

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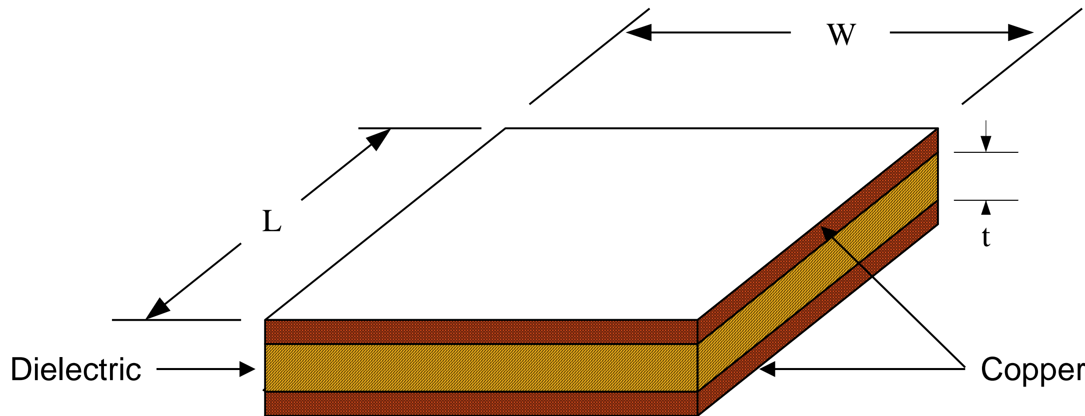
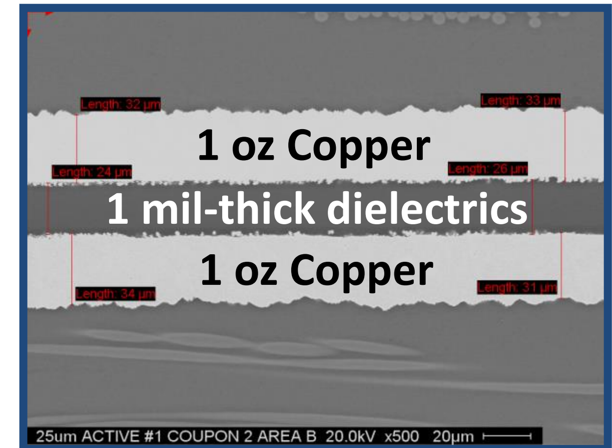
Thin laminates: material choices and applications

Thin Laminates : Construction



Cross-section



Dielectric thickness is 1mil (=25um) and below.

18 x 24 inch is standard size.

$$\text{Cap. density, nF/cm}^2 = 0.885 \frac{\text{k, the dielectric constant}}{\text{dielectric thickness, µm}}$$

$(\text{nF/cm}^2 \times 6.45 = \text{nF/in}^2)$

Prof. Richard Ulrich

Thin Laminates : Material Choices

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DuPont (Interra^{TM} HK04J)	Oak-Mitsui (FaradFlex®)	3M (ECM)
H 1 = 34.39 µm; H 2 = 31.49 µm; H 4 = 27.47 µm; H 5 = 26.13 µm; H 7 = 31.71 µm; H 8 = 32.28 µm	H 4 = 11.95 µm; H 5 = 12.28 µm; H 8 = 4.354 µm	
	6/16/2017 7:28:23 PM; HV 10.00 kV; det TLD; mode SE; mag 25 000 x; WD 4.0 mm; HFW 16.6 µm; 5 µm; Helios	0.1141 µm; 0.1240 µm; 0.1091 µm; 0.1390 µm; S3400 15.0kV 5.1mm x20.0k BSE3D 2.00um

Thin Laminates : Applications

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DuPont (Interra™ HK04J)	Oak-Mitsui (FaradFlex®)	3M (ECM)
BC Application Server & telecommunication equipment for power distribution improvement		
	Discrete Application MEMS mic, RF module, RF capacitor for miniaturization, functionality	

Thin Laminates for High Layer Count PCB

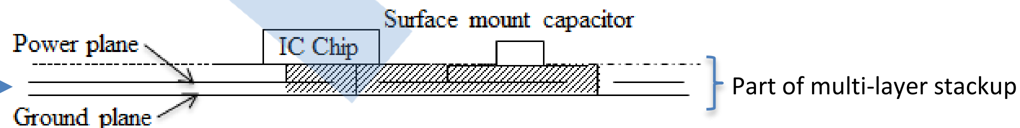
High-end computing telecom industry

- Server
- Switch
- Router
- Supercomputer

SUN's V890 server and its CPU module, which has 1 mil HK 04 on some of it's power rail. Source: **Istvan Novak**, *SUN's Experience with Thin and Ultra Thin Laminates for Power Distribution Applications, DesignCon 2006, February 6-9, 2006*

Minimize inductance in PDN
(power distribution network)

Thin laminates for power-ground layers



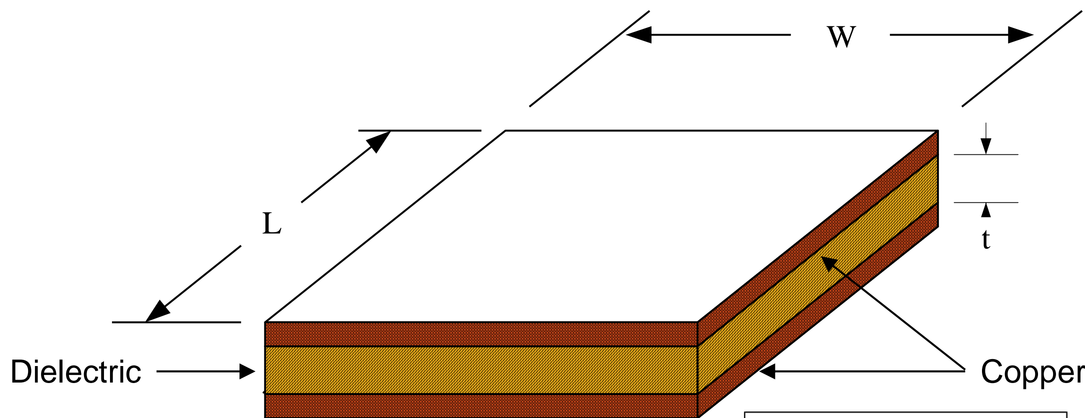
Part of multi-layer stackup

Thin laminates create very low inductance!

Design with HK04J

HK04J comes in a dielectric thicknesses of 25 and 12 microns.

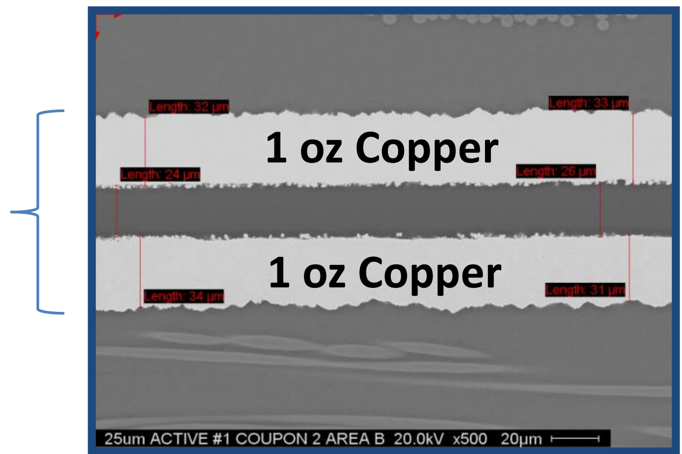
Use HK04J to improve PDN design in high layer count PCB.



$$\frac{nF}{cm^2} = 0.885 \times \frac{D_K}{t\ (\mu m)}$$

HK04J25 36 E
- E → ED copper
- 36 → 36um (1oz) copper
- 25 → 25um dielectric thickness

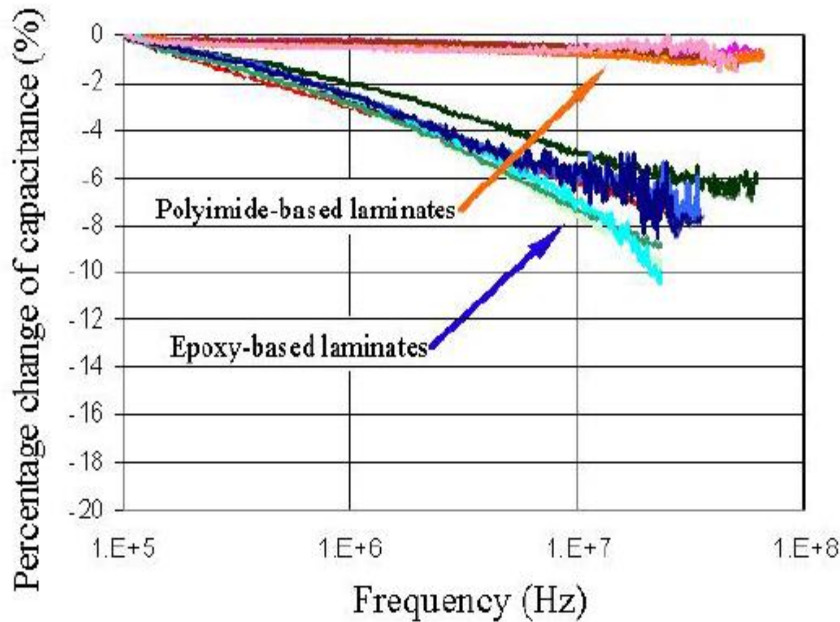
HK04J Cross-section

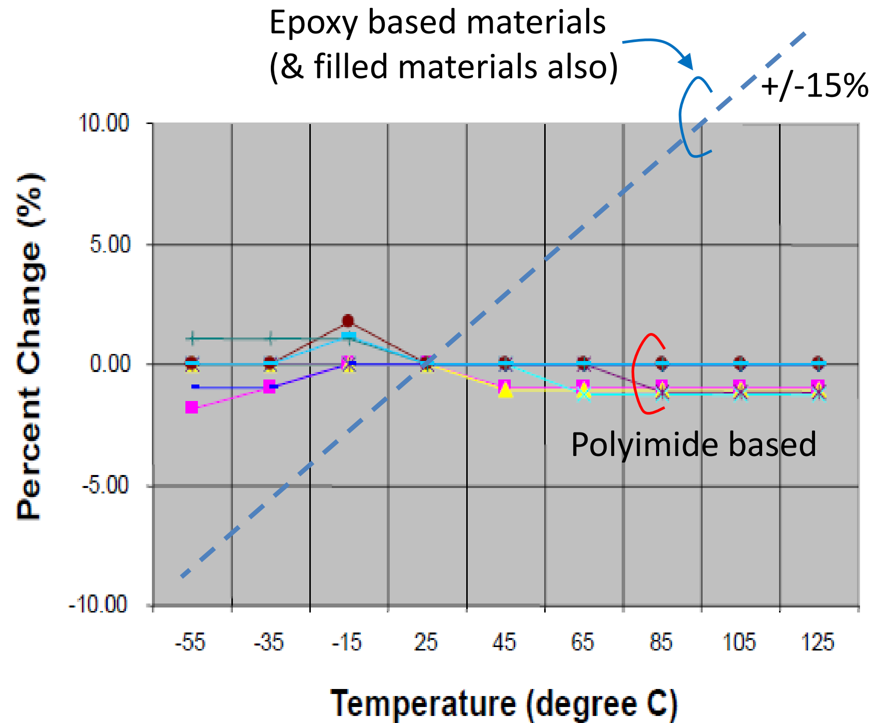


Interra® HK04J certified to IPC-4821/1

☞ Over size (i.e. 24 x 36 inch), unbalanced constructions are available.

Capacitance Stability over Temp, Freq and Bias Voltage

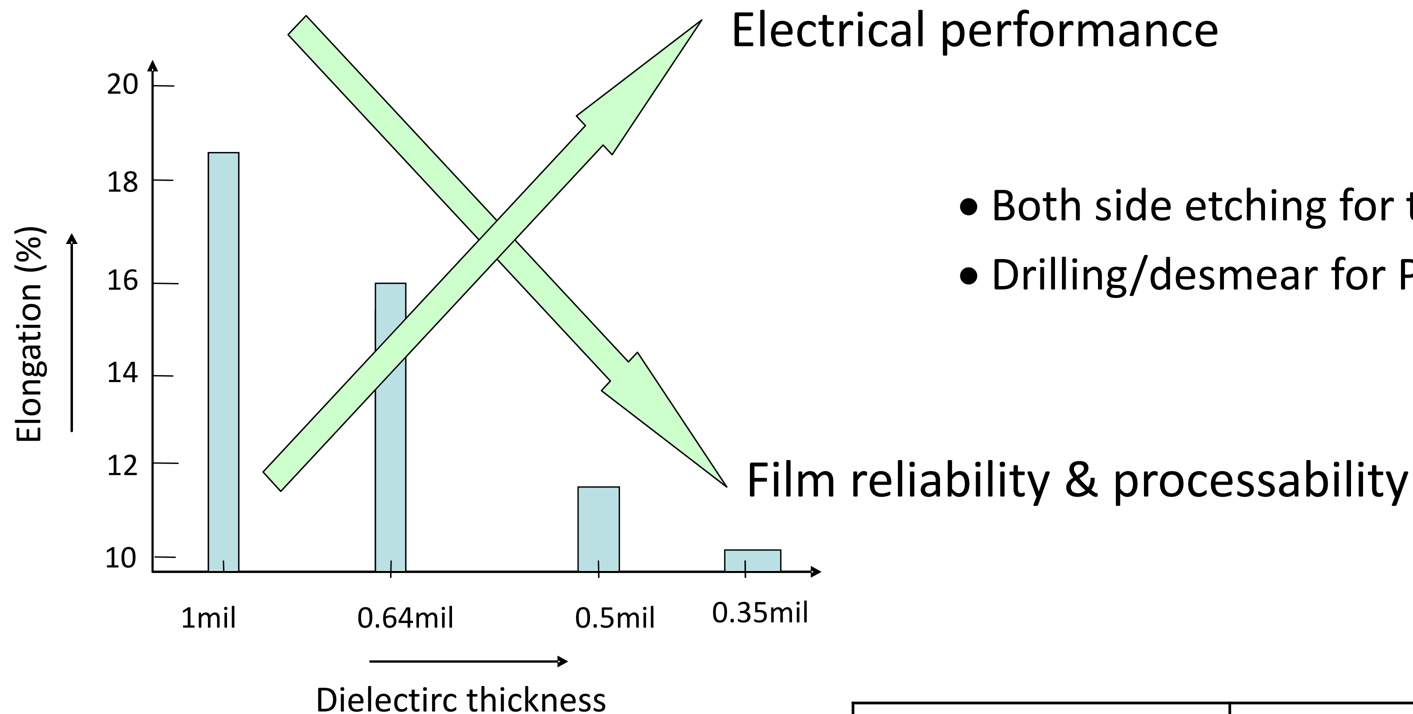




from Sun Microsystems

* TCC: Temperature coefficient of capacitance

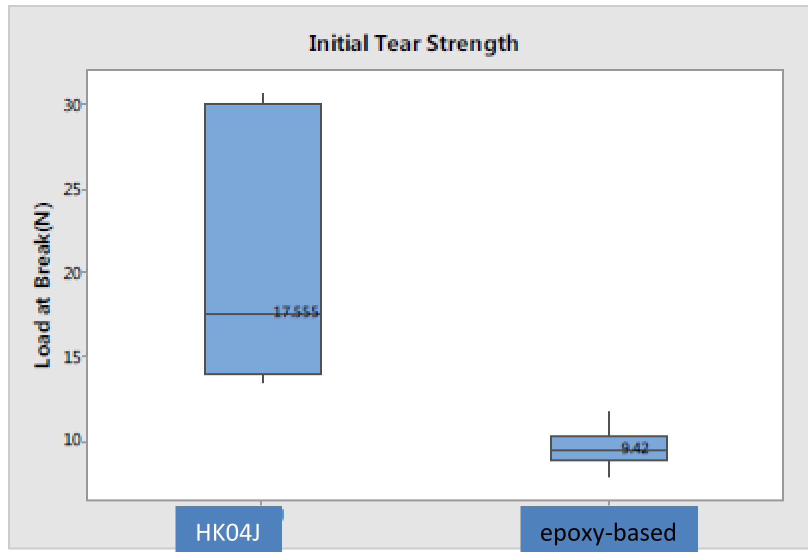
Dielectric film strength to optimize mechanical reliability and electrical performance

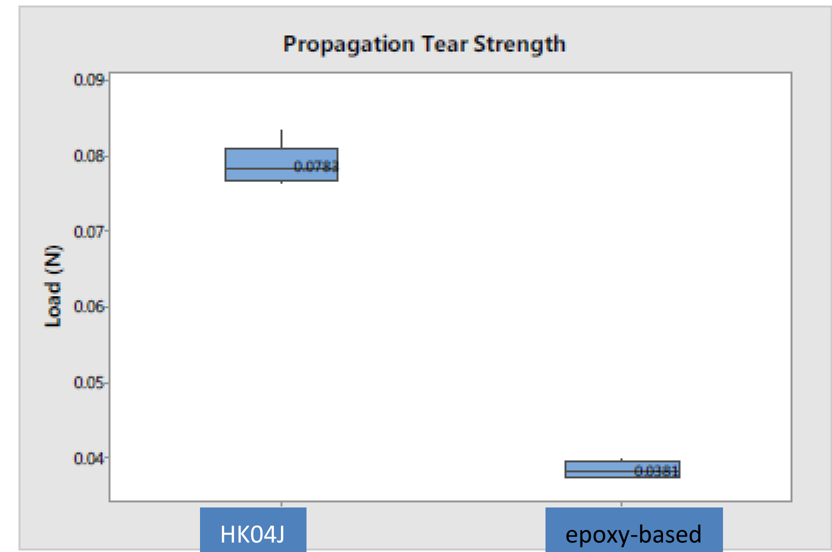


- Both side etching for thick Cu
- Drilling/desmear for PTH

Dielectrics	elongation(MD, in %)
HK04J 25um	73
HK04J 8um	45

Tear Strength Side by Side Comparison for 1mil-thick BC Core





Initial & propagation tear strength of polyimide-based dielectrics is almost double than that of epoxy-based materials which indicates robustness in manufacturing.

Interra® HK04J Product Lineup

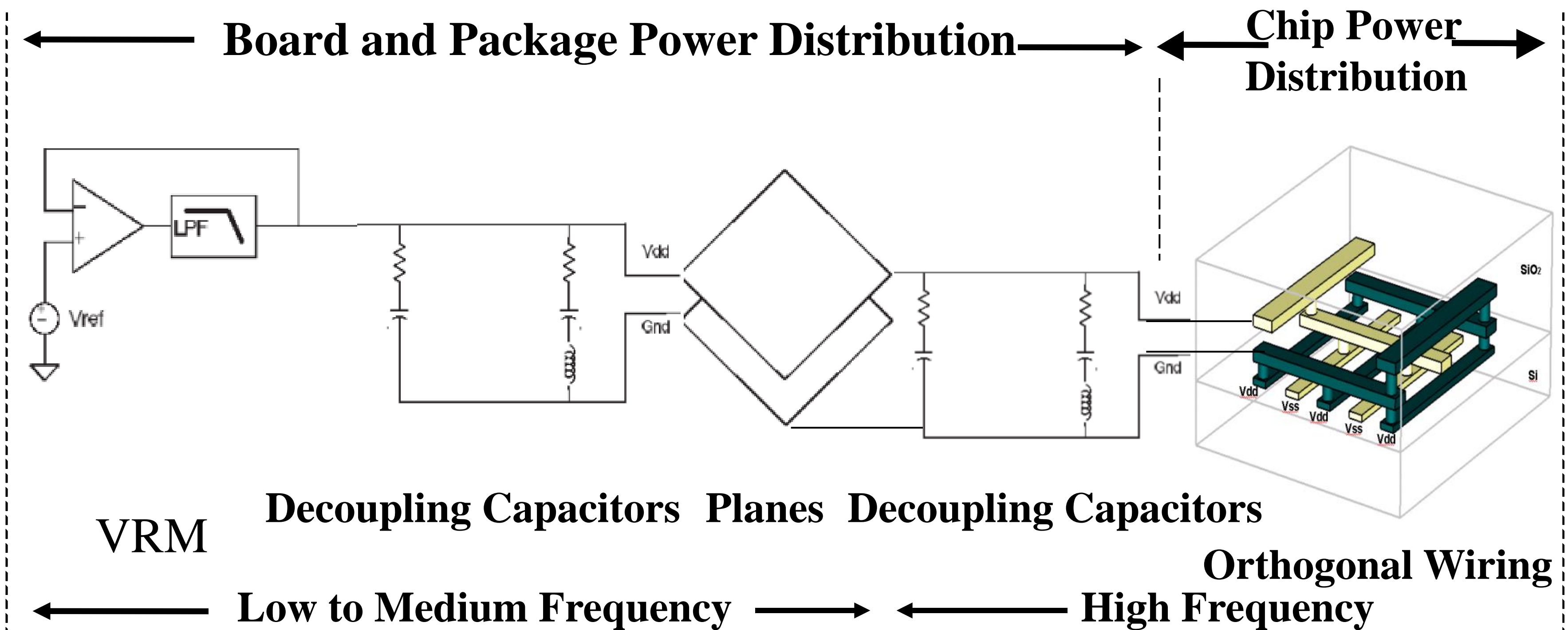
Laminate requirement	Units	Interra® HK04J			
		HK04J25 ED	HK04J12 ED	HK04J08*	
				ED	RA
Dielectric thickness (nominal)	㎛	25	12	8	8
Peel strength	kN/m	1.8	1.4	3.2	4.7
Capacitance, at 1MHz	pF/cm^2	125	260	411	384
Thermal stress, 180sec at 288℃	sec	PASS	PASS	PASS	PASS
BDV (breakdown voltage)	kV	>5	3-4	1.6	1.8

* Product under development – Initial data, based on using 2oz copper
* 8u core is not commercialized but was made off our commercial line using the same process to make standard HK04J product.

Buried capacitance for power distribution network

PDN Function

- PDN, power distribution network delivers power to ICs and other active circuits.
- Provide a return path for signals.
- PDN consists of a power supply, circuit traces, capacitors, power and ground planes, capacitors and an IC or some other active silicon
- At frequencies from as low as 100kHz the dielectric that separates power and ground planes begins strongly influencing PDN performance.
- A typical PDN looks like this :



Why HK04J Improves PDN Performance?

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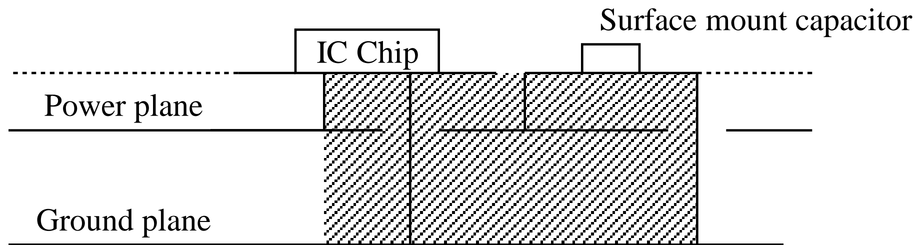
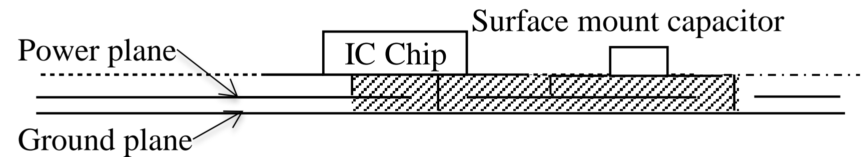


Conventional Design



Design with HK04J

- Capacitors in the past have been placed on the surface of the board in parallel to reduce the capacitor bypass inductance
- The capacitance density of the thin power and ground plane laminate is very low and does not come close to matching the total capacitance of the SMT caps
- So, why does HK04J allow you to remove capacitors from the surface of the board and save money?
- HK04J reduces the plane spreading inductance and reduces modal resonances

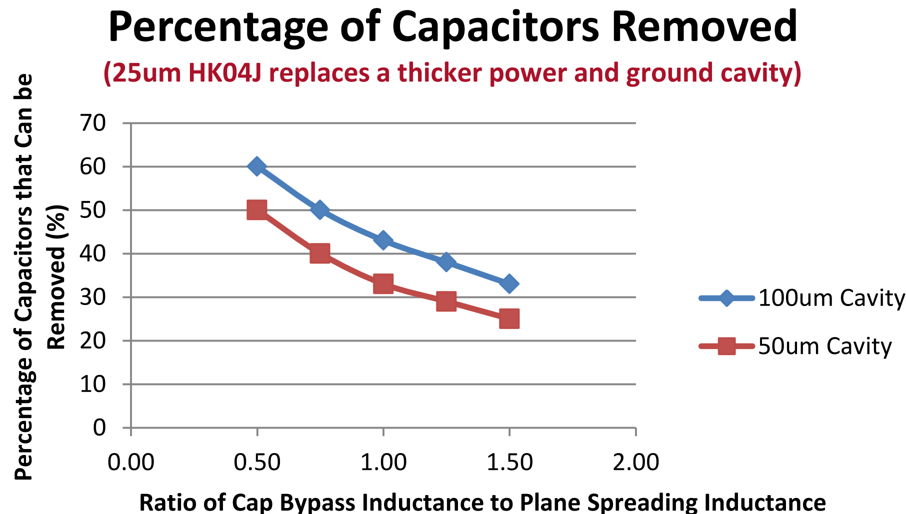
So What?

The number of capacitors needed is less – improved escape routing, increased yield by reducing assembly defect.

There is much more flexibility in where the capacitors are placed (i.e. improved circuit density).

How Many SMT Capacitors Can I Remove?

- Estimate the capacitor bypass and plane spreading inductances. Divide the bypass inductance by the plane spreading inductance to get a factor.
- The graph shows how many capacitors can be removed from your design

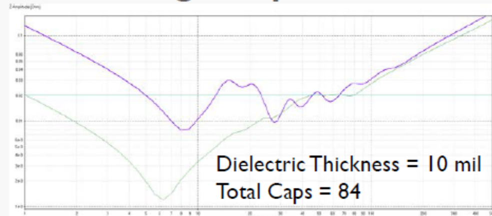


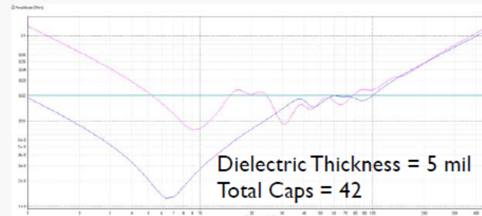
Example: If the original design uses a 100um power and ground cavity that is replaced with a 25um HK04J cavity, the percentage of capacitors that can be removed will be 43% if the ratio of the capacitor bypass network inductance to plane spreading inductance is 1.0.

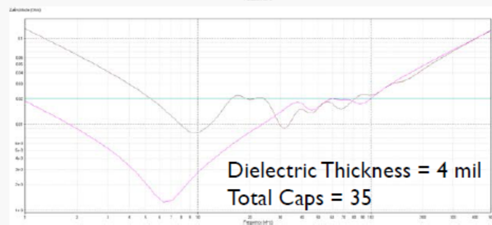
How Many SMT Capacitors Can I Remove?

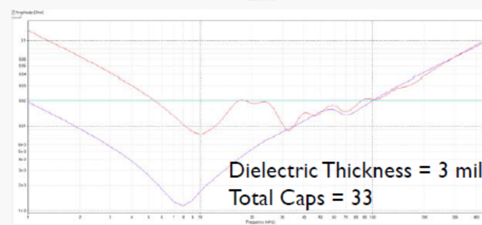
POWER DISTRIBUTION NETWORK

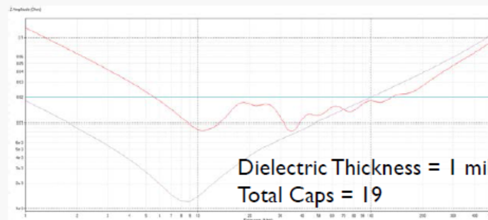
Different dielectric thicknesses and the total amount of capacitors needed to achieve target impedance of 0.02 Ohms:



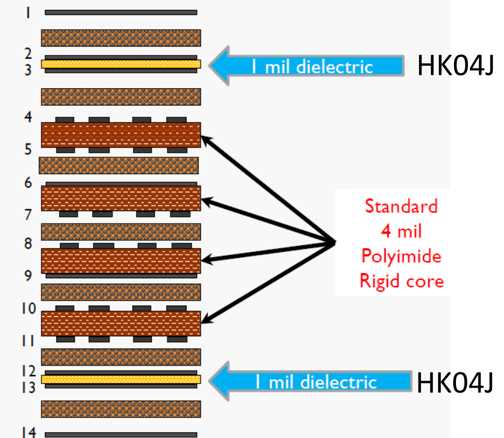








yers, ½ OZ copper on all layers



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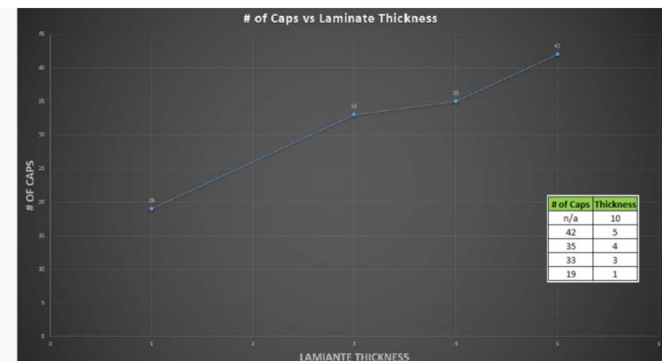


# of Caps	Thickness
n/a	10
42	5
35	4
33	3
19	1

Courtesy from Lockheed Martin
IPC Hi-Rel conference, April 2017

HK04J reduces inductance and reduces modal resonances.

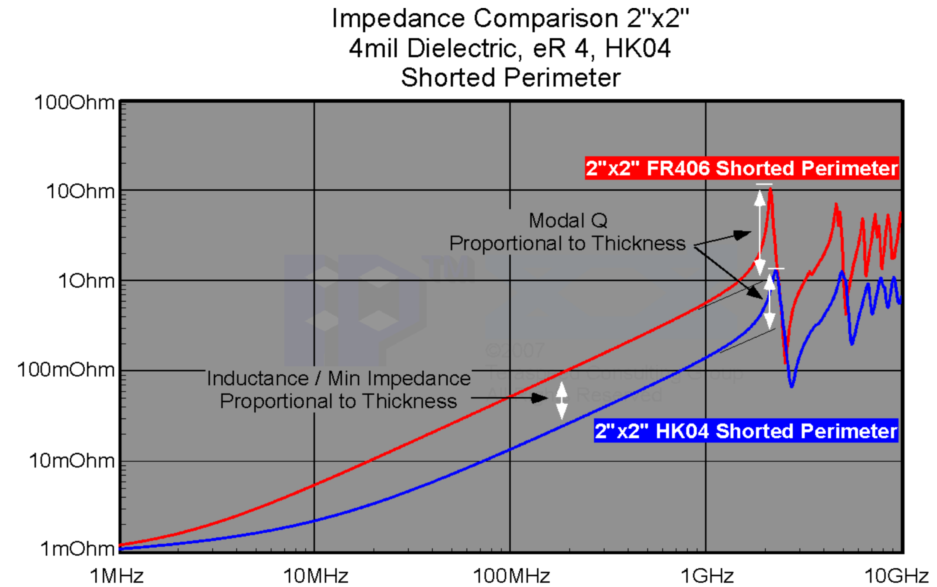
Modal resonances result from the size and shape of the power cavity, and location of IC noise source

Modal resonances are typically the worst EMI offenders

They can cause substantial SI problems as well

Characteristic Impedance:
HK04J material: typically 3.8X – 7.6X Lower Z_{CHAR} **than 100um FR-4**

Peak Impedance:
HK04J material: typically 8X – 20X lower Z_{PEAK} **than 100um FR-4**



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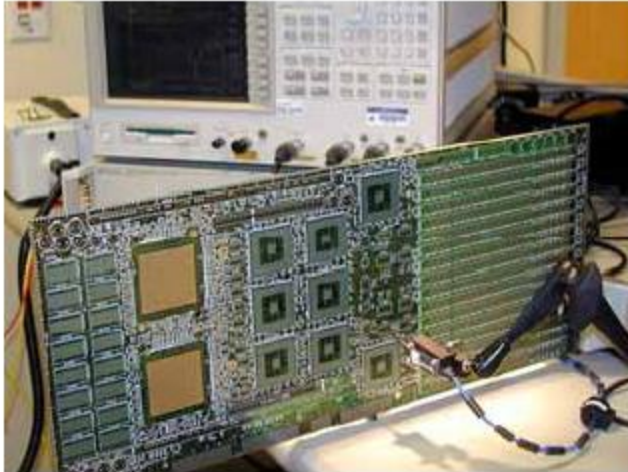
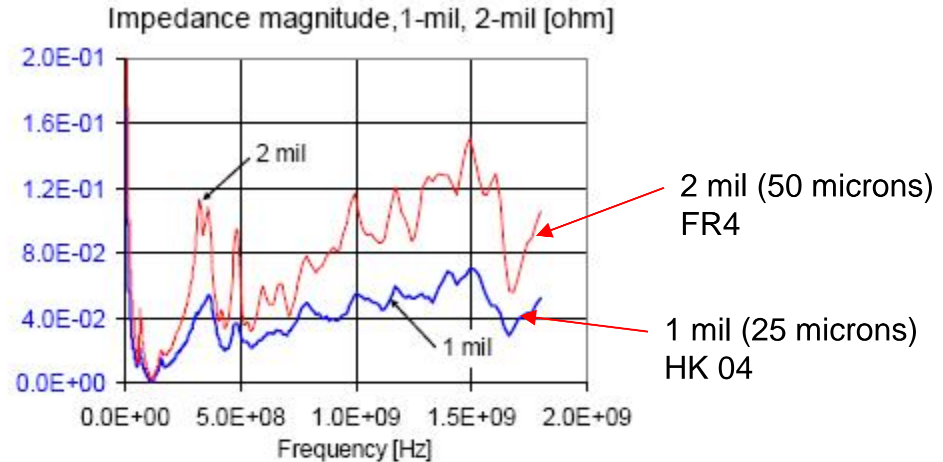
Interra® HK04J reduces impedance



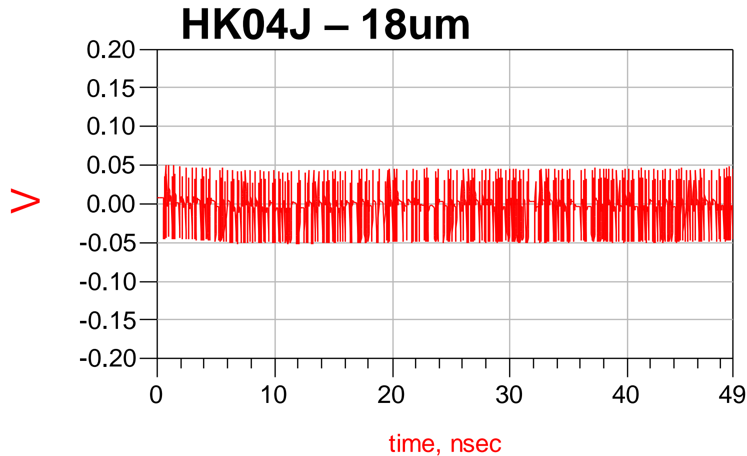
Impedance Testing set-up for SUN's V890 server CPU module

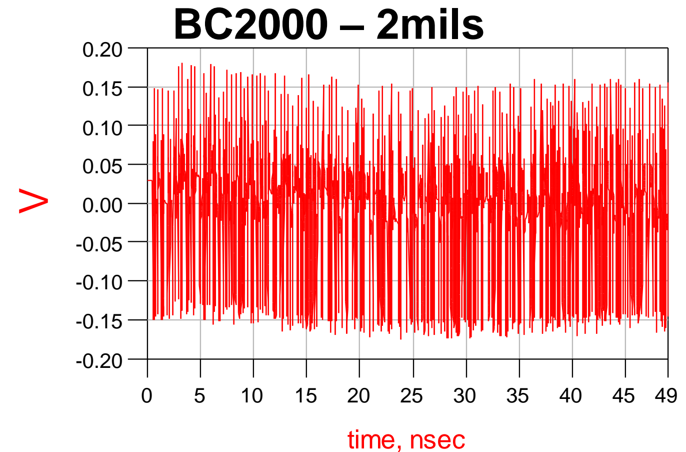


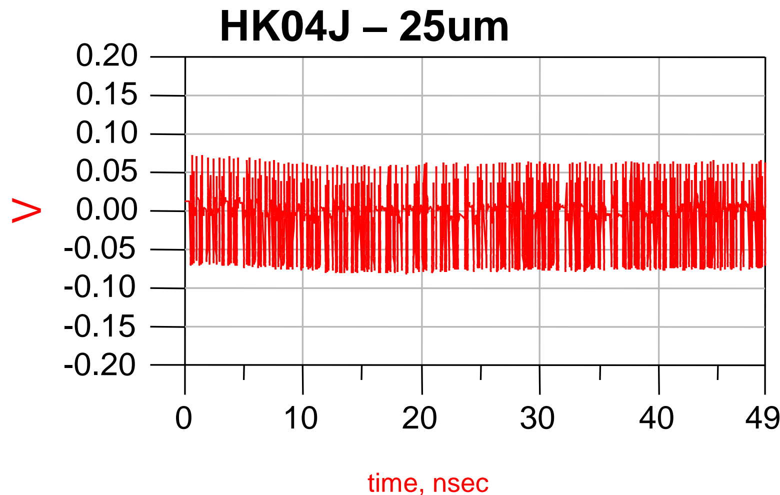
Comparison of impedance b/w 2-mil FR-4 and 1-mil HK04 at one of the test points on the bare CPU module board.

Example from a Sun V 890 server CPU module showing reduce impedance and resonance.
Source: Istvan Novak, "Embedded Capacitance and Embedded Capacitors: Overview of Modeling and Applications" at DesignCon 2006, Feb 6-9, 2006, Santa Clara, CA

SSN dramatically reduced on 6 layer board with HK04J as layers 3 and 4 as P/G and signals on layers 2 and 5







Material	SSN (peak)
HK04J – 18um	50mV
HK04J – 25um	65mV
BC2000 – 2mils	150mV

1 mil (25 µm) HK04J provides large reductions in SSN versus 2 mil BC2000

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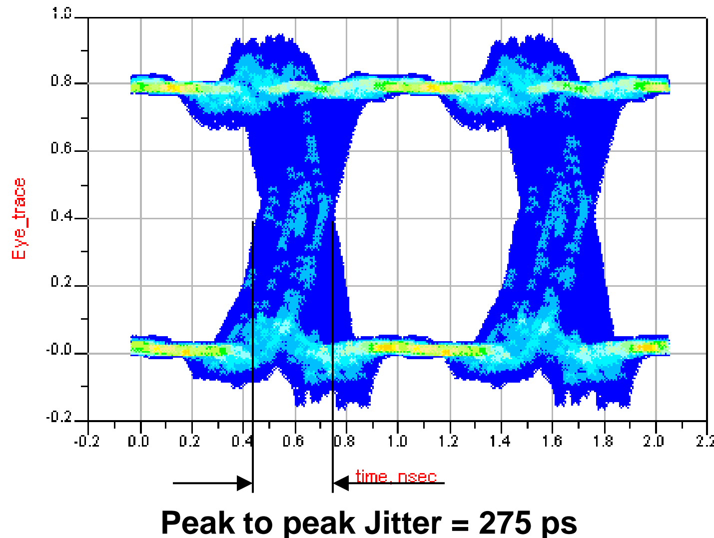
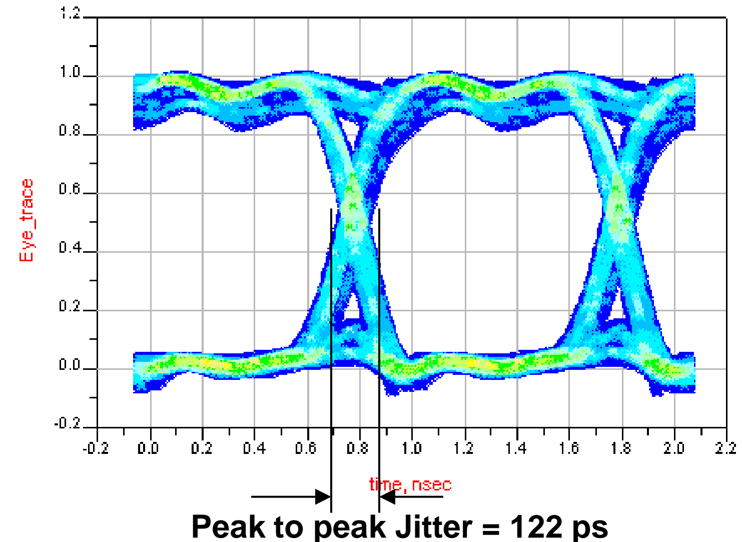
In Addition to Improved PDNs HK04J Improves Signal Integrity

FR-4, 50 microns + 100 of 100nF AVX Caps



Peak to peak Jitter = 275 ps

HK04J, 25 microns



Peak to peak Jitter = 122 ps

Simulation confirmed comparison impact on eye-opening for above two cases:

Assumptions: Similar to Server Front Side Bus

- Link Speed = 1 Gbps
- Number of lanes = 16 bit
- Line Type = Stripline, Single Ended, 50 Ohms
- Voltage swing: 1V
- Trise/Tfall = 300 ps
- Termination = 100 Ohms to both Gnd and Vdd
- Datastream = PRBS

Reducing Board Thickness

Reduce board thickness or add thicker Cu layers, for the same thickness

		WITHOUT	WITH	
1	Outer layer	0.0022	0.0022	
	Prepreg	0.003	0.003	
2	Copper	0.0012	0.0012	
	Core	0.004	0.004	
3	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
4	Copper	0.0012	0.0012	
	Core	0.004	0.001	
5	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
6	Copper	0.0012	0.0012	
	Core	0.004	0.001	
7	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
8	Copper	0.0012	0.0012	
	Core	0.004	0.001	
9	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
10	Copper	0.0012	0.0012	
	Core	0.004	0.001	
11	Copper	0.0012	0.0012	
	Prepreg	0.0045	0.0045	
12	Copper	0.0012	0.0012	
	Core	0.004	0.004	
13	Copper	0.0012	0.0012	
	Prepreg	0.003	0.003	
14	Outer layer	0.0022	0.0022	
		0.0713	**0.0593**	
		Does not fit	Fits	
			-17%	
	Copper	0.0144	0.0144	
	Dielectric	0.0525	0.0405	(- 0.012")

HK04J

(Source: Benefits and Reliability of a Thin Dielectric in a Power Supply Printed Circuit Board, Valerie A. St. Cyr, 2005 IPC Works, paper SO4-3)

Example of a 14-layer board using 4 layers of 1-mil HK04J compared to that using 4 layers of 4-mil FR-4 , reducing board thickness by 12 mils, and helping the PWB meet a 0.060 mil thickness requirement.

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Interra™ HK04 helps reduce total cost

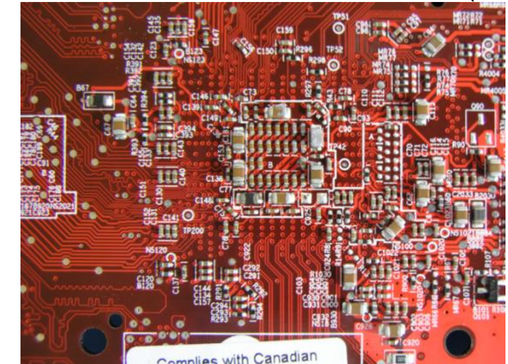
1. Reduce the number of capacitors:
   - Typically, 30-50 % of existing capacitors can be removed
   - Typical cost: 0.5 cents per capacitor + 1.2 cents assembly, rework/yield loss.
   - Example:
     - 30-layer count PCB with 3000 caps → 2000 caps = $ 17 savings.

2. Reduce the number of PTH
   - Typically, 0.08 cents per PTH; 2 PTH per cap.
   - Example:
     - 30-layer count PCB with 3000 caps → 2000 caps = 2000 PTH saved = $ 1.6 saved

3. Reduce signal-layers by reducing capacitors around a dense layer constraining BGA.
   - Example:
     - 24-layer count PCB → 22-layer count PCB = $ 140-160 savings per panel.

4. Reduce PTH aspect ratio:
   - Replace thicker Power/Ground layers, 4-mil FR-4 → 1 mil HK 04 = 3 mils savings.
   - Reduce signal layer count.
   - Impact:
     - 9-12, 0.5 % yield per unit aspect ratio improvement
     - 12-15, 1 % yield per unit aspect ratio improvement
     - 15-18, 2 % yield per unit aspect ratio improvement

Top view of a PCB with a dense BGA (GPU)



Bottom view of a PCB: Note the dense array of SMTs that can block routing.

When Does it Make Sense to Use HK04J?

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The design demands high performance:

When lower impedance is required from 300MHz to 800MHz (or higher) than is possible with thicker dielectric

The existing design is too expensive:

In high volume mfg HK04J 25um saves money if the original design has more than 3-4 caps / sq in

In medium volume mfg HK04J 25um saves money at even lower original capacitor densities

The existing capacitor bypass network is too big:

HK04J 25um typically removes > 40% of the bypass capacitors

HK04J 25um removes even more capacitors in high performance designs

Reliability and manufacturing process

HK04J Shows Proven Reliability

Test	Method/Conditions	Results
Humidity, Temperature, Bias Testing, 85/85	85ºC/85% RH for 1000 hours, 100 VDC bias	Passed with no change in resistance. Resistance under conditions E10Ω
Humidity Temperature Bias Testing, HAST	120ºC/90% RH, 2.0 atm pressure for 69 hours, 100 VDC bias	Passed with no change in resistance. Resistance under conditions E8Ω
Moisture and Insulation Resistance, M&IR	IPC TM-650 2.6.3.2	Passed. Resistance E11Ω
Temperature Coefficient of Capacitance, TCC	From –25ºC to 125ºC	Variation less than 5% over range. – 15ppm/ºC
Humidity Coefficient of Capacitance	0 to 90% RH	Increase less than 10% from 0 to 90% RH
Capacitance Change with 85/85 Aging	85ºC/85% RH for 1000 hours	Capacitance unchanged during aging
Peel Strength Change after Solder Float	Solder float 288ºC, 10 sec	No change in peel strength
Peel Strength Change with 85/85 Aging	85ºC/85% RH for 1000 hours	Peel strength > 6 pli (1N/mm) after 1000 hours
Peel Strength Change with High Temperature Aging	Bake at 150ºC for 1000 hours	No change in peel strength
Peel Strength Change with Thermal Cycling	-55ºC to 150ºC for 1000 hours	No change in peel strength

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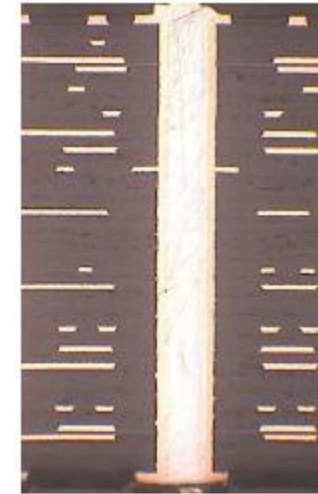
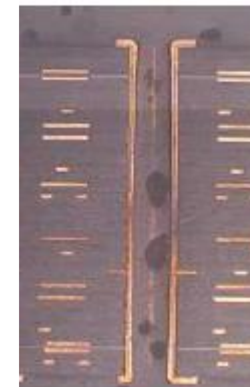
Reliability tests conducted by major PWB fabricator (using HK04J in commercial volumes)

NO.	TEST ITEM	TEST CONDITION	ACCEPTANCE	TEST RESULT	SAMPLE
1	THERMAL STRESS	PER IPC-TM-650,METHOD 2.6.8 288℃±5℃ 10~11SEC. 6CYCLES	PER IPC-6012B,3.6	NO SEPARATION NO CORNER CRACK	4 PCS
2	THERMAL SHOCK	PER IPC-TM-650,METHOD 2.6.7.2 AIR TO AIR -55℃ → 125℃ 15MIN 15MIN TOTAL 400 CYCLES	MICROSECTION MUST HAS NO CRACK,DELAMINATION,BARREL CRACK AND IP-SEPARATION	PASS	2 PCS
3	PRESSURE COOKIER TEST	TEST CONDITION : 121℃,100%RH,168H PRESSURE : 2 KGF/CM² TEST VOLTAGE : 100 VDC	MICROSECTION MUST HAS NO CRACK,DELAMINATION,BARREL CRACK AND IP-SEPARATION	PASS	2 PCS
4	INFRA-RED REFLOW	LEAD-FREE PROFILE (260℃) 6 CYCLES	PER IPC-6012B,3.10.8	NO DELAMINATION	3 PCS

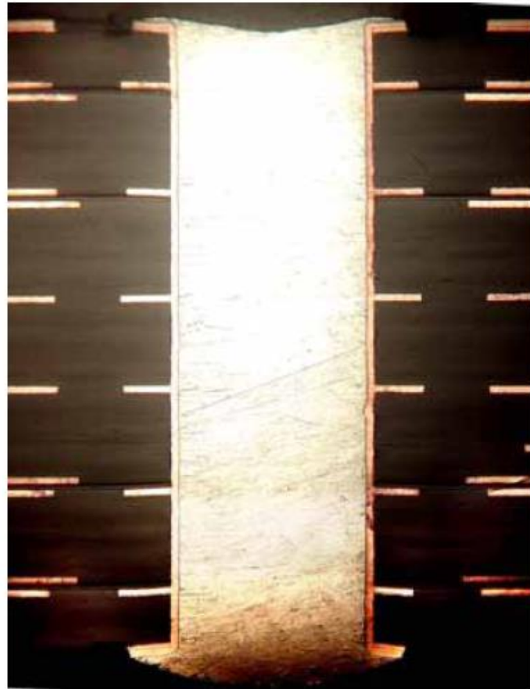


22L PWB with 2 layers of HK04J, after 6x thermal stress

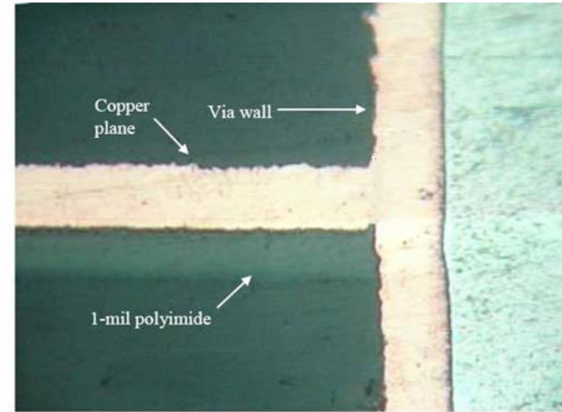


22L PWB with 2 layers of HK04J, after 400 cycles of thermal shock

Interra™ HK04J Reliability

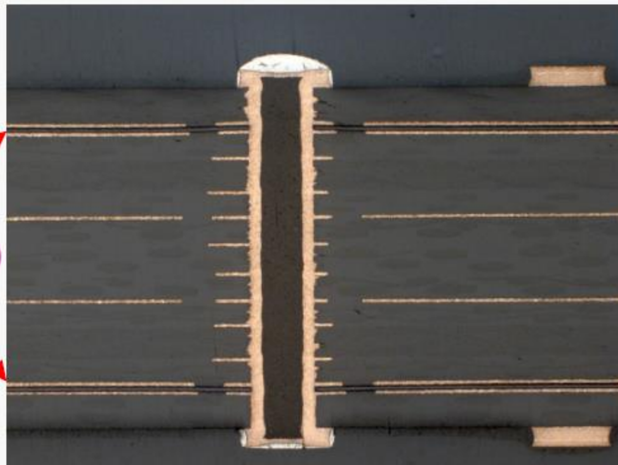


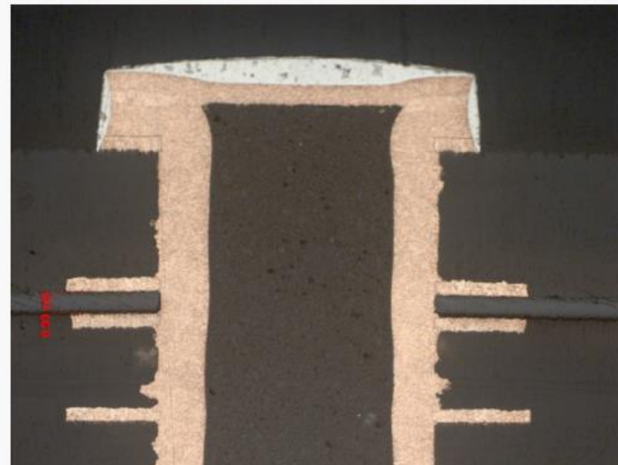
1 mil HK04J2536



Cross-section of PTH with 1 mil HK04J after 6 X solder float. No damage to the PTH. *Source:* ***Istvan Novak,*** *SUN's Experience with Thin and Ultra Thin Laminates for Power Distribution Applications, DesignCon 2006, February 6-9, 2006*

1 mil HK04J (25 microns)





Courtesy from Lockheed Martin IPC Hi-Rel conference, April 2017

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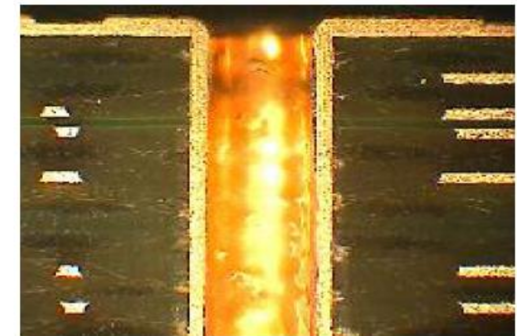
Interra™ HK04 Manufacturing: *Overview*

- **Processes on equipment capable of running 2-mil FR-4.**
  - Does NOT Require front-edge leaders at develop/etch/strip
  - Vertical Racked Black-oxide acceptable
  - No puncturing of clearance holes (anti-pads) during inner-layer processing.

  * Thin material processing equipment required

- **Double Side Processing**
  - One pass through the inner-layer process * Not requiring sequential lamination
- **PTH electroless and electroplating process = Standard**
- **HK04 scales consistently and scale-factors are comparable to that of 2-mil FR-4**
  - Dimensional Stability (mils/inch): * Does require scale characterization
    - Warp (MD): HK 04, Avg.: -0.16, σ = 0.18 vs. ZBC 2000, Avg.: - 0.93, σ = 0.11
    - Fill (TD): HK 04, Avg.: -0.36, σ = 0.14 vs. ZBC 2000, Avg.: - 0.8, σ = 0.16
- **Typical yields are significantly better than that of 2-mil FR-4**
  - HK04 Inner Layer Yield (after HiPot), Typically = 99 % vs. 2-mil FR-4 = 85-97 %
  - HK04 Final process yield, typically = 98 %, vs. 2-mil FR-4 = 85-97 %
- **Processing costs similar to that of 2-mil FR-4**



Cross-section of a PTH plated using standard electroless/electroplating process

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Processing Guidelines

Process – step	Guideline	Special concerns, if any and resolutions	Typical Yield
Preclean/ Lamination	Thin core equipment required – no leaders	• Surface Cleaning = standard • Need to be careful that the chain grippers on the roller coat line dryer don't tear through the edges for the material.	99+%
Expose	Standard Process	No Known Issues	99+%
Develop, Etch, Strip	Thin core equipment required, no leaders	No Known Issues	
Post Etch Punch	Front/ Manual Unloading Required	No issues with the cameras on etched fiducials.	99+
AOI	Standard Process	No Known Issues	
Oxide	Horizontal or vertical acceptable	Extra care when lowering layers in slots so the layers don't dent on bottom of basket.	99+
Lay-up	Standard Process	No known issues. Core less likely to fracture than woven cores.	99+

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Presentation Summary

- Power needed when an IC chip turns on is delivered by the capacitors mounted near the chip.
- Reducing the inductance associated with the power delivery network results in many good things.
- Primary advantages are a reduced # of SMT caps required for your design and improved reliability.

HK04J Benefits Summary

- Fewer plated through holes due to fewer SMT capacitors
- Improved routing capability
- Probable layer count reduction
- Lower power and ground noise
- Reduced simultaneous switching noise
- Improved signal integrity
- No glass bundles – no CAF issue
- Reduced board thickness

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Detailed Technical Discussion, Please Contact to :

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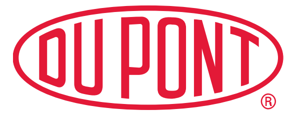
(919) 248-5024



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