PCB Cost Adders

IPC Designers Council – Orange County Chapter

TTM Technologies

Global Presence | Local Knowledge

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Objectives of this Presentation

- **Cost Adders:** Factors associated with manufacturing PCBs.
  - Design Guidelines: use green column whenever possible
  - Panel utilization
  - Variable
  - Fixed
  - Other visuals for reference
- **Class 2 vs Class 3:** Cost comparison and options
- **Material:** Cost increased with speed
- **Increased Technology:** How it affects complexity and cost
- **PCB Cost Index:** Progressively more complex stack-ups
- **Microvia Sublaminations (HDI)**

TTM NA Manufacturing Capability: Refer to the technology tables to select the best-cost design when possible

- ***'Standard'*** *Current everyday*
  capability with no premium

- ***'Advanced'*** *Current everyday*
  capability with a small premium
  - ***Extra process steps***
  - ***More expensive raw material cost***

- ***'Engineering'*** ***= Viasystems maintains experience with and can fabricate on request with a significant premium; contact Viasystems engineering to discuss your requirements***

- ***'Development'*** ***= Process development in-process based on customer demand and collaboration, will cost you an arm and a leg***

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TTM NA PCB Technology

		Standard	Advanced	Engineering	Development
Trace & Space	External Trace	0.004" - 100 µm	0.003" - 75 µm	0.0025" - 63 µm	0.002" - 50 µm
	External Space	0.004" - 100 µm	0.003" - 75 µm	0.0025" - 63 µm	0.002" - 50 µm
	Internal Trace	0.004" - 100 µm	0.003" - 75 µm	0.0025" - 63 µm	0.002" - 50 µm
	Internal Space	0.004" - 100 µm	0.003" - 75 µm	0.0025" - 63 µm	0.002" - 50 µm
Drilled Via Size	Drill Diameter	0.010" - 254 µm	0.008" - 200 µm	0.006" - 150 µm	0.004"- 100 µm
	Pad Diameter	0.020" - 508 µm	0.016"- 400 µm	0.012"- 300 µm	0.004" - 100 µm
Aspect Ratio	0.006"- 150 µm drill		6.5:1	10:1	14:1
	0.008"- 200 µm drill	8:1	10:1	12:1	16:1
	0.010"- 254 µm drill	10:1	12:1	16:1	18:1
	0.012"- 300 µm drill	10:1	14:1	18:1	20:1
	0.013.5"- 342 µm drill	10:1	16:1	20:1	24:1
Microvia	Via Diameter	150 µm & 125 µm	0.004"- 100 µm	0.006" - 150 µm	0.004" - 100 µm
	Pad Diamater	300 µm & 254 µm	0.008"- 200 µm	0.010"- 254 µm	0.007" - 175 µm
	Aspect Ratio	0.6:1	0.8:1	1:1	1:1
		2013	2013	2013	2014

TTM NA PCB Technology

		Standard	Advanced	Engineering	Development
Microvia Stack-up	# Microvia layers	1+1	2+2 3+3 4+4 5+5	6+6	>7+7
	Buried Sub	Yes	Yes	Yes	Yes
	Stacked MicroVias	No	Yes	Yes	Yes
Microvia Materials	→	Std FR4 Laser Prepregs	Low loss Epoxy Polyimide & BT	Microwave	Film Lased BUM
Attributes	Layer Count	Up to 24	26 to 44	46 to 60	>60
	Thickness	up to 3.30 mm-0.130"	up to 7.62 mm-0.300"	up to 10.16 mm-0.400"	>10.16 mm-0.400"
Laminate Materials	→	High Temp FR4 Lead Free Assembly HDI Flex & Rigid Flex	High Speed Low Loss BT & Polyimide Stablcor	PTFE RF & Microwave	LCP Film Based Non-Reinforced
		2013	2013	2013	2014

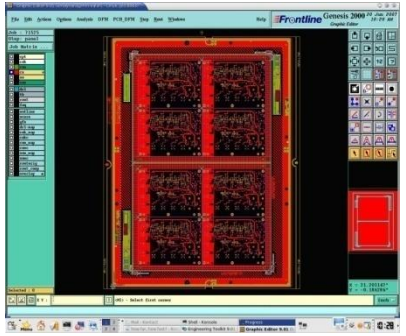
TTM NA PCB Technology

		Standard	Advanced	Engineering	Development
Embedded Passives	→	0.002" - 50 µm Capacitive Cores	Buried Resistors FaradFlex™ MC Dupont™ HK-04	High Dk Ceramic Filled	Embedded Active/Passive Devices
Surface Finishes	→	HASL OSP Immersion Tin	Lead free HASL Immersion Silver Immersion Gold	E-Less Gold Multiple ENEPIG	Neutral Eless Au Ormecon
Solder Mask	Registration	0.0025"- 64 µm	0.002"- 50 µm	0.001"- 25 µm	<0.001"- <25 µm
	Min opening	0.008"- 200 µm	0.006"-150 µm	0.006"- 150 µm	0.004"- 100 µm
Via Fill/Cap Plate CVF = Conductive Via Fill Non-CVF = Non-Conductive Via Fill	Min Drilled hole Aspect ratio	0.012" - 300 µm 8:1 Non-CVF & CVF	0.010" - 254 µm 10:1 Non-CVF & CVF	0.008" - 200 µm 6.5:1 Non-CVF	0.008" - 200 µm 10:1 Copper CVF
		2013	2013	2013	2014

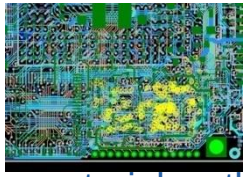
Factors that Drive PCB Cost

1) Manufacturing **Panel Utilization** (how many PCBs fit on the master panel)
2) Performance **Class** (IPC 6012B Class 2 vs 3)
3) **Layer Count** (total number of required cores)
4) Design **Complexity**, including minimums/maximums for:
    - ***Line Widths and Feature Spacing / Impedance tolerance***
    - ***Drilled Hole Size (Aspect Ratios – (PCB Thickness/Diameter)***
    - ***Overall PCB Thickness (Equipment Limitations)/ Aspect Ratios***
    - ***Annular Ring Requirements (Registration Capabilities)***
    - ***Copper Weights (Cost, Availability, and impact on Etching)***
5) Type of dielectric **Material**
6) **HDI/High Technology** (via-in-pad, buried capacitance)
7) Process **Yield** (often a **Hidden Cost**!)

Factors that Drive PCB Cost

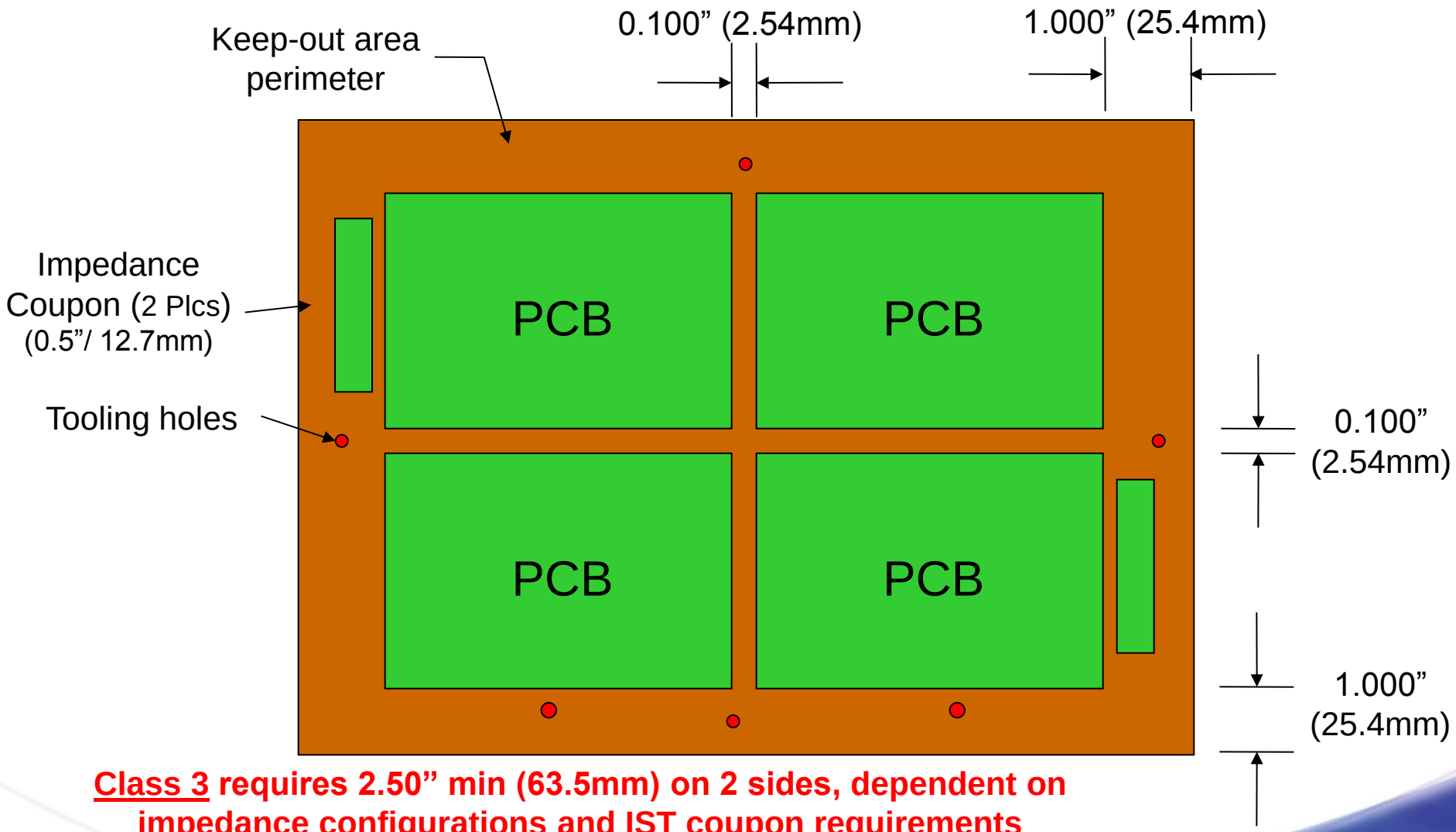


Panel Utilization is the most important factor affecting PCB cost



- PCB vendors manufacture **panels**, not individual PCBs
- Manufacturing panels come in various sizes. Some are optimized for special process or materials, others are optimized for volume production, and many panel sizes are vendor-specific
- **18" x 24"** manufacturing panels are optimized for "standard" PCB manufacturing equipment and are considered "**universal**" in that all vendors can process them
  - *"Working Area" (minus edge features - coupons, tooling, etc.) is approx 16"x22"*
  - *Other sizes include 21"x24", 14"x24", 12"x18", and 12"x12"*
- Panel utilization must be considered in the very early phases of product design, NOT AT PCB LAYOUT, since product attributes often dictate form factor
- and circuit size
- When calculating units per production panel, include rails/keep-outs required for assembly

Manufacturing Panel Utilization- Class 2

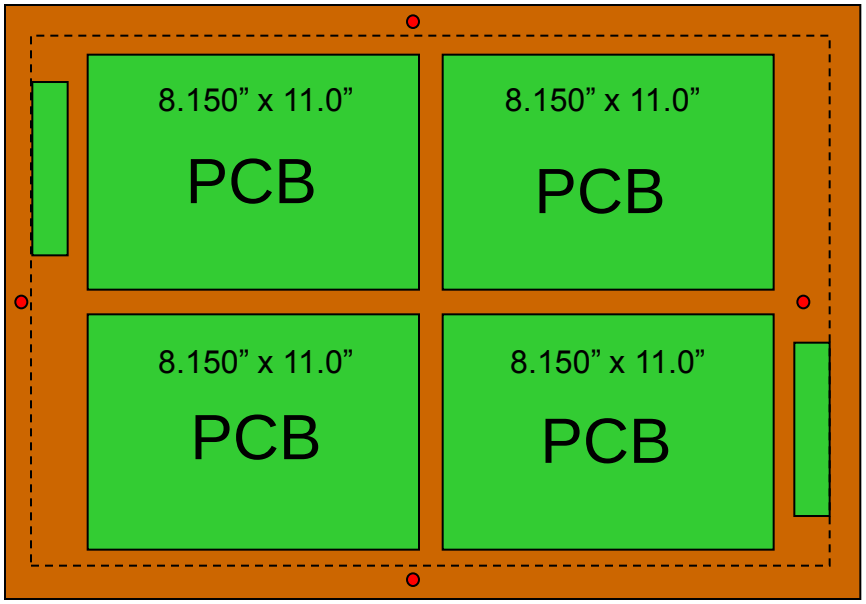


Class 3 requires 2.50” min (63.5mm) on 2 sides, dependent on impedance configurations and IST coupon requirements

Note: If board geometry permits, scoring can be used

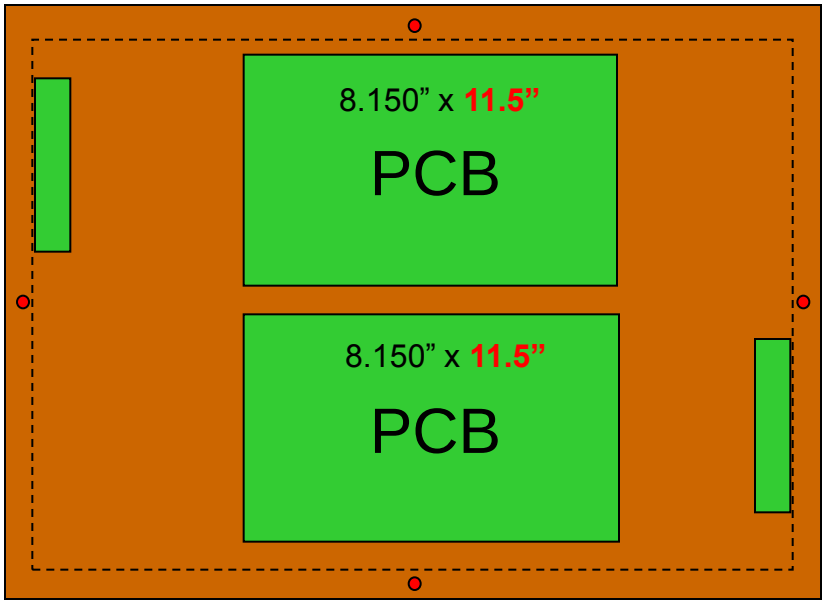
Manufacturing Panel Utilization- Class 2

Excellent Panel Utilization



Total usable area 371 in^2 total
Circuit area (including assembly rails) 358 in^2
97% panel utilization

Poor Panel Utilization



Total usable area 371 in^2 total
Circuit area (including assembly rails) 187 in^2
50% panel utilization

PCB COST = 2X

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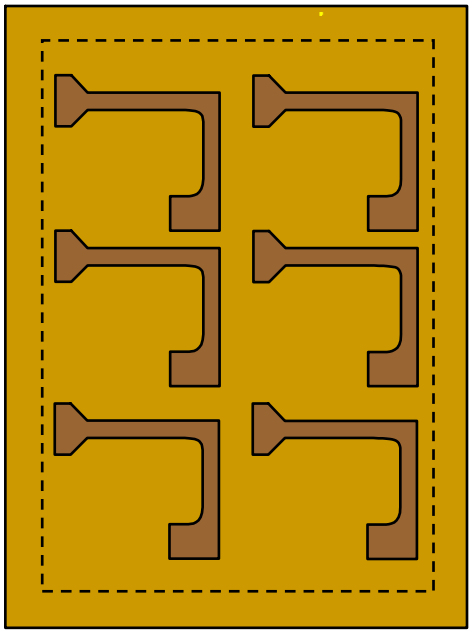
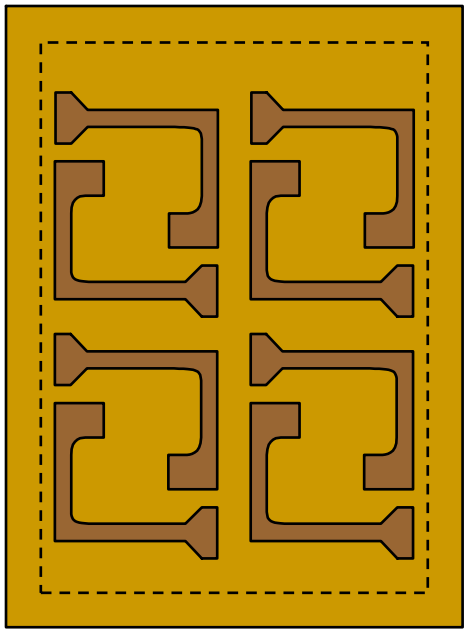
Manufacturing Panel Utilization – Nesting



No Nesting
Panel Yield: **6 parts**



Circuits Nested
Panel Yield: **8 parts**

Class 2 vs. Class 3 Cost Adders

IPC6012 Class 2 vs. Class 3 = 10-20% cost adder

- IPC **Class 2** requires cross-sections to be done on a **sampling basis** per customer requirement, if any. Most customers do not request sections.
- IPC **Class 3** requires cross-sections to be done on **100%** of the manufacturing panels. Cost impact is as follows:
  - *Greatly **increased lab time** for sectioning and report creation due to lower C=0 Sampling Index*
    - *.10 for Class 3 versus 1.5*
  - *Coupons must be **removed, documented, and retained** (up to 20 yrs for some customers)*
  - ***Additional coupons** are required for Class 3 product versus Class 2, due to sectioning and retention requirements. PCB number up and panelization can be affected.*
- IPC **Class 3** requirements result in some special process steps that consume production time and resources:
  - *All panels are **serialized** to ensure full traceability*
  - ***Plating times** are 25% longer (1 mil min vs. 0.8 mil min)*
  - *Additional **in-process micro-sectioning** is completed in order to ensure compliance with Class 3 requirements for copper and annular ring*

Class 2 vs. Class 3 Cost Adders

- Aside from the section and reporting requirements, what are the two main design differences between Class 2 and Class 3 PCBs?
  1. **Annular Ring** requirements (internal and external)
     - *Requires design modification*
  2. **Plating Thickness** requirements
     - *Mainly a process modification for the fabricator*
- The cost of going to Class 3 is primarily in the **reporting and sectioning** requirements of the spec, as well as the **lost space in panelization** due to addition coupon placement.
- If Class 3 product performance without the cost is desired, design with Class 3 annular ring and require extra plating, but specify Class 2 performance.
  - *Eliminates extra coupon requirements and subsequent lost space on the panel.*
- High-reliability fabricators usually have one main process flow, which is already set-up for Class 3 performance, for process simplification.

Class 2 vs. Class 3 Cost Adders

Attributes	IPC 6012/Cls 2	IPC 6012/Cls 3	IPC 6012/Cls 3A	MIL P 55110G	MIL-PRF-31032/5
Annular Ring External Internal	 90° breakout acceptable 90° breakout acceptable	 0.002" min, 0.001" min	 0.002" min 0.002" min	 0.002" min 0.002" min	 as specified, default .004" as specified, default .002"
Bow & Twist	0.75% max. if SMT used 1.5% max. for other	0.75% max. if SMT used 1.5% max. for other	0.5% max	As specified; otherwise, 1.5% max	As specified; otherwise, 1.5% max
Dielectric Thickness	If not specified, 0.0035" min .001" 25 µm	If not specified, 0.0035" min .001" 25 µm	if not specifiec 0.0035" 2 plys min. min .001" 25 µm	as specified if not specifiec 0.0035"	Min dielectric shall be as specified
Cu plating/Ductility	Elongation 12% min; . Tensile strength 36,000 psi min	Elongation 12% min; . Tensile strength 36,000 psi min	Elongation 18% min; . Tensile strength 40,000 psi min	No Requirement	Elongation 18% min; . Tensile strength 36,000 psi min
Copper Plating					
Through holes	avg .000787" 20 µm	avg .000984" 25 µm	avg .0015" 38µm	.001" avg	.001" avg
	min .000709" 18 µm	min .000787" 20 µm	min .0012" 30µm		
Blind vias	avg .000787" 20 µm	avg .000984" 25 µm	avg .0015" 38µm	.001" avg	.001" avg
	min .000709" 18 µm	min .000787" 20 µm	min .0012" 30µm		
Buried vias	avg .000787" 20 µm	avg .000984" 25 µm	avg .0015" 38µm	.0006" avg	.0006" avg
	min .000709" 18 µm	min .000787" 20 µm	min .0012" 30µm		
Microvias	avg .000472" 12 µm	avg .000472" 12 µm	min .0008" 20µm	.00047" avg	.00047" avg
	min .000394" 10 µm	min .000394" 10 µm			
Conductor Width Reduction	not >20% of min	not >20% of min	not >20% of min	not to exceed 20%	within +/- 20%
Etchback	when specified .0002" - .003"	when specified .0002"-.003"	.0002"- 0.0015" when required	.0002"-.002"	.0002"-.002"
Negative Etchback	shall not exceed 0.001"	shall not exceed 0.0005"	not acceptable	not acceptable	not acceptable
Cracks, barrel/corner	None allowed	None Allowed	None Allowed	None Allowed	None Allowed
Crazing	shall not span more than 50% of the distance between conductors	shall not span more than 50% of the distance between conductors	no crazing allowed	no crazing allowed	no crazing allowed
Dealmination/Blistering	shall not span more than 50% of the distance between conductors	shall not span more than 50% of the distance between conductors	no delamination allowed no blistering allowed	no delamination allowe no blistering allowed	no delamination allowed no blistering allowed
Nailheading	Acceptable	Acceptable	Acceptable	not to exceed 1.5 times cu foil thickness	

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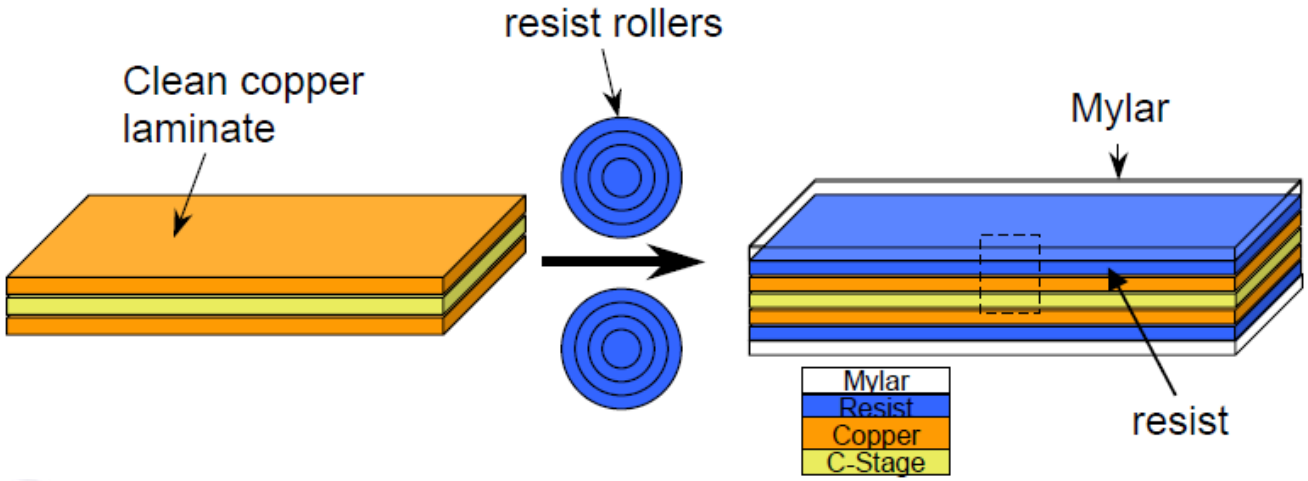
Layer Count

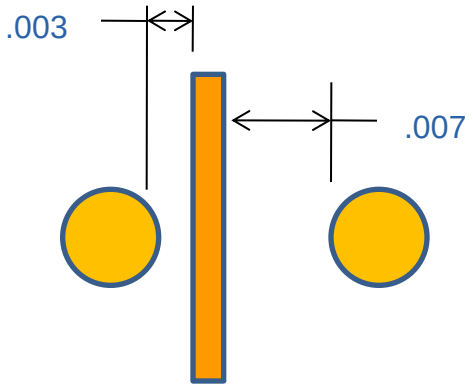
- Every two layers (core) added to a multi-layer PCB will add ~20-25% to the unit cost

- Odd layers ***do not*** save money. For example, a **7 layer** PCB costs the same as an **8 layer** PCB, due to the standard manufacturing processes involved (***same number of cores***).
  - *Standard cores are supplied to fabricators as 2-sided (Cu foil on both sides)*
  - *Internal layers are processed in pairs (individual cores)*



Fixed Costs – Line Width and Feature Spacing

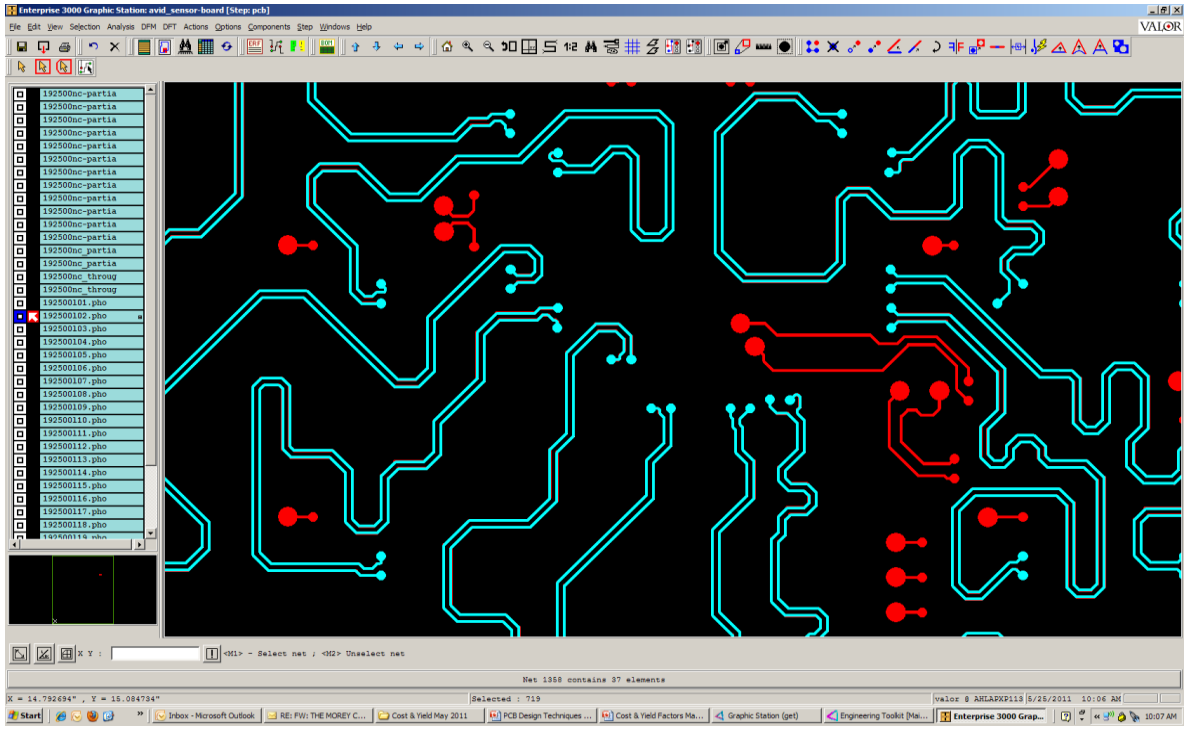
- Standard is .004”/.004” (0.102mm) L/S on ½ oz material
- .003”/.003” (0.076mm) L/S adds ~ 20-30%
- .0025”/.0025” (0.051mm) L/S adds ~ 50%
- If thinner lines and spacing are required within a confined area (BGA), using them **only where needed** will result in higher yields than using across the PCB



Rout in the center or Pads .005/.005

Impedance Trace Identification Helpful Hint

- Use **unique ‘D-codes’** (aperture line widths) for each impedance controlled trace so that the traces can be picked out and modified independently of other lines or fills. The D-codes can be as different as 0.0001 mil
  - *For example, use a 4.01 mil for an impedance controlled line width, and 4 mil for a non-controlled line width (or different ohm lines), or line-drawn plane fills*



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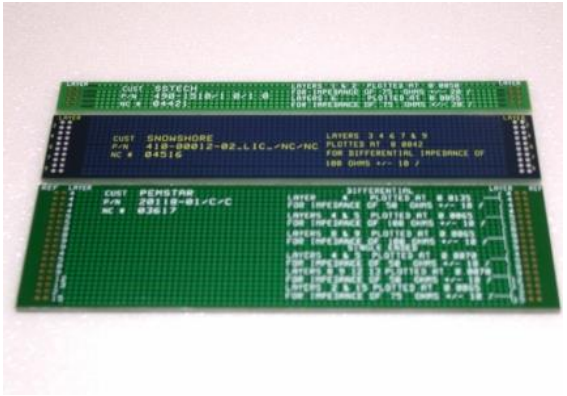
Fixed Costs – Impedance Tolerance

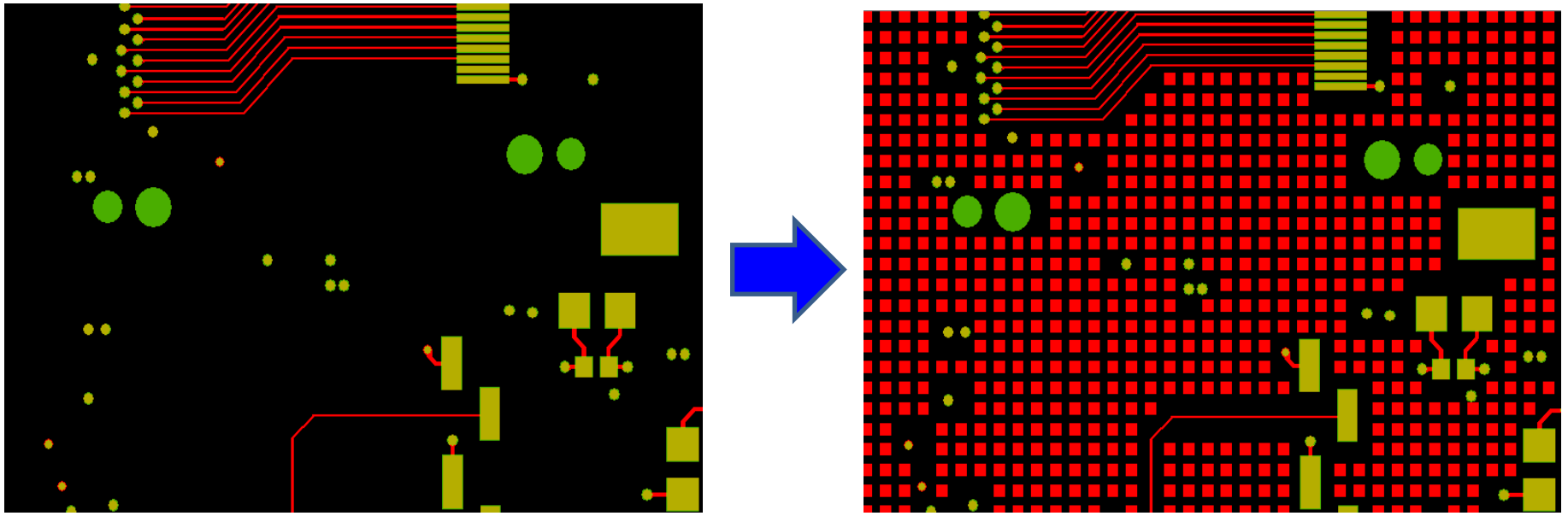
- +/-10% tolerance is standard
- +/-7% tolerance adds 20%
- +/-5% tolerance adds 30%



- Paying for the tightened impedance tolerance may be of no benefit if the proposed stackup and material set are not **robust**
  - *Standard TDR coupon per IPC-2221 requirements is used for verification*
  - *Actual PCB is more likely to have unpredictable variations than the coupon*

- Etching tolerances are independent of line widths, and improved tolerances can be obtained by using wider lines
  - *A 0.1 mil line width difference on a **3 mil** 50 Ohm line equals **1.6%***
  - *A 0.1 mil line width difference on a **5 mil** 50 Ohm line equals **0.9%***

Impedance Variation due to Poor Copper Distribution



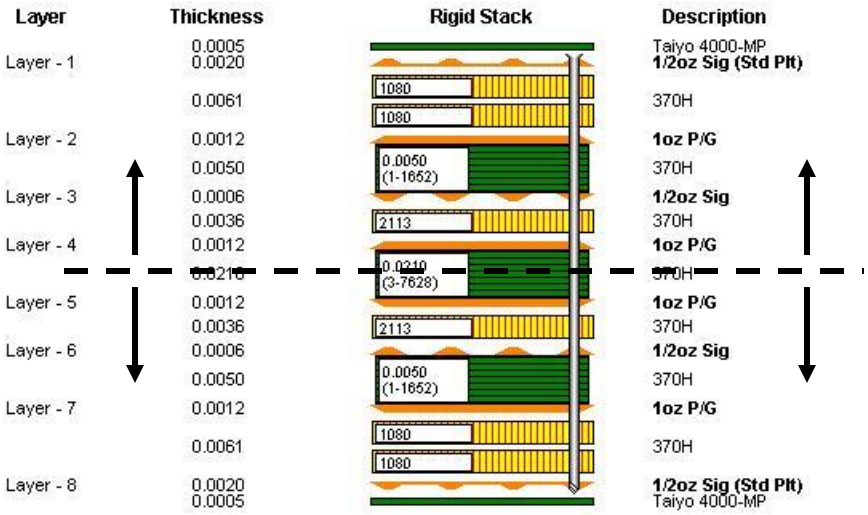
Thieving squares/dots or solid copper area fill eliminates poor feature distribution

*Maintain 0.200” min keep-out zone from any copper feature

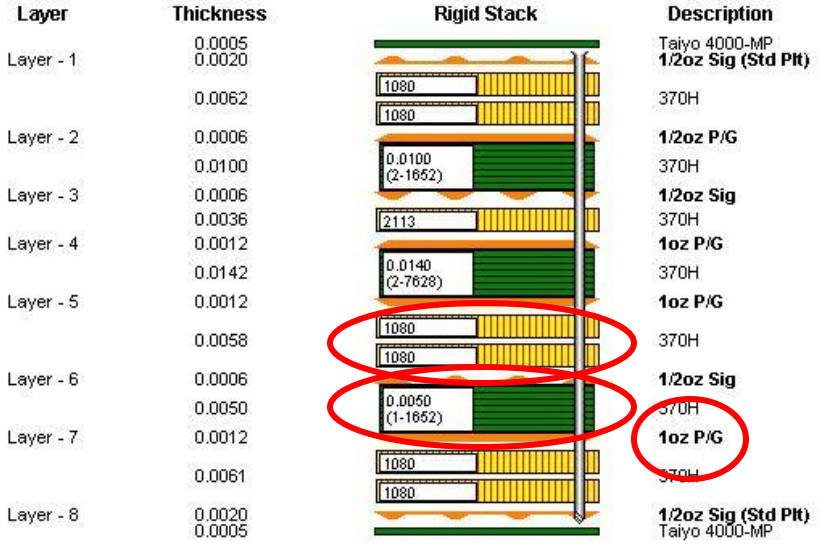
Stackups – Symmetry

- With BGA devices prevalent in today's designs, **flatness** is critical
- Symmetry is the most important step that can be taken to ensure that no **warpage** or **residual stresses** are present in the final product
- The build should be symmetrical about the Z-axis, including copper, prepregs, and cores
- When possible, use single-ply cores, except for heavy copper designs
- The best builds will utilize the **same core thickness and prepreg style** throughout.

PREFERRED



NOT PREFERRED



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Variable Costs – Mechanical Drilling

- The **largest variable cost** in PCB manufacturing
- Drilling holes consumes drill bits at the rate of one bit for every 1000 holes drilled. (0.006” drills ~500-700 hits)
- Some fabricators (TTM included) will often include a certain amount of drill hits *per manufacturing panel* in the **base cost** (for TTM, up to 25K hits on a manufacturing panel are included)
- Additional costs will amount to 1-2% for every extra 10K holes
- Drill hole **size is not an adder until** size is **less than 8 mils** (0.2mm) in NA
  - *15-20% cost adder for 6 mil (0.15mm) holes*
  - *Aspect Ratio (depth/diameter) must be considered*

Variable Costs – Mechanical Drilling

- Estimators look for the smallest drill size on the drill table within the fabrication drawing, which is always the **smallest via size** in the design

- General rule of thumb is that drill sizes in a drill table are “finished” hole sizes, but this is not entirely correct with respect to vias

- Hole sizes less than 18 mils (0.46mm) are **almost always interconnecting vias**, and are usually interpreted in the drill table as ***drill bit*** size, not finished hole size

- For maximum fabricator flexibility, tolerances on vias should be stated as “+.000”/- (*hole size*)” or “**no min**”

SIZE	QTY	SYM	PLATED	TOL
0.008	2724	F	YES	+0.002/−0.008
0.012	1317		YES	+0.003/−0.012
0.025	172		YES	+/−0.002
0.032	4	M	YES	+/−0.003
0.035	14	A	YES	+/−0.003
0.037	2	E	NO	+/−0.003
0.041	28	P	YES	+/−0.003
0.052	8	I	YES	+/−0.003
0.06	2	H	YES	+/−0.003
0.062	2		YES	+/−0.003
0.07087	5	N	YES	+/−0.003

Variable Costs – Mechanical Drilling

- How about the **Number of Drill Sizes** on a particular design?
- This is a challenge for many fabricators, as having too many drill sizes results in more drill bits required in each “kit” for manufacturing, particularly if each drill size is used for a small number of holes, and can lead to a cost adder, if excessive
- Finished hole sizes are drilled oversized by 4-6 mil (0.1-0.15mm) by fabricators in order to account for subsequent plating requirements (copper + final finish)
- Hole diameters that are close will generally be drilled with the same size drill bit, as long as finished diameter is within specified tolerance

Variable Costs – Mechanical Drilling

- Example of excessive number of drill sizes
- 44 “unique” drill bit sizes
  - Combine sizes into one that will fit
- 93% of holes are defined by the first four bit sizes
- 70% of tool sizes are used for <10 holes on the manufacturing panel (1-up part/panel)

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILLIMETERS

FIGURE	SIZE	TOLERANCE	PLATING	TYPE	QTY
△	0.20	+/-0.025	PLATED	uVia	414
A	0.25	+0.000 -0.150	PLATED	Drill	5990
D	0.33	+/-0.075	PLATED	Drill	934
F	0.43	+/-0.075	PLATED	Drill	865
N	0.44	+/-0.075	PLATED	Drill	34
R	0.44	+/-0.075	PLATED	Drill	119
S	0.55	+/-0.075	PLATED	Drill	15
V	0.70	+/-0.075	PLATED	Drill	39
V	0.70	+/-0.075	PLATED	Drill	6
Y	0.80	+/-0.075	PLATED	Drill	84
H	0.90	+/-0.075	PLATED	Drill	134
L	0.95	+/-0.075	PLATED	Drill	6
W	1.00	+/-0.075	PLATED	Drill	33
C	1.15	+/-0.075	PLATED	Drill	4
T	1.25	+/-0.075	PLATED	Drill	6
K	1.50	+/-0.075	PLATED	Drill	4
P	1.65	+/-0.075	PLATED	Drill	2
U	1.95	+/-0.075	PLATED	Drill	4
X	2.30	+/-0.075	PLATED	Drill	12
B	2.50	+/-0.075	PLATED	Drill	3
Ⓜ	2.54	+/-0.075	PLATED	Drill	4
K	3.30	+/-0.075	PLATED	Drill	2
◇	0.74	+/-0.05	NON-PLATED	Drill	2
Ⓖ	0.80	+/-0.05	NON-PLATED	Drill	9
Ⓔ	1.10	+/-0.075	NON-PLATED	Drill	3
R	1.10	+/-0.075	NON-PLATED	Drill	3
Ⓨ	1.20	+/-0.05	NON-PLATED	Drill	4
Ⓗ	1.25	+/-0.05	NON-PLATED	Drill	2
◇	1.30	+/-0.05	NON-PLATED	Drill	4
Ⓘ	1.40	+/-0.05	NON-PLATED	Drill	1
Ⓒ	1.50	+/-0.05	NON-PLATED	Drill	3
Ⓒ	1.50	+/-0.05	NON-PLATED	Drill	3
Ⓚ	1.60	+0.04 -0.00	NON-PLATED	Drill	13
△	1.60	+0.04 -0.00	NON-PLATED	Drill	4
Ⓜ	1.65	+/-0.05	NON-PLATED	Drill	7
Ⓜ	1.70	+/-0.05	NON-PLATED	Drill	2
Ⓝ	1.80	+/-0.05	NON-PLATED	Drill	8
Ⓟ	1.95	+/-0.05	NON-PLATED	Drill	1
Ⓛ	2.00	+/-0.05	NON-PLATED	Drill	4
Ⓞ	2.05	+/-0.05	NON-PLATED	Drill	1
W	2.15	+/-0.05	NON-PLATED	Drill	2
Ⓣ	2.20	+/-0.05	NON-PLATED	Drill	2
Ⓤ	2.25	+/-0.05	NON-PLATED	Drill	2
Ⓦ	2.35	+/-0.05	NON-PLATED	Drill	4
Ⓔ	3.00	+/-0.05	NON-PLATED	Drill	2
Ⓔ	3.00	+/-0.05	NON-PLATED	Drill	2
Ⓖ	3.175	+/-0.075	NON-PLATED	Drill	11
◇	3.20	+/-0.05	NON-PLATED	Drill	14
Ⓜ	3.50	+/-0.05	NON-PLATED	Drill	8
Ⓞ	3.90	+/-0.05	NON-PLATED	Drill	11
				TOTAL HOLES:	8846

Fixed Cost Adders – Board Thickness and Via Aspect Ratio

Board Thickness Adders

- Any thickness up to 93 mils is considered standard
  - Thin cores cost more
- 94-120 mils adds ~10-20%
- 121-250 mils adds ~25-35%
- Design review is required for anything over 250 mils (6.35mm) (equipment limitations) or under 20 mils (0.5mm) (handling issues)

Aspect Ratio (thickness : min drill size) Adders

- Aspect ratios of 10:1 or less are considered standard
- >10:1-11.99:1 adds ~10-15%
- 12:1-12.99:1 adds ~20-25%
- 13:1-14.99:1 adds ~30-35%

Board Thickness and Via Aspect Ratio

Aspect ratio is the ratio of overall thickness to drill size), but is not a universal indicator of capability. Related to how easily the holes walls can be plated with copper.

- Examples (**All 10:1** Aspect Ratios):
  - *120 mil (3mm) thick PCB with 12 mil (0.3mm) drill* - **STANDARD**
  - *80 mil (2mm) thick PCB with 8 mil (0.2mm) drill* - **ADVANCED**
  - *60 (1.5mm) thick PCB with 6 mil (0.15mm) drill* - **ENGINEERING**

		Standard	Advanced	Engineering	Development
Aspect Ratio	0.006" drill		6.5:1	10:1	14:1
	0.008" drill	8:1	10:1	12:1	16:1
	0.010" drill	10:1	12:1	16:1	18:1
	0.012" drill	10:1	14:1	18:1	20:1
	0.0135" drill	10:1	16:1	20:1	24:1

- Always understand the context of a fabricator's maximum aspect ratio capability listing

Fixed Cost Adders – Surface Finish

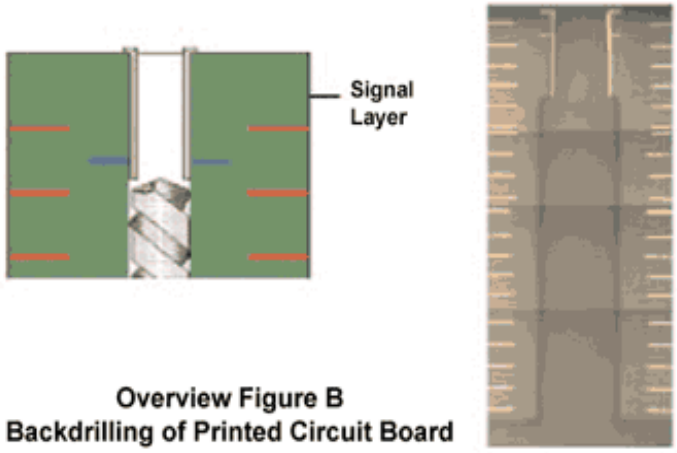
Surface Finish Adders

- **OSP**, Immersion **Silver**, **ENIG**, and **SnPb HASL** are **NOT** cost adders
- **ENEPIG** adds 10% per manufacturing panel
- **Lead-Free HASL** adds 5% per manufacturing panel (subcontract is higher)
- **Hard Gold** is priced per in^2 area at the current market price of gold
- Selective Finishes (**combinations**) are priced on an individual basis

Fixed Cost Adders – Fabrication

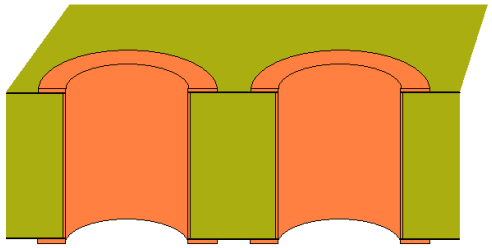
Miscellaneous Adders

Removing the Unused Portion of PTH

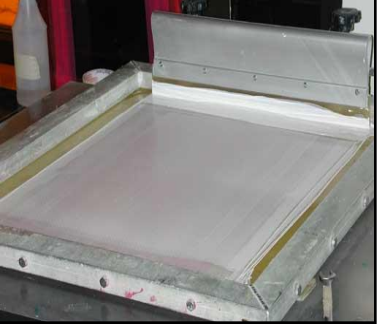


Overview Figure B
Backdrilling of Printed Circuit Board

- Scoring – No Cost Adder
- Milling – 5-10% (at +/-5 mil tolerance)
- Edge Plating – 5-10% (plus additional costs associated with reduced #up on the manufacturing panel, if affected)
- Back Drilling – 15-25%
- Castellations – 10-15% depending on size and density
- Cavities – *Avoid if Possible!* – price is design specific



Soldermask & Silkscreen



- Glossy or Matte Soldermask – No Cost Adder
- **Different Color** (non-green) Soldermask – 5-10%, depending on lot size.
  - *Use Caution with **Black or White** Soldermask (cost, capability, and yield issues)*
  - *The cost adder for different soldermask is due to having to break down the set-up for one color in order to use another (time consuming, storage issues, etc.)*
- **Soldermask** is a **Continuous Process**, and the application is independent of the PCB design, except for 2 oz copper and greater (double coat)
- However, the **Silkscreen** process is a **Batch Process**, and is set-up for each particular work order / part number. Only **Printed** nomenclature is a cost adder, an option for greater legibility when text is smaller than standard (~.035” high)
- Customers that use different soldermask colors to identify RoHS or lead-free products should consider using a different silkscreen color instead.

Internal Annular Ring

Internal annular ring measurements DO NOT include through hole plating

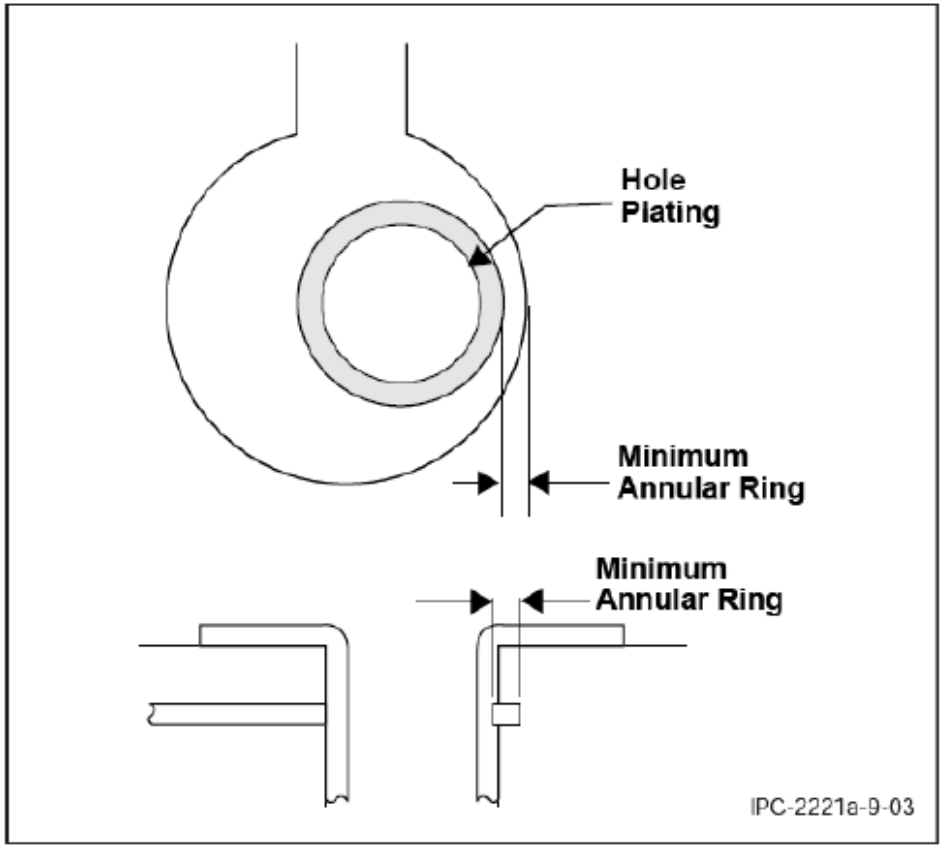
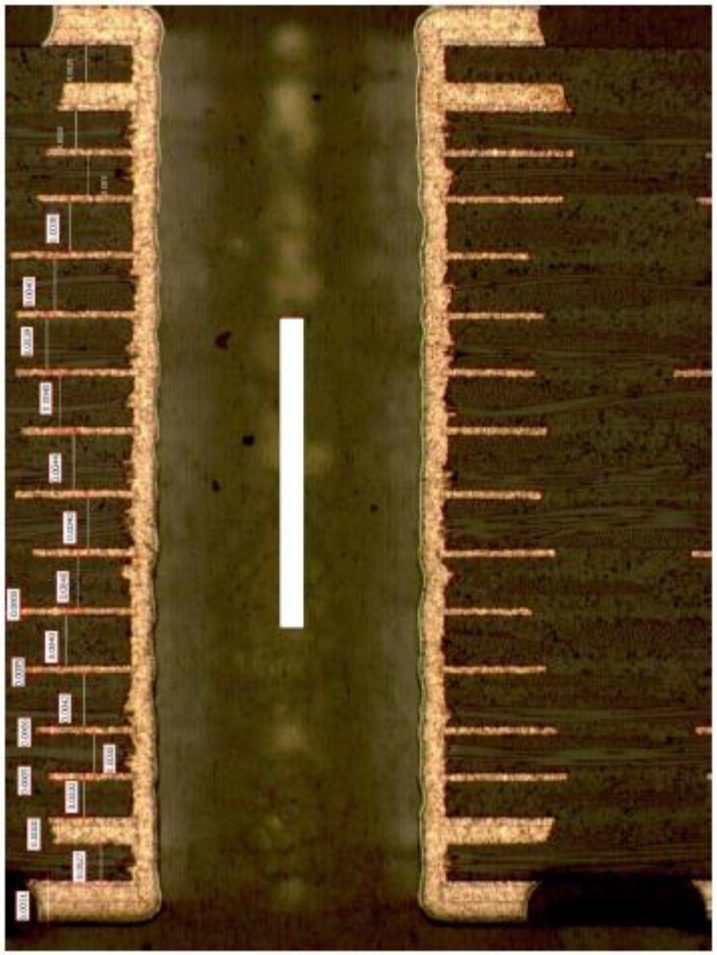
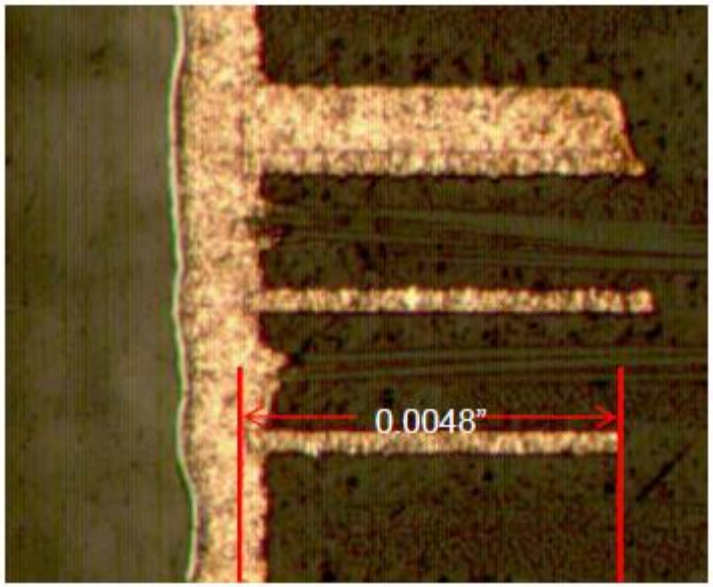


Figure 9-3 Internal Annular Ring

Internal Annular Ring





Internal annular ring is measured from Drilled edge to etched edge of foil.

External Annular Ring

External annular ring measurements DO include through hole plating

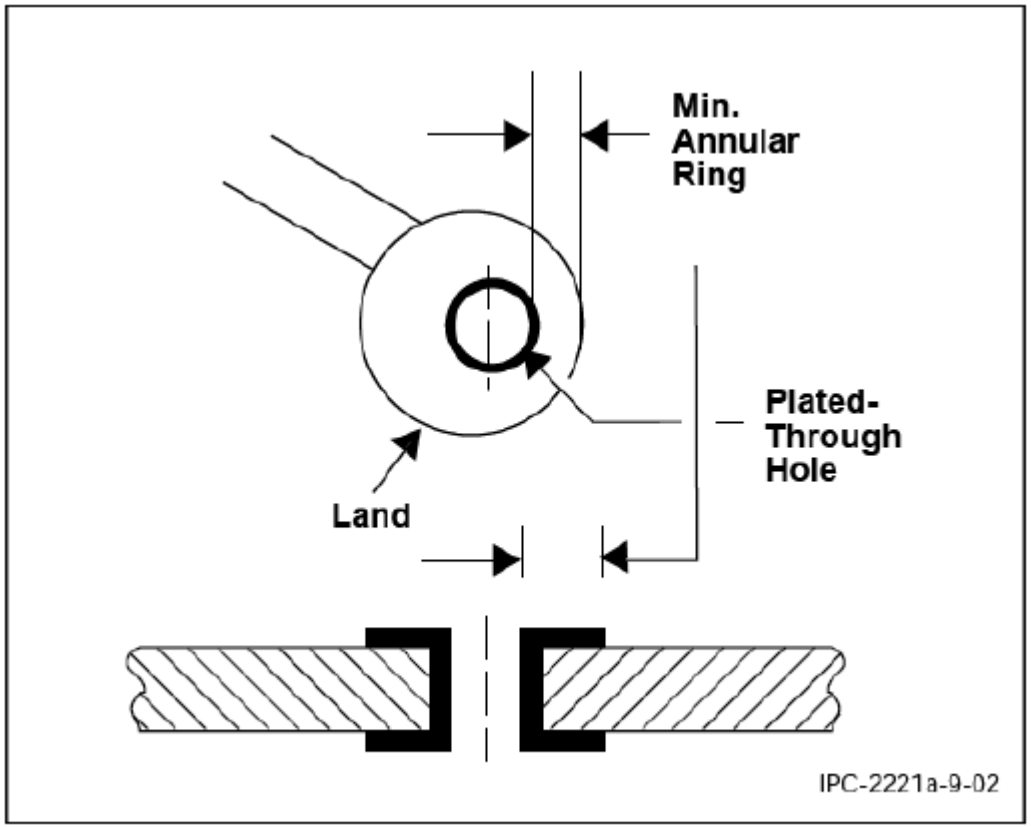
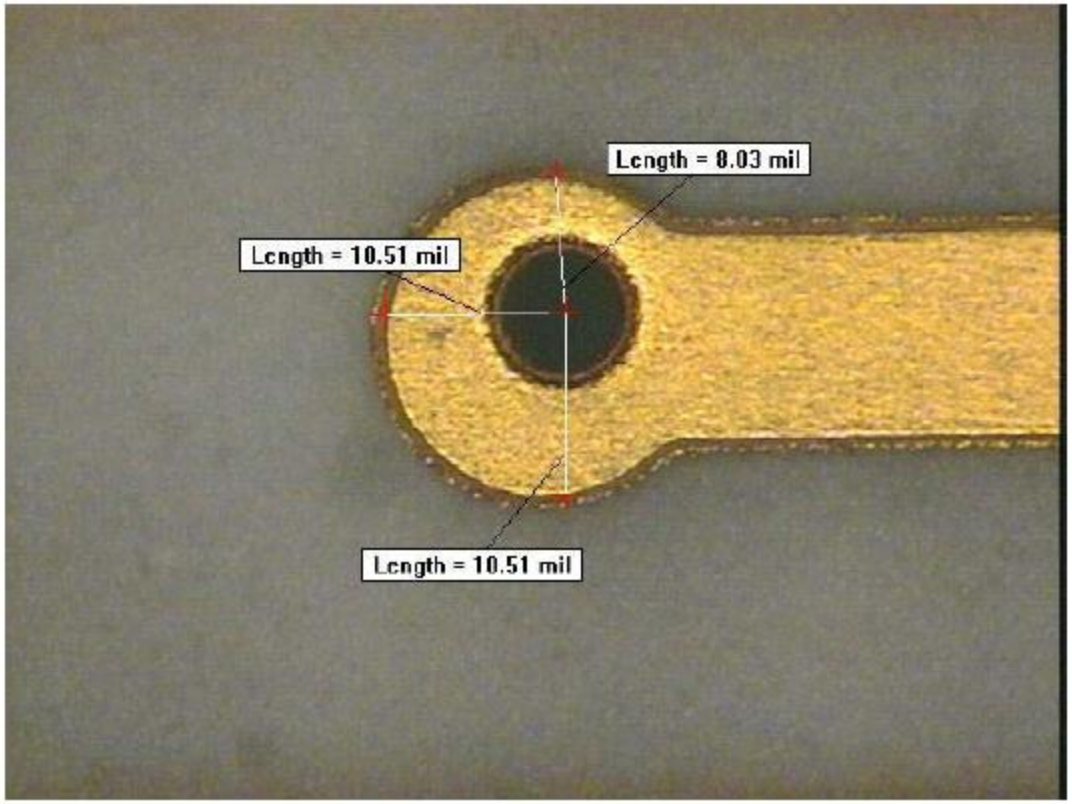
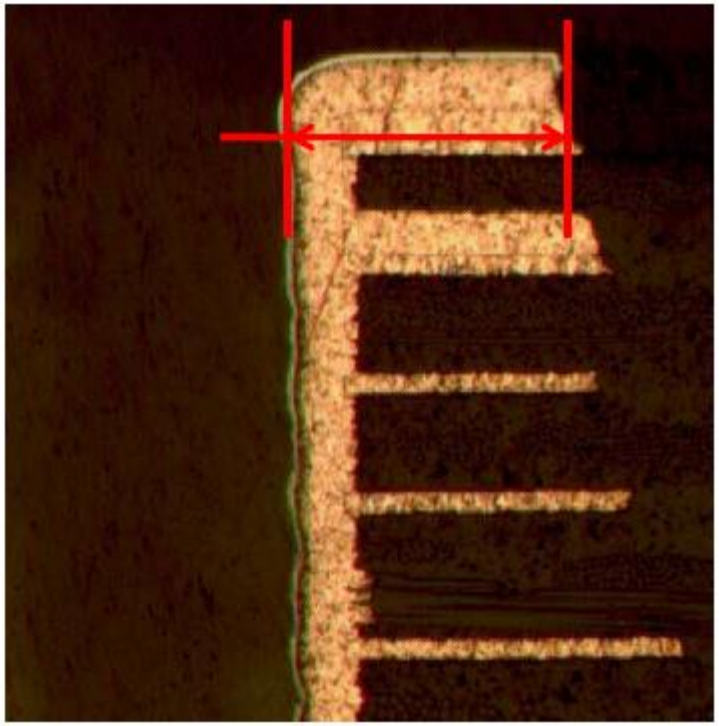


Figure 9-2 External Annular Ring

External Annular Ring





PCB Design Guidelines

Mechanical Drilled Blind, Buried, and Through Holes

	Drill	Pad	Anti-Pad	PCB Thickness	Aspect Ratio
	0.006"	0.016"	0.026"	up to 0.039"	6.5:1
Drill & Pad Diameter	0.008"	0.018"	0.028"	up to 0.062"	7.75:1
IPC Class 2	0.010"	0.020"	0.030"	up to 0.100"	10:01
1/2 oz copper	0.012"	0.022"	0.032"	up to 0.120"	10:01
	0.0135"	0.024"	0.034"	up to 0.135"	10:01

	Drill	Pad	Anti-Pad	PCB Thickness	Aspect Ratio
Drill & Pad Diameter	0.008"	0.023"	0.033"	up to 0.062"	7.75:1
IPC Class 3	0.010"	0.025"	0.035"	up to 0.100"	10:01
1/2 oz copper	0.012"	0.027"	0.037"	up to 0.120"	10:01
	0.0135"	0.028"	0.038"	up to 0.135"	10:01

PCB Design Guidelines

Mechanical Drilled Blind, Buried, and Through Holes

Drill & Pad Diameter	8 Layers or less	>8Layers			
IPC Class 2	Pad dia over drill	Pad dia over drill			
1/4 oz copper	.010"	.010"			
3/8 oz copper	.010"	.010"			
1/2 oz copper	.010"	.010"			
1 oz copper	.012"	.012"			
2 oz copper	.014"	.014"			
3 oz copper	.016"	.016"			
4 oz copper	.018"	.018"			

Drill & Pad Diameter	8 Layers or less	>8Layers			
IPC Class 3	Pad dia over drill	Pad dia over drill			
1/4 oz copper	.013"	.015"			
3/8 oz copper	.013"	.015"			
1/2 oz copper	.013"	.015"			
1 oz copper	.015"	.017"			
2 oz copper	.016"	.018"			
3 oz copper	.019"	.021"			
4 oz copper	.022"	.024"			

Microvia Annular Ring Guidelines

IPC 6016

Qualification & Performance Specification for HDI PCBs

Microvia Design Guidelines

Standard
Pad Diameter = 0.006” +
Laser drill diameter

Advanced
Pad Diameter = 0.005” +
Laser drill diameter

3.4.3 Annular Ring (External)

3.4.3.1 Capture Land to Microvia Capture lands **shall** have tangency at a minimum. Breakout is not allowed, unless the design and procurement documentation specify (i.e., landless microvia). See Figure 3-2.

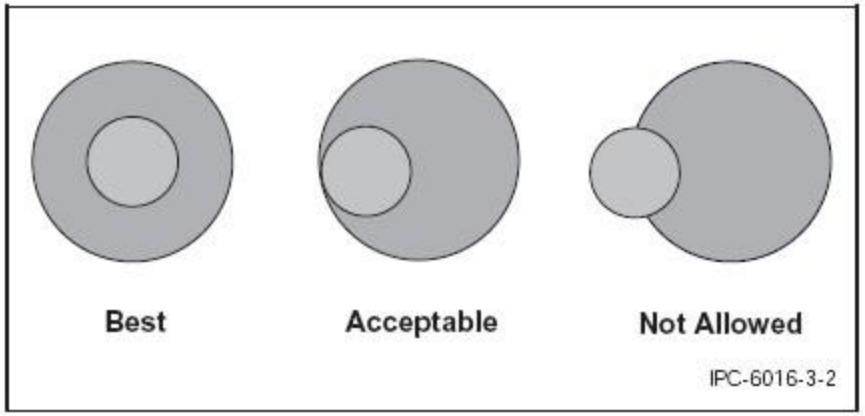


Figure 3-2 Capture Land Registration

3.4.3.2 Plated-Through Holes External annular ring for plated-through holes **shall** be in accordance with the applicable sectional performance specification (i.e., IPC-6012, IPC-6013, etc.).

PCB Design Guidelines

Laser Drilled Blind & Buried Microvias

Attritube	Standard	Advanced	Engineering	DpMV™	
Pad diameter	0.012"	0.010"	0.0086"	0.012"	
Laser drill diameter	0.006"	0.005"	0.005"	0.006"	
Dielectric thickness	0.0025" - 0.003"	0.0025" - 0.004"	0.0025 - 0.004"	0.006"	
Aspect Ratio	0.4:1 - 0.5:1	0.5:1 - 0.8:1	0.5:1 - 0.8:1	one-to-one	
Anti Pad	0.005"/side	0.004"/side	0.004"/side	0.004"/side	
Dog Bone Offset	0.005" space Pad-Pad	Pads Tangent	0.001" Pad overlap	0.005"Space	

TTM Technologies

PCB Design Guidelines: As Cu thickness increases, so do lines/spaces

Internal & External Trace Widths

		Standard	Advanced	Engineering	
	External Trace	.004"	0.003"	0.0025"	
Trace & Space	External Space	.004"	0.003"	0.0025"	
	Internal Trace	.004"	0.003"	0.0025"	
	Internal Space	.004"	0.003"	0.0025"	
Cu Weight		Trace & Space	Trace & Space	Trace & Space	Finished Weight
Plated Layer starting	External 1/4 oz		0.003"	0.0025"	average 0.0016"
Plated Layer starting	External 3/8 oz		0.003"	0.00275"	average 0.0018"
Plated Layer starting	External 1/2 oz	0.004"	0.0035"		average 0.0021"
Plated Layer starting	External 1 oz	0.005"	0.0045"		average 0.0026"
Plated Layer starting	External 2 oz	0.008"	0.0075"		average 0.0038"
Plated Layer starting	External 3 oz	0.011"	0.0105"		average 0.005"
Plated Layer starting	External 4 oz	0.014"	0.0135"		average 0.0062
Plated Layer starting	External 5 oz	0.017"	0.0165"		
non-plated Layer starting	Internal 1/4 oz		0.003"	0.0025"	
non-plated Layer starting	Internal 3/8 oz		0.003"	0.00275"	0.0004"
non-plated Layer starting	Internal 1/2 oz	0.004"	0.0035"		0.0006"
non-plated Layer starting	Internal 1 oz	0.005"	0.004"		0.0012"
non-plated Layer starting	Internal 2 oz	0.007"	0.006"		0.0026"
non-plated Layer starting	Internal 3 oz	0.009"	0.008"		0.004"
non-plated Layer starting	Internal 4 oz	0.011"	0.010"		0.0054"
non-plated Layer starting	Internal 5 oz	0.013"	0.012		0.0068"

PCB Design Guidelines

		Standard	Advanced
Drill-to-Copper		0.008"	0.0065"
Anti-Pad		0.010" over Pad dia	0.008" over Pad dia
Thermal Relief	non Plated Layer	0.006"/side	0.004"/side
	Plated Layer	.008"/side	.006"/side
Circuit to PCB edge		0.025"	0.010"
Plane to PCB edge		0.025"	0.010"
Routing Tolerance		+/- 0.005"	+/- 0.002"
Edge of hole barrel to PCB Edge		0.025"	0.020"
Solder Mask Dam		0.004" min	0.003" min
Filled Vias	Conductive	0.012" drill min	0.010" drill min
	non-conductive	0.010" drill min	0.008" drill min

Via-in-Pad filled & plated over require wrap around plating

wrap around plating reduces trace & space capabilities on plated layers

TTM Technologies

PCB Design for Cost

Copper - The conductive layer of the PCB

- Thickness is often specified in terms of 'weight' (oz/ft^2)
  - 1 oz copper weight = 1.35 mil
  - 1.35 mil = thickness of 1ft^2 x 1ft^2 copper square that weighs 1 oz
- Different copper weights are used depending on whether the conductor or plane will be used to carry a high current
  - Most common thickness is ½ oz (= 0.68 mil thickness)
  - Other common thicknesses include 1 oz, and 2 oz
  - Thickness above 2 oz will require design review and factory approval
    - Adds 15-20% (Design constraints)
- External layers of a PCB are always plated, and so the final thickness of copper will include the plating thickness

PCB Materials

Base Laminate Materials are comprised of three components:

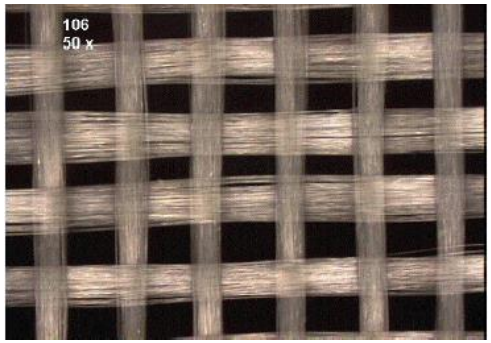
- ***Copper Foil***
- ***Woven Glass Fabrics***
- ***Resin***

PCB Construction

The printed circuit board stack-up is the combination of various material types, cores, and prepreg, including copper and dielectric thicknesses.

- **Core** = Fully cured dielectric between 2 copper foil layers
- **Prepreg** = partially cured dielectric used to bond cores and/or foil in the stack-up
- **Copper Foil** – The copper used on outer/inner (subs) layers of the PCB or on the core layers

Prepreg Glass Styles



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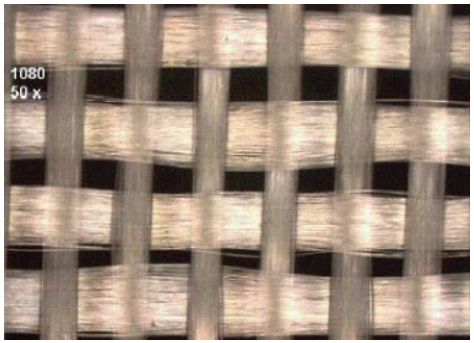
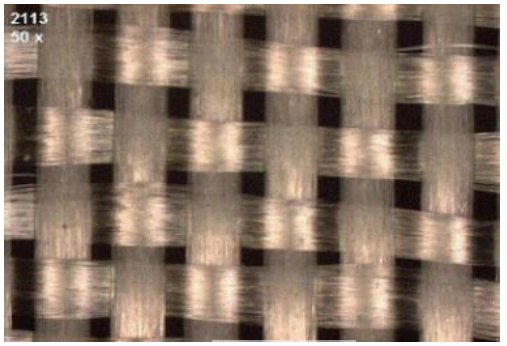


1080



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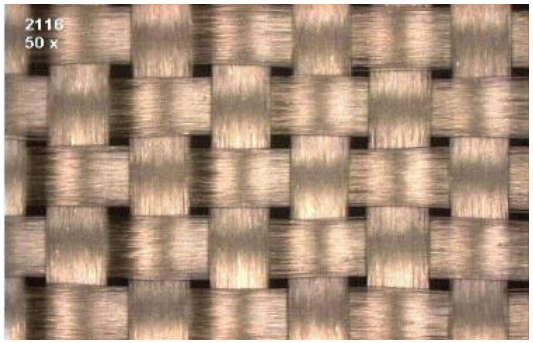

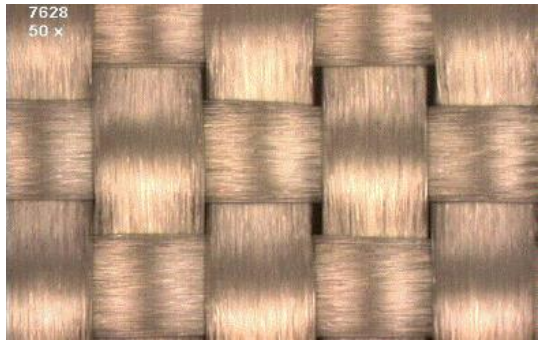

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Note: Due to material availability and general preferences, glass styles and resin contents used in Asia are often different to those used in North America

TTM Technologies

Material Selection – High Performance

What material is best for a high-performance design?

- **Signal Integrity** performance (signal speed and signal loss) is often
- the driving factor in going to a higher cost material set

- Other factors include:
  - ***Thermal*** *performance*
  - ***Assembly*** *and* ***Rework***
  - *Long term* ***Reliability***
- Going to a 'higher speed' material provides much **improved** signal loss (**attenuation**), but trace lengths also play a major role in determining loss characteristics
  - *Normally, once speeds of* ***2.5Gbps*** *(1.25GHz) are employed, higher speed materials should be considered*
  - *Signal loss on* ***shorter traces*** *is less, and standard high-Tg* ***FR4*** *can therefore be used at speeds as high as* ***10Gbps*** *as long as the trace lengths are short enough (a good rule of thumb is 3" or less)*

Laminate Cost Factors Based on Resin System

Material Group/ Resin System	Vendor Specific	Cost Factor
High Tg FR4 (Baseline sqft. Price)	Isola 370 HR	1
High Tg/Reliability-Filled	Nelco 4000-29, Isola 370HR	1
High Speed/ Mid Low Loss	Rogers Theta	1.1
High Speed/ Mid Low Loss	Nelco 4000-13 EP, Isola FR408	1.2
High Speed/ Low Loss	Nelco 4000-13EP SI	3X
High Speed/ Low Loss	Panasonic Megtron 6	4X
Polyimide	Nelco N7000-2, Isola P96, Arlon 35N	3X
High Frequency	Rogers 4350B, RO4003	5X
BT Packaging Substrate	Nelco N5000-32	3X

Note: Based on square foot pricing

Material Selection – High Speed Options

- **Pure package with desired high-speed material**
  - *Although this will provide **superior performance**, it will also be the **most expensive** option, and should be used when all PCB layers require improved signal performance*

- **Hybrid Builds**
  - *Often, high-speed signals can fit on just a few of the layers within the build.*
  - *Utilizing the high speed material on either one or both external layers (with standard **FR4 on the remaining layers**) may provide a desirable performance/cost benefit*
  - *Hybrid builds should use a core construction (cores on external dielectrics) in order to maximize dielectric thickness consistency*

Check with factory for material compatibility

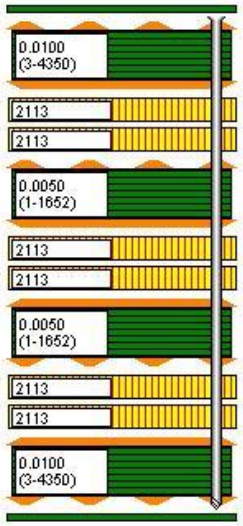
Mixed Materials (Hybrid Builds) Symmetry

- When using a mixed material build, consider the effects of warpage due to the mixing of materials, and take steps to eliminate it
- PWB cost may increase, but the build will be more robust

PREFERRED

Layer	Thickness	Description
	0.0005	Taiyo 4000-MP
Layer - 1	0.0020	1/2oz Sig (Std Plt)
	0.0100	R4350B
Layer - 2	0.0006	1/2oz P/G
	0.0080	370H
Layer - 3	0.0006	1/2oz Sig
	0.0050	370H
Layer - 4	0.0006	1/2oz P/G
	0.0081	370H
Layer - 5	0.0006	1/2oz P/G
	0.0050	370H
Layer - 6	0.0006	1/2oz Sig
	0.0080	370H
Layer - 7	0.0006	1/2oz P/G
	0.0100	R4350B
Layer - 8	0.0020	1/2oz Sig (Std Plt)
	0.0005	Taiyo 4000-MP

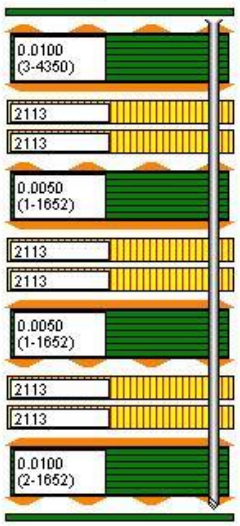
Rigid Stack



ACCEPTABLE

Layer	Thickness	Description
	0.0005	Taiyo 4000-MP
Layer - 1	0.0020	1/2oz Sig (Std Plt)
	0.0100	R4350B
Layer - 2	0.0006	1/2oz P/G
	0.0080	370H
Layer - 3	0.0006	1/2oz Sig
	0.0050	370H
Layer - 4	0.0006	1/2oz P/G
	0.0081	370H
Layer - 5	0.0006	1/2oz P/G
	0.0050	370H
Layer - 6	0.0006	1/2oz Sig
	0.0080	370H
Layer - 7	0.0006	1/2oz P/G
	0.0100	370H
Layer - 8	0.0020	1/2oz Sig (Std Plt)
	0.0005	Taiyo 4000-MP

Rigid Stack



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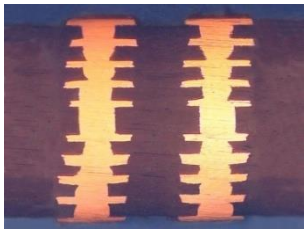
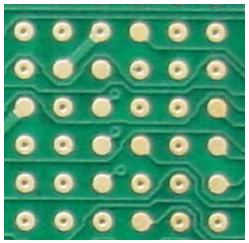


Factors Impacting PCB Yield



Yield will impact cost as PCB technologies are increased. Some of the major factors impacting yield are as follows:

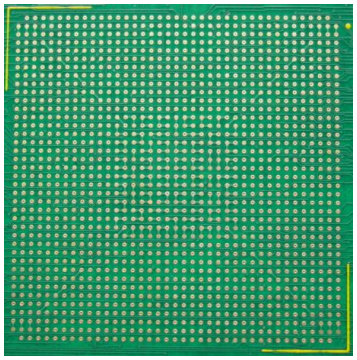
Aggressive PCB design geometries: ***

- *Line Widths and Spacing Less than **4 mils** (0.1mm)*
- *Drill Diameters Less than **10 mils** (0.25mm)*
- *Pad Sizes Less than **drill dia. + 10 mils** (0.25mm) **
- *Aspect Ratio greater than **10:1***
- *Drilled Hole to Copper Spacing Less than **8 mils** (0.2mm)*
- *Anti-Pads Less than **drilled dia. + 18 mils** (0.46mm) **

Complexity of the manufacturing process (**Added processes**)

- ***HDI** is a key contributor to higher complexity/ cost.*

HDI (High Density Interconnect)



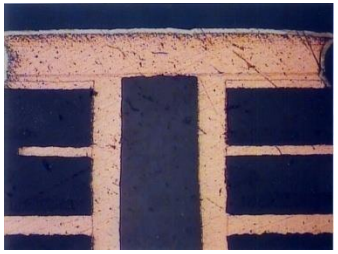
- The decision to go to high-density interconnect (**HDI**) technology can add **cost** to the PCB
- In many cases (0.5mm BGA, 0.4mm BGA, via-in-pad, reduced PCB size), the use of HDI is **unavoidable**

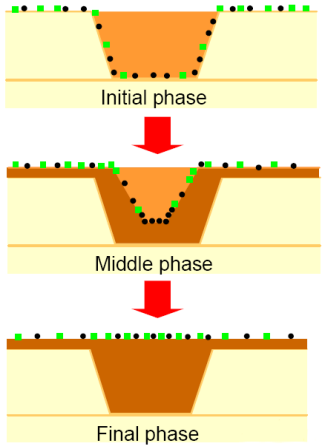
HDI – Technology Adds Cost (and Time)

Technology and Density Cost Adders include:

- **Blind** Vias (***Laser***): **10-15%** per Layer (second side is **5%**)
- **Buried** Vias (***Laser***): **40-50%** (plus any sub filling costs if stacked)
- **Blind** Vias (***Mechanical***): **50-100%** (plus any sub filling costs if stacked)

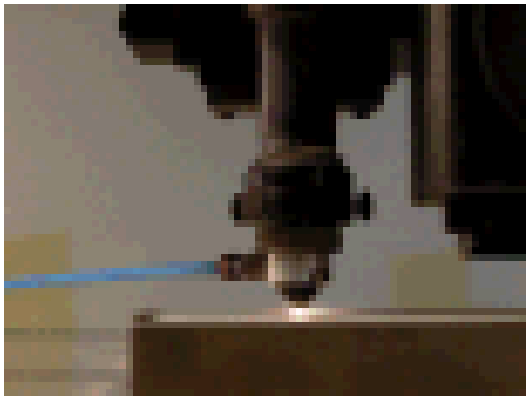
- Through **Hole Fill** (*non-conductive*): **20%** per Panel
- **Sub**assembly **Hole Fill** (*non-conductive*): **15%** per Layer
- Microvia **Copper Fill**: **20%** per Layer





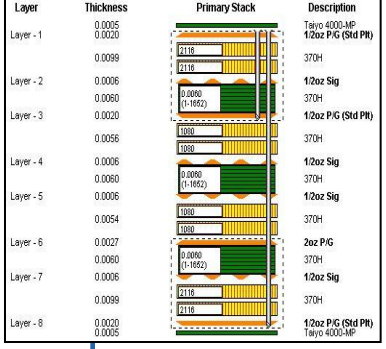
- Buried **Capacitance**: **~5%** per Std BC Core (more for high performance matl's)
- Buried **Resistance**: ~**75%** per Resistive Layer

HDI Multipliers



- Adders for Hole Fill, Laser Microvias, and/or Mechanical Blind/Buried holes are for the **process itself** and are not dependent on the total number of holes
  - *Once you add one blind/buried/filled via, you can use as needed to take advantage of the increased density*
- When Via Fill is considered, maintain a single hole size for optimized filling
  - *Copper filling **multiple microvias** on the same layer is as cost effective as filling just one microvia*

Build Complexity



- Laser drilled microvias with internal buried vias are preferred over mechanical blind vias for ease of manufacture, especially with respect to external layer wrap plate processing

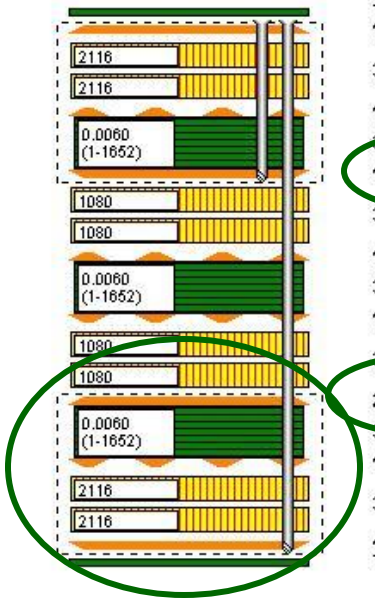
- When considering blind vias, the following rules of thumb will help make the design more robust:
  - Design the build so that the blind vias are **symmetrical** about the center axis and extend to the middle
    - *Example: 12L PCB with blinds L1-6 & L7-12, instead of L1-5 & 8-12.*
  - If possible, consider **back drilling** on long blind vias
    - *Example: 12L PCB with blinds L1-5 (consider a straight build with back drills)*
    - *Also less expensive and less time consuming than multiple lams*
  - If only one set of blind vias is required, the build should be **mirrored** on the opposite side using a **dummy subassembly** and heavier copper to mimic the extra Cu plating on the blind via subassembly

Asymmetric Subassemblies

On subassemblies where the build is unbalanced, use **dummy subassemblies** and **copper weight changes** to force the build into a more symmetric state

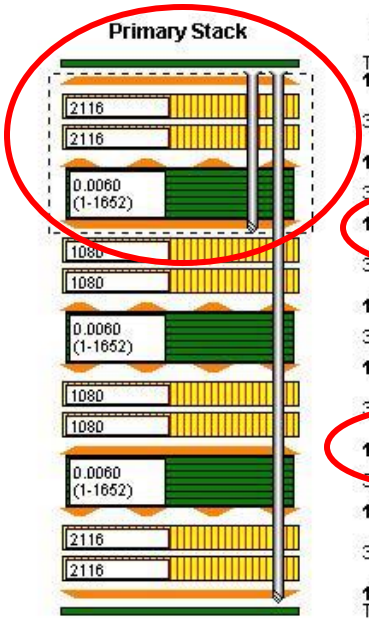
PREFERRED

Layer	Thickness	Description
	0.0005	Taiyo 4000-MP
Layer - 1	0.0020	**1/2oz P/G (Std Plt)**
	0.0099	370H
Layer - 2	0.0006	**1/2oz Sig**
	0.0060	370H
Layer - 3	0.0020	**1/2oz P/G (Std Plt)**
	0.0056	370H
Layer - 4	0.0006	**1/2oz Sig**
	0.0060	370H
Layer - 5	0.0006	**1/2oz Sig**
	0.0054	370H
Layer - 6	0.0027	**2oz P/G**
	0.0060	370H
Layer - 7	0.0006	**1/2oz Sig**
	0.0099	370H
Layer - 8	0.0020	**1/2oz P/G (Std Plt)**
	0.0005	Taiyo 4000-MP



NOT PREFERRED

Layer	Thickness	Description
	0.0005	Taiyo 4000-MP
Layer - 1	0.0020	**1/2oz P/G (Std Plt)**
	0.0099	370H
Layer - 2	0.0006	**1/2oz Sig**
	0.0060	370H
Layer - 3	0.0020	**1/2oz P/G (Std Plt)**
	0.0056	370H
Layer - 4	0.0006	**1/2oz Sig**
	0.0060	370H
Layer - 5	0.0006	**1/2oz Sig**
	0.0060	370H
Layer - 6	0.0006	**1/2oz P/G**
	0.0060	370H
Layer - 7	0.0006	**1/2oz Sig**
	0.0099	370H
Layer - 8	0.0020	**1/2oz P/G (Std Plt)**
	0.0005	Taiyo 4000-MP



TTM Technologies

PCB Cost Index

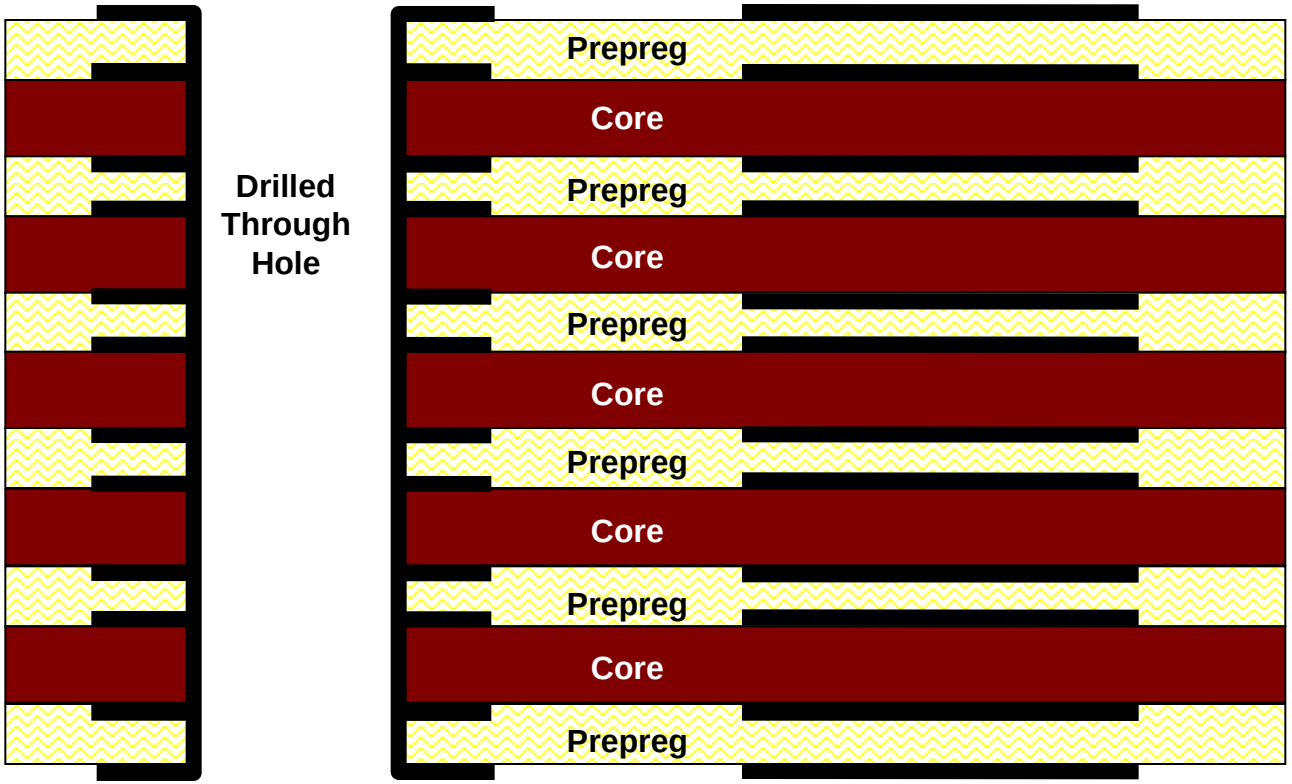
The following examples use a 12 layer printed circuit to illustrate how different via configurations impact manufacturing complexity. We start with a standard through hole design and then add blind and buried vias, Microvias, and Via-In-Pad technologies.

Major Process Operations

Printed circuit fabrication requires many detailed processing steps. However, for the purpose of developing a basic cost index for engineering purposes, one way to look at the fabrication process is to keep track of the number of major operations:

- Inner layer processing: Photo image and etch
- Pattern plated layer processing: Photo image, copper plate and etch
- Via-In-Pad Wrap plating process (Copper panel plate + Image and barrel plate)
- Blind Via Wrap plating process (Copper panel plate)
- SMV plating process (Photo image and copper button plate)
- High pressure lamination
- Mechanical drilling
- Laser drilling

12 Layer PCB



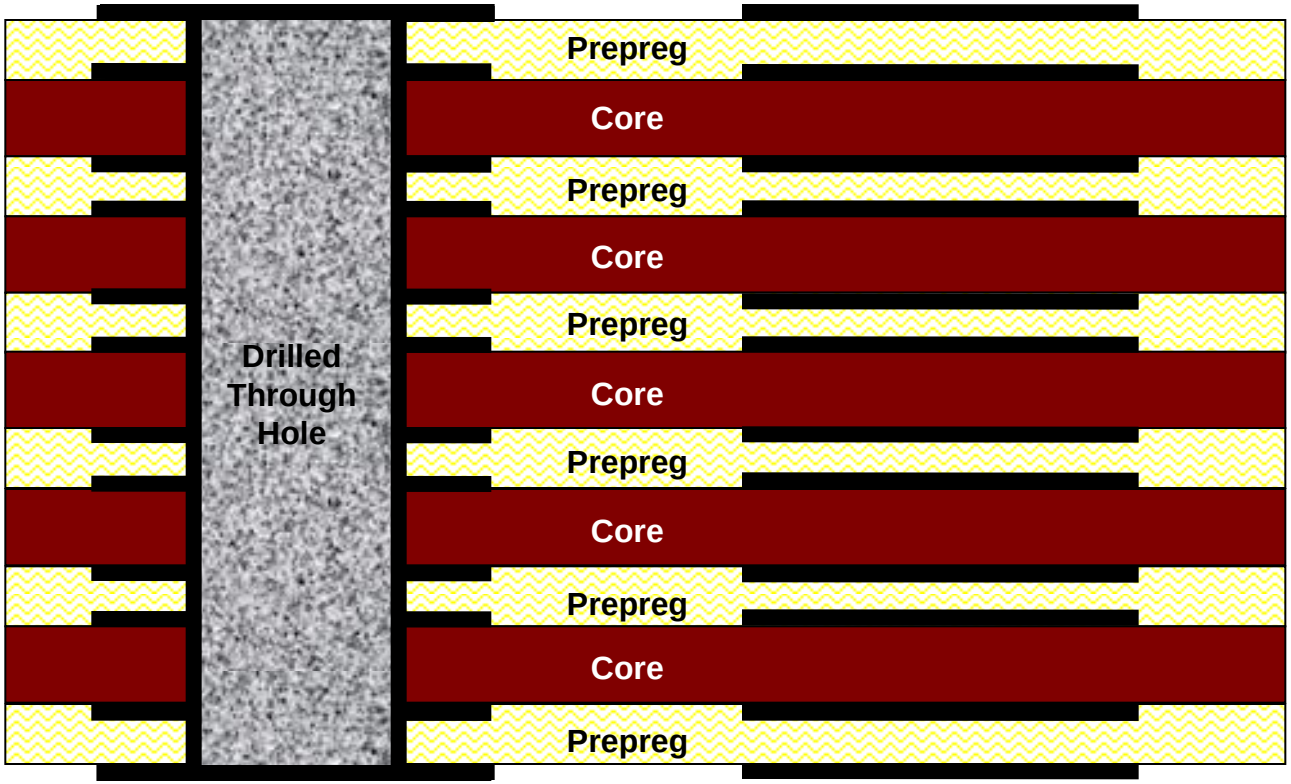
5	Inner layer processing
1	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
0	SMV plate process
1	**Lamination**
1	Mechanical drilling
0	Laser drilling
Index Total	8

Note: to add or subtract layer pairs (i.e. 2 layers) the index will only change by 1 since each inner layer process produces two layers.

Example: For 14 layers the index would be 9, and for 10 layers the index would be 7

Via Structure: Basic 12 layer PCB with through hole via
(Standard through hole PCB)

12 Layer PCB



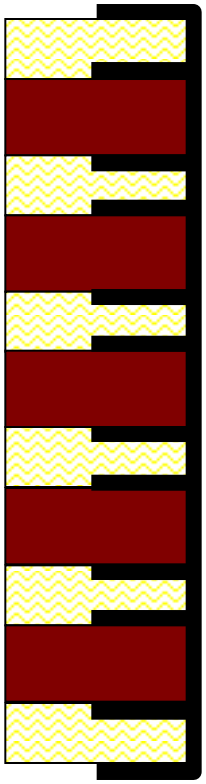
5	Inner layer processing
1	Cu pattern plated layer
1	VIP wrap plate = 2x 2
0	BV wrap plate
0	SMV plate process
1	**Lamination**
1	Mechanical drilling
0	Laser drilling
Index Total	10

The via-in-pad process requires the filled vias to be plated separately, and also requires a fill and planarize step

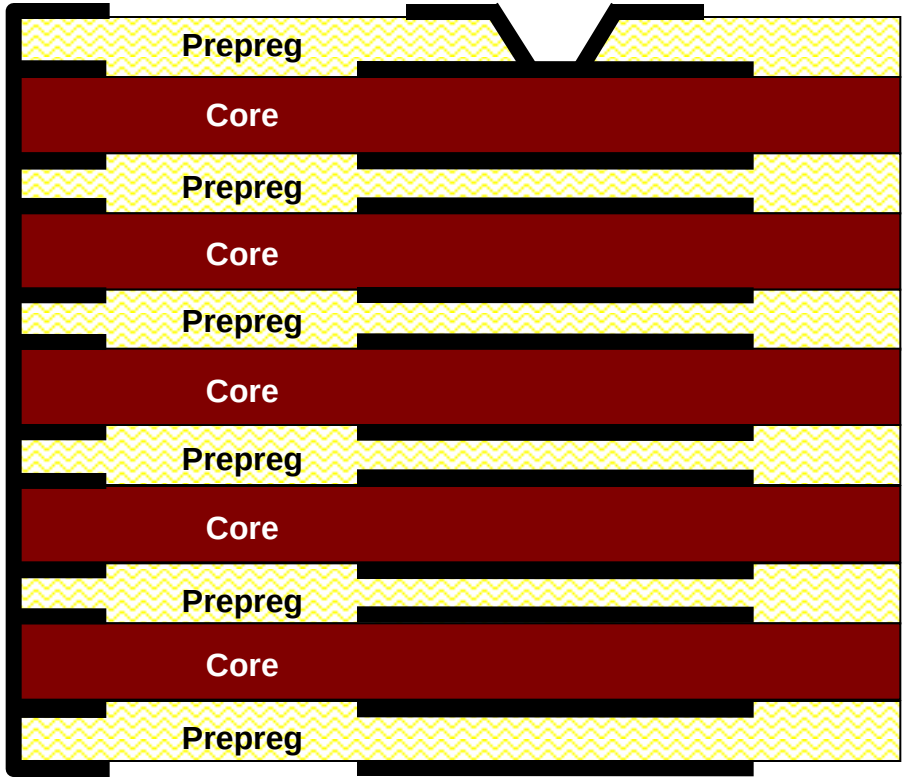
Via Structure: Through hole via-in-pad (VIP)

(PCB with **0.8mm** pitch BGA)

12 Layer PCB



Drilled Through Hole

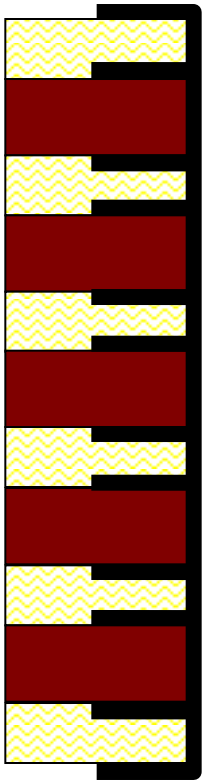


5	Inner layer processing
1	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
0	SMV plate process
1	**Lamination**
1	Mechanical drilling
1	Laser drilling
Index Total	9

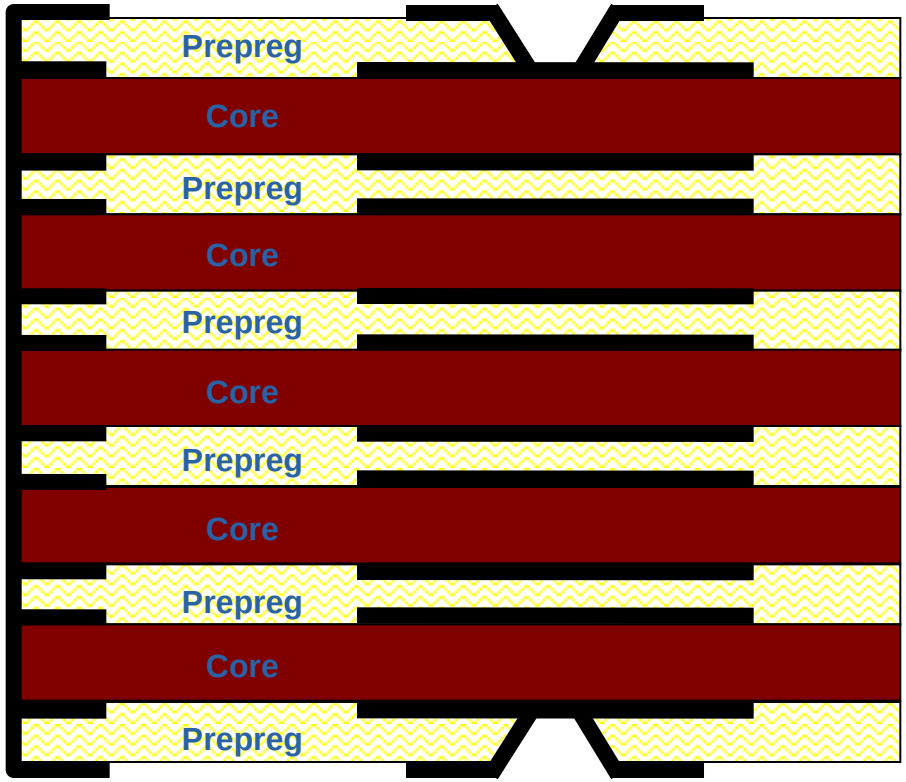
Via Structure: Through hole and laser microvia L1-2

(PCB with **0.65mm** pitch BGA or less – low pin count)

12 Layer PCB



Drilled Through Hole

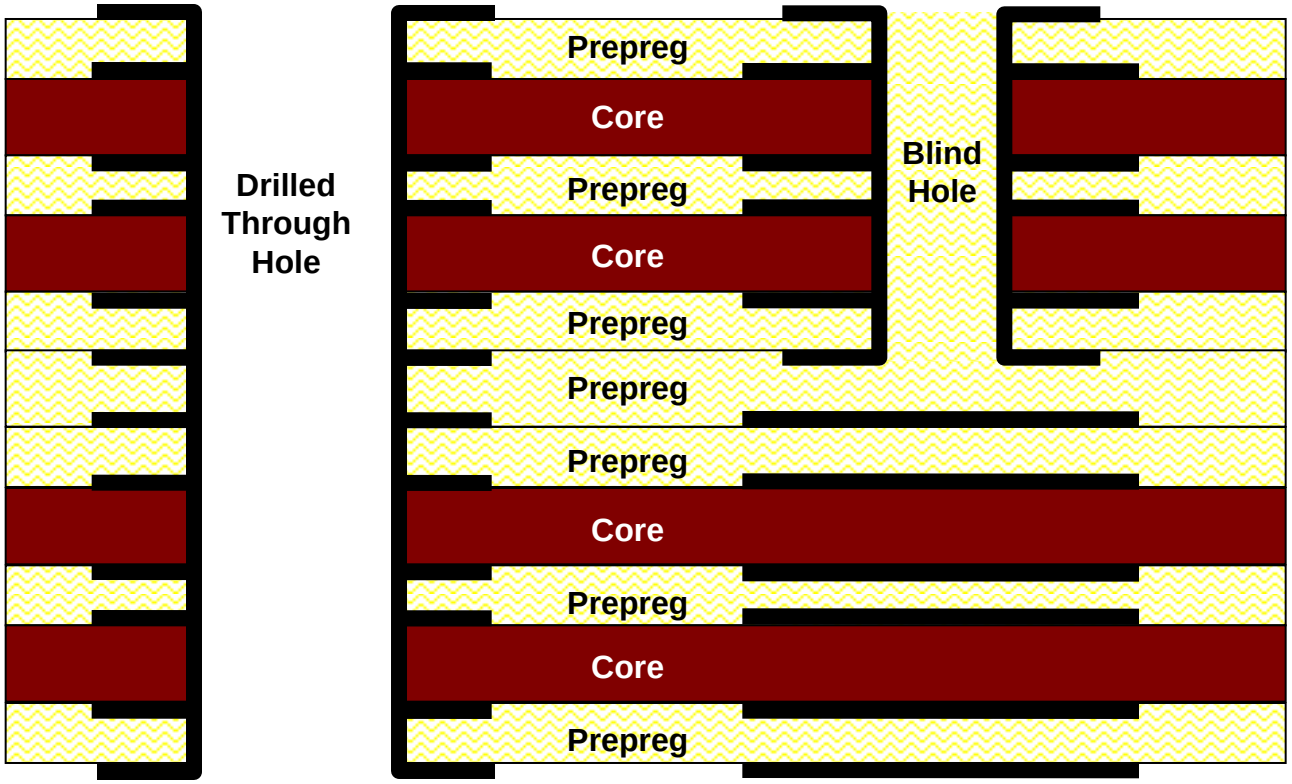


5	Inner layer processing
1	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
0	SMV plate process
1	**Lamination**
1	Mechanical drilling
2	Laser drilling
Index Total	10

Via Structure: Through hole and microvia L1-2, L12-11

(PCB with **0.65mm** pitch BGA or less – low pin count)

12 Layer PCB



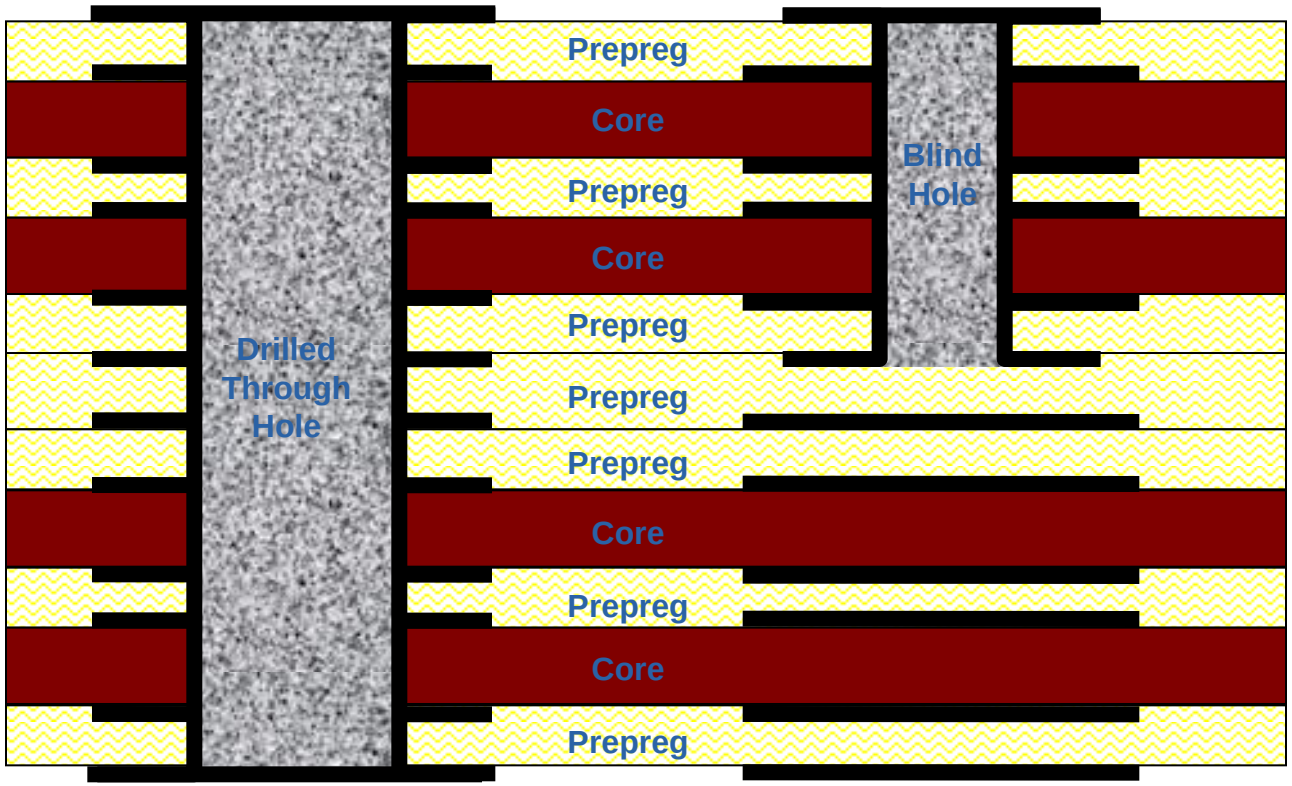
4	Inner layer processing
2	Cu pattern plated layer
0	VIP wrap plate = 2x 0
1	BV wrap plate
0	SMV plate process
2	**Lamination**
2	Mechanical drilling
0	Laser drilling
Index Total	11

Via Structure: Through hole and blind via L1-6

(Increased density PCB with **larger BGAs**, typically 1.0mm or greater)

TTM Technologies

12 Layer PCB

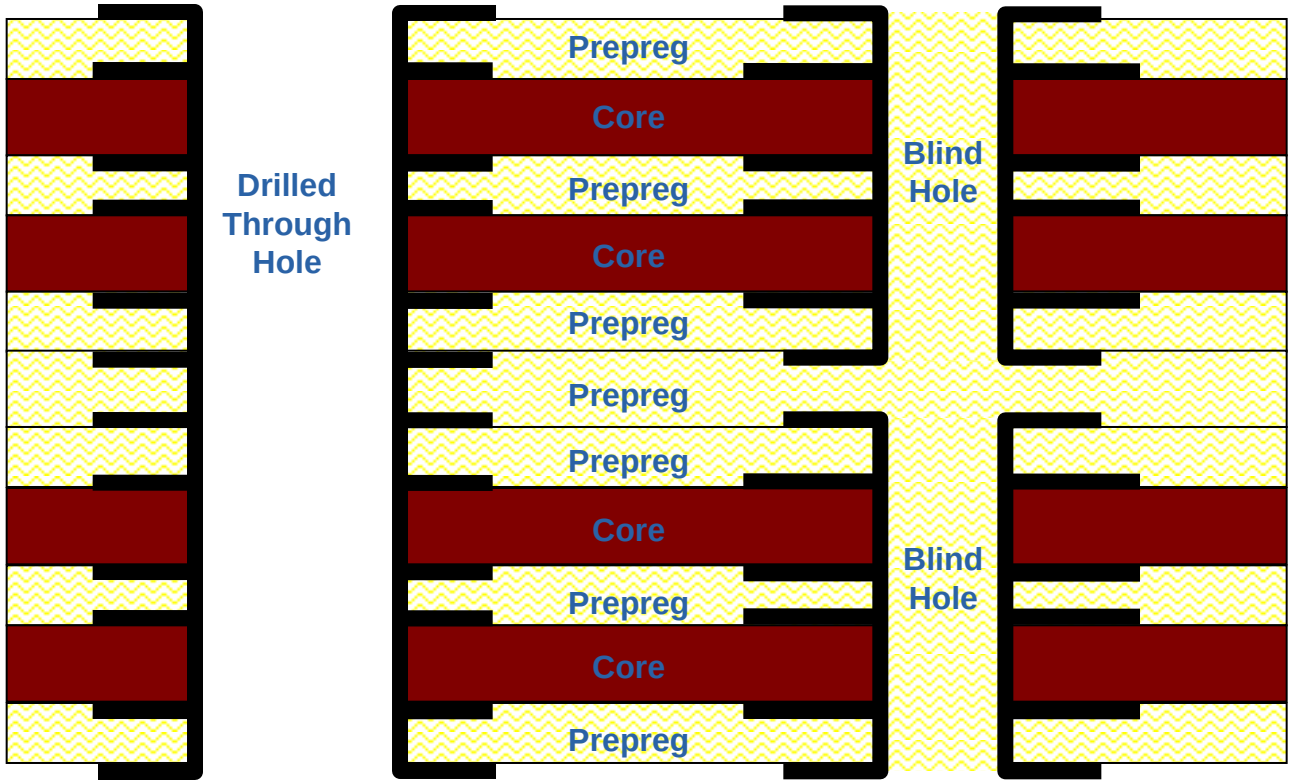


4	Inner layer processing
2	Cu pattern plated layer
2	VIP wrap plate = 2x 4
0	BV wrap plate
0	SMV plate process
2	**Lamination**
2	Mechanical drilling
0	Laser drilling
Index Total	14

Via Structure: Through hole and blind via L1-6 with via-in-pad (two wrap cycles)

(Increased density PCB with **0.8mm** pitch BGAs)

12 Layer PCB

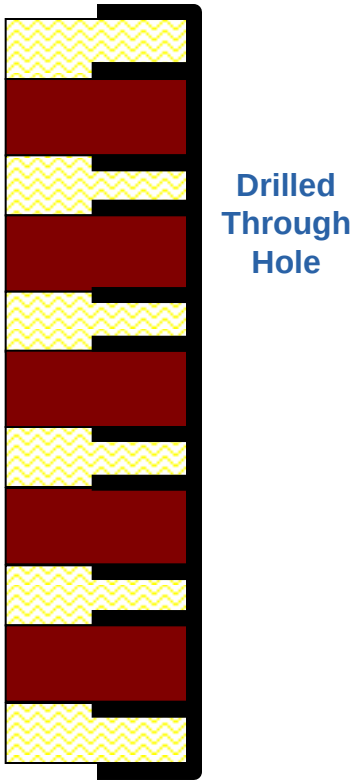


4	Inner layer processing
3	Cu pattern plated layer
0	VIP wrap plate = 2x 0
2	BV wrap plate
0	SMV plate process
3	**Lamination**
3	Mechanical drilling
0	Laser drilling
Index Total	15

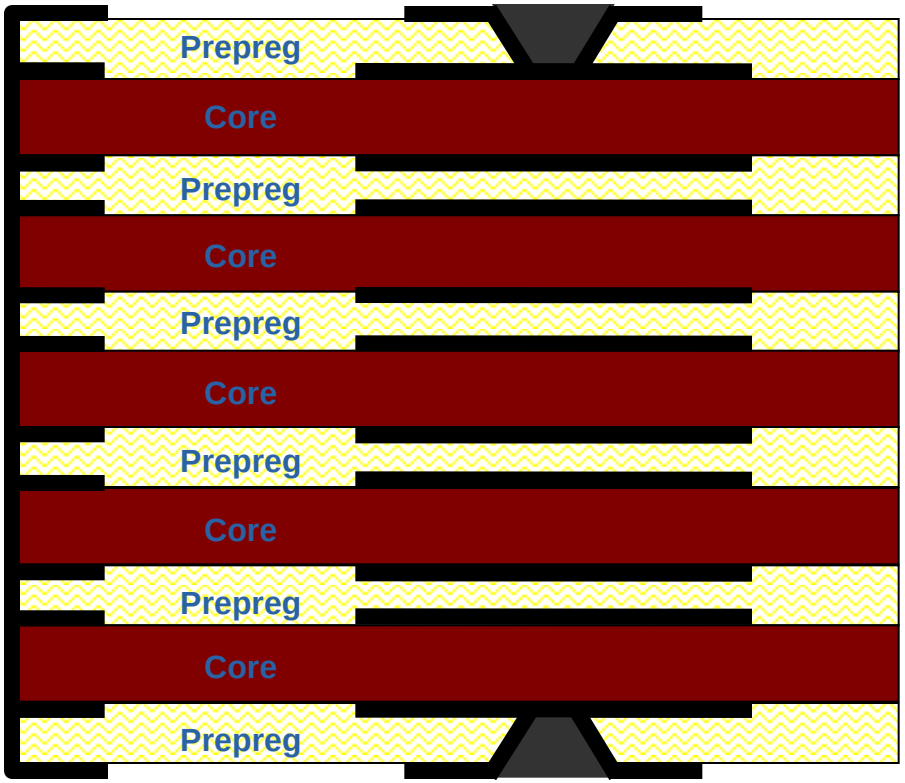
Via Structure: Through hole, blind via L1-6 and L7-12

(Increased density PCB with **0.8mm** pitch BGAs on **both sides**)

12 Layer PCB



Drilled Through Hole



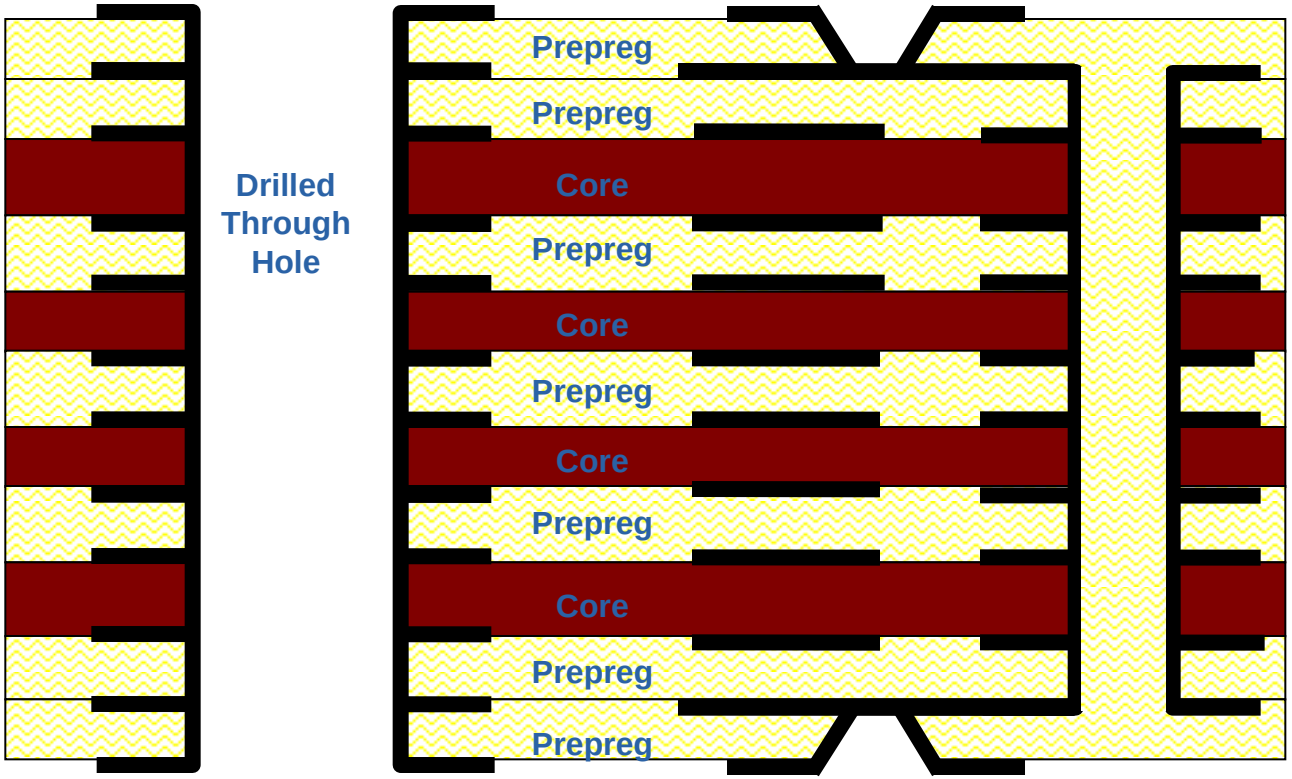
5	Inner layer processing
1	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
1	SMV plate process
1	**Lamination**
1	Mechanical drilling
2	Laser drilling
Index Total	11

Via Structure: Through hole and microvia-in-pad L1-2, L12-11 with MV copper fill

(PCB with **0.5mm** BGA or less – low pin count – via in pad)

TTM Technologies

12 Layer PCB



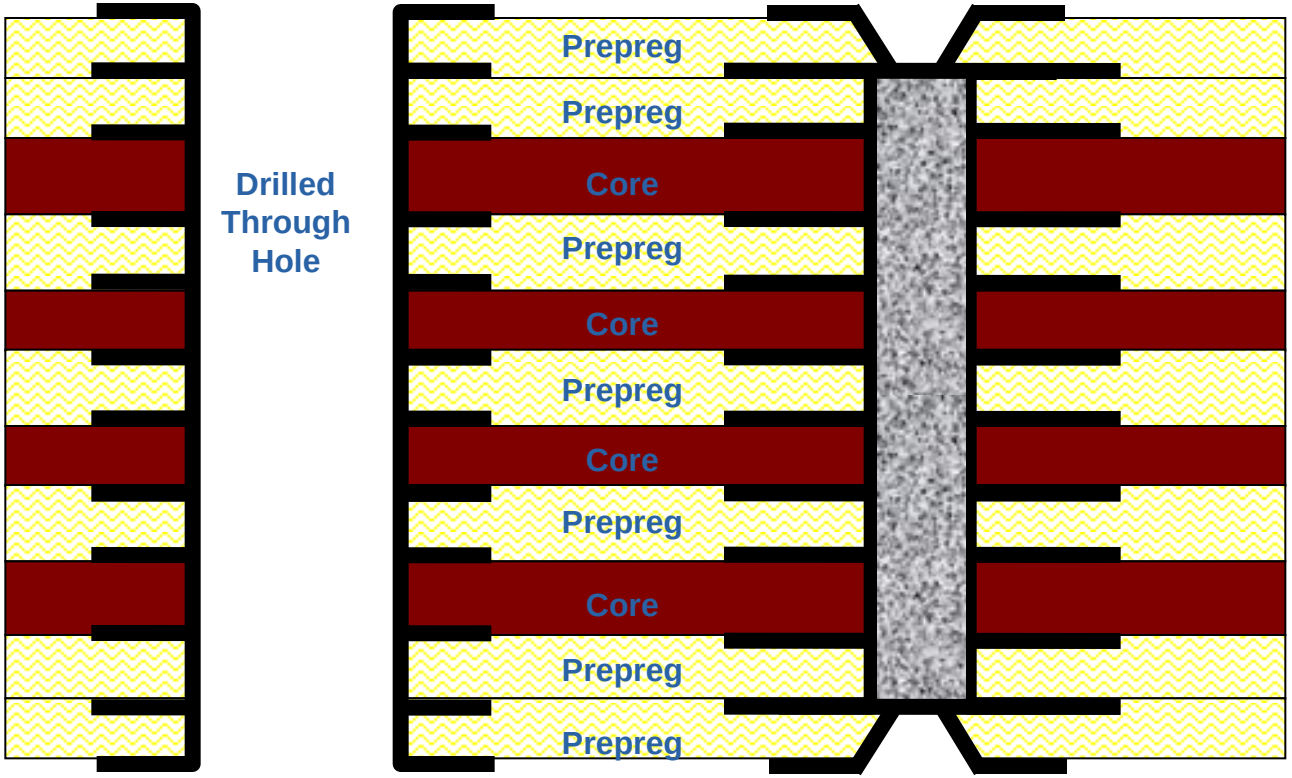
4	Inner layer processing
2	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
0	SMV plate process
2	**Lamination**
2	Mechanical drilling
2	Laser drilling
Index Total	12

Via Structure: Through hole and microvia L1-2, L12-11, with buried via L2-11

(Most popular HDI construction – **increased density**, **0.5mm** BGA, medium pin count)

TTM Technologies

12 Layer PCB

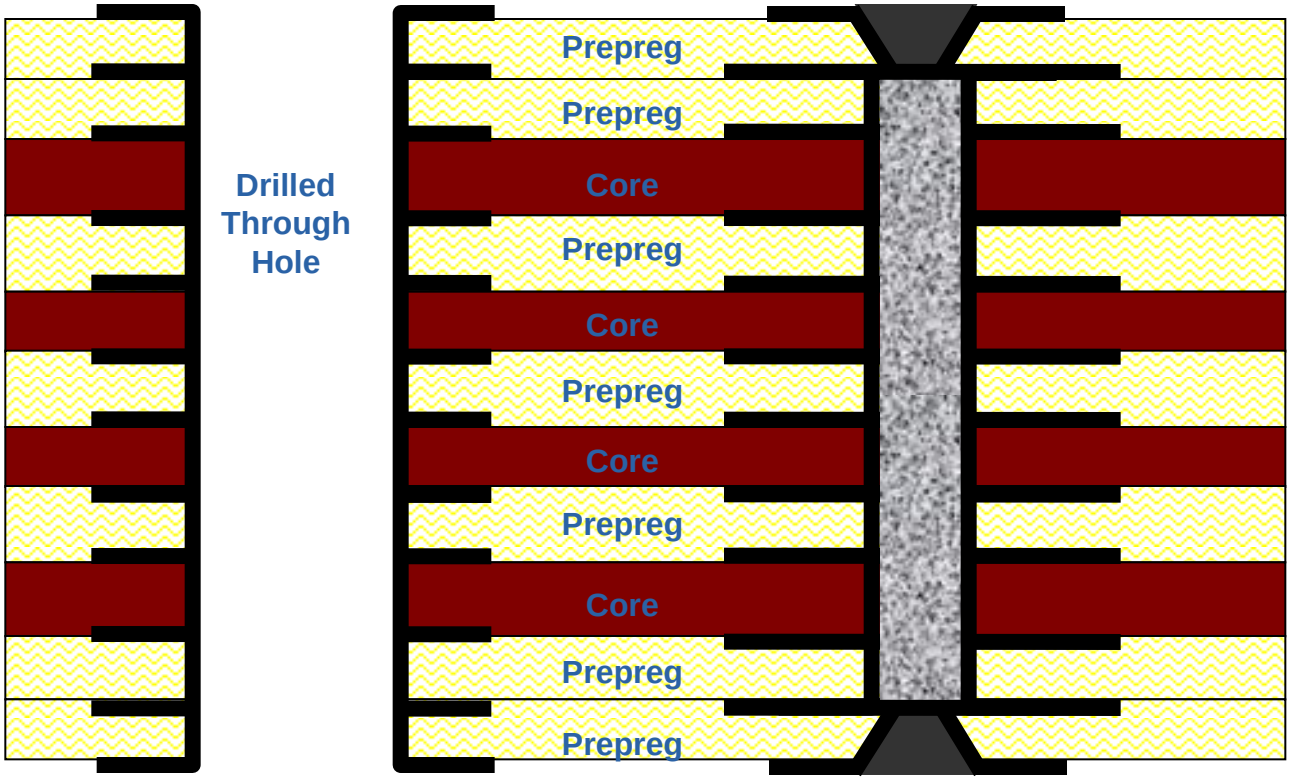


4	Inner layer processing
2	Cu pattern plated layer
1	VIP wrap plate = 2x 2
0	BV wrap plate
0	SMV plate process
2	**Lamination**
2	Mechanical drilling
2	Laser drilling
Index Total	14

Via Structure: Through hole and microvia L1-2, L12-11, stacked on an internal filled buried via L2-11 with copper over-plate

(Increased density PCB with **0.65mm** BGA or less – low pin count)

12 Layer PCB

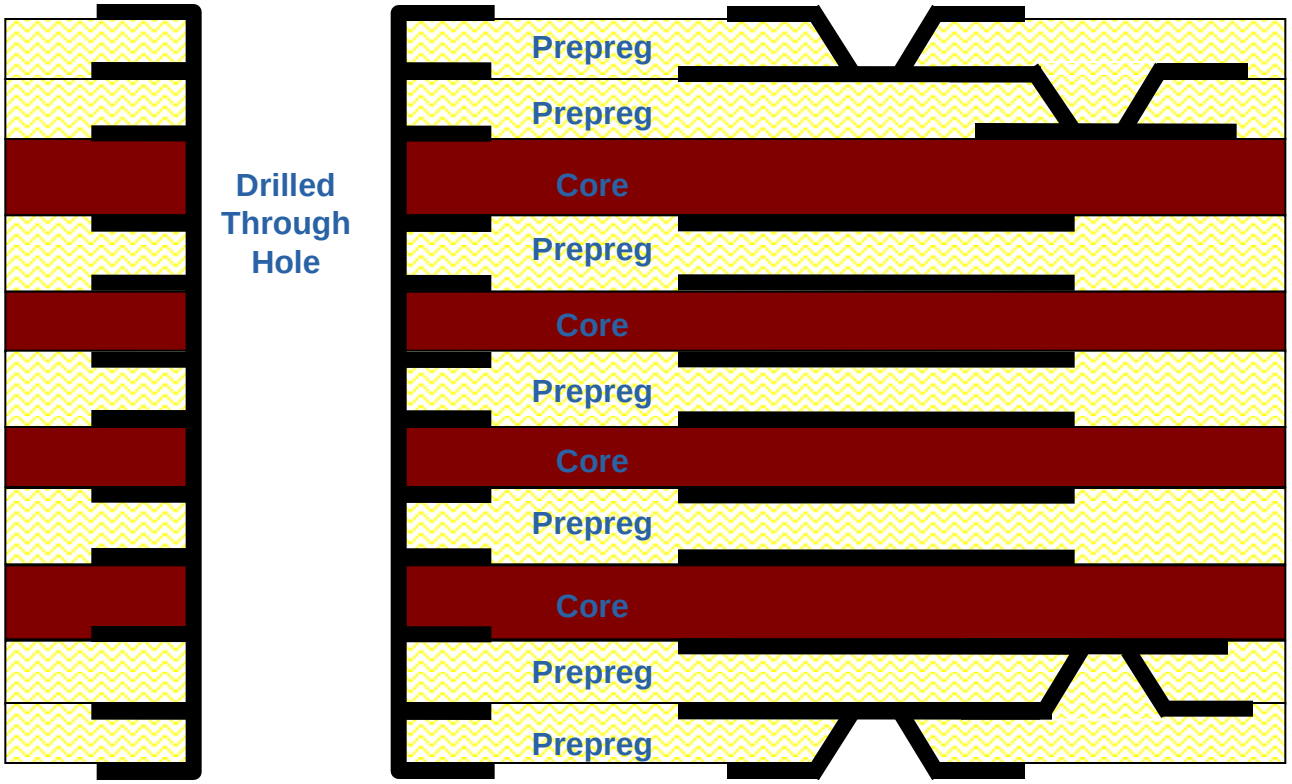


4	Inner layer processing
2	Cu pattern plated layer
1	VIP wrap plate = 2x 2
0	BV wrap plate
1	SMV plate process
2	**Lamination**
2	Mechanical drilling
2	Laser drilling
Index Total	15

Via Structure: Through hole and microvia L1-2, L12-11, stacked on an internal filled buried via L2-11 with copper over-plate plus copper filled microvias

(Increased density PCB with **0.5mm** BGA or less – low pin count & via in pad)

12 Layer PCB

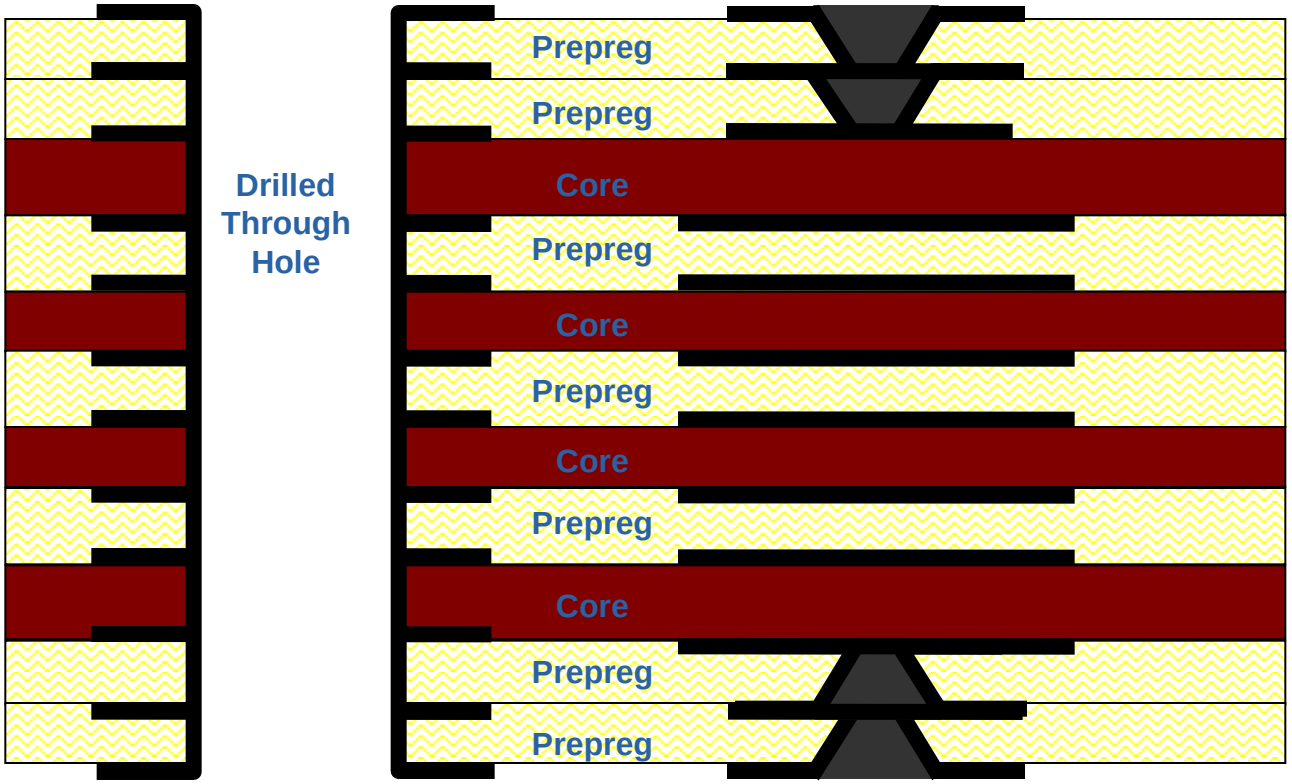


4	Inner layer processing
2	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
0	SMV plate process
2	**Lamination**
1	Mechanical drilling
4	Laser drilling
Index Total	13

Via Structure: Through hole and microvia L1-2, L2-3, L12-11, L11-10 (staggered)

(PCB with **0.5mm** BGA or less, medium pin count)

12 Layer PCB

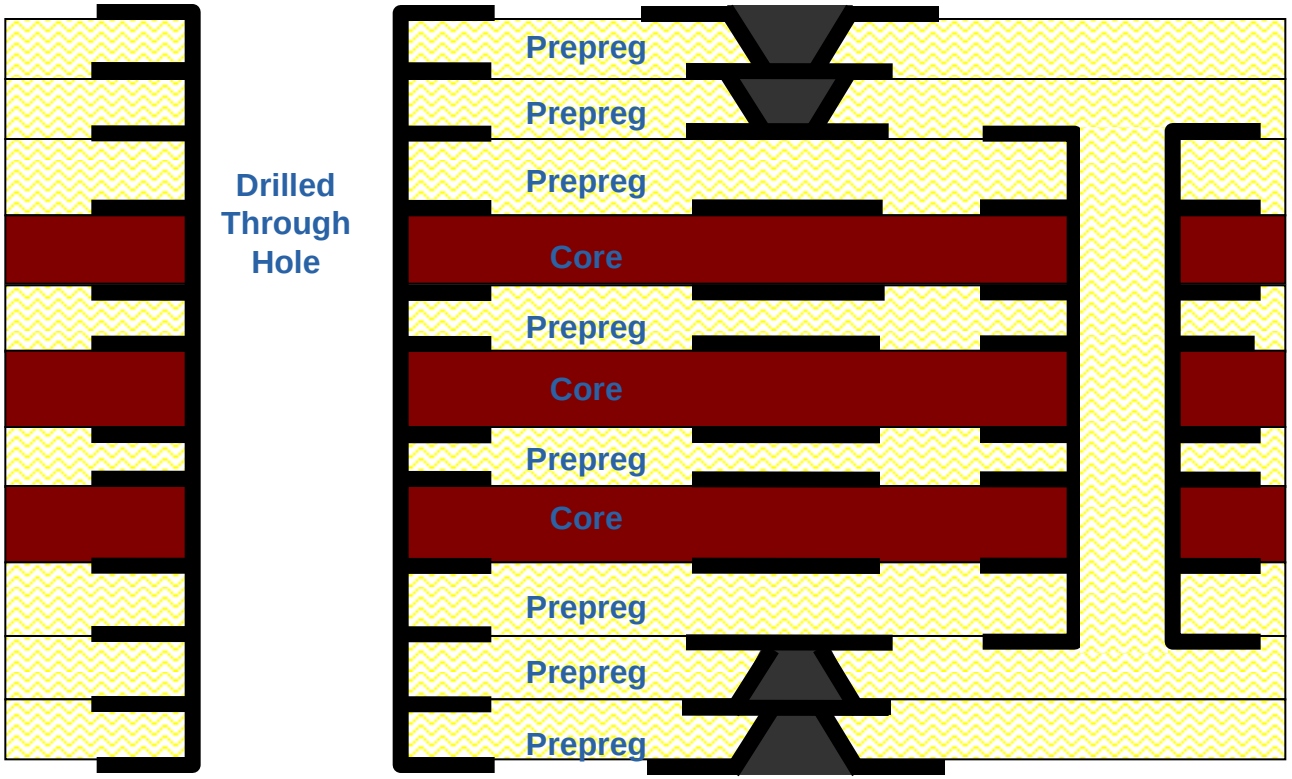


4	Inner layer processing
2	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
2	SMV plate process
2	**Lamination**
1	Mechanical drilling
4	Laser drilling
Index Total	15

Via Structure: Thru hole and microvia-in-pad L1-2, L2-3, L12-11, L11-10 (SMV stacked structure)

(PCB with **0.4mm** BGA, medium pin count, via in pad)

12 Layer PCB

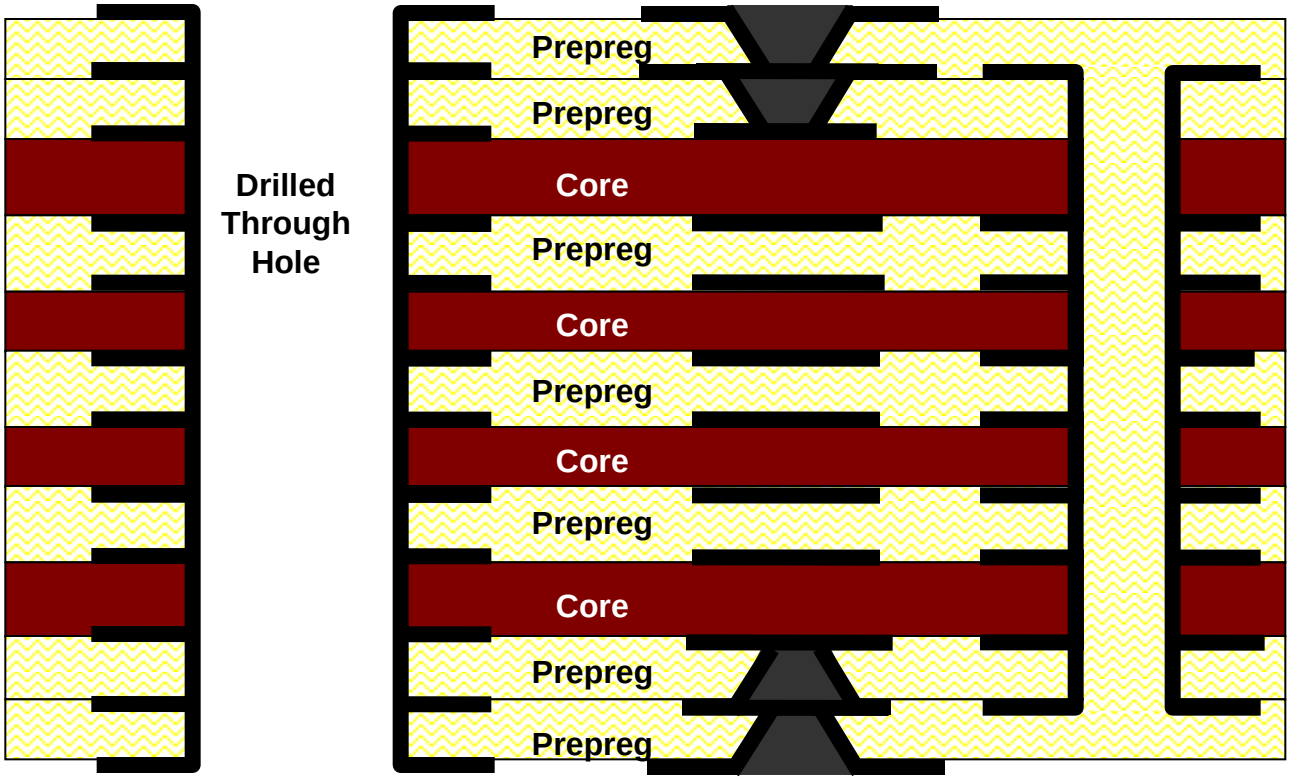


3	Inner layer processing
3	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
2	SMV plate process
3	**Lamination**
2	Mechanical drilling
4	Laser drilling
Index Total	17

Via Structure: Through hole and SMV L1-2, L2-3, L12-11, L11-10, with L3-10 buried via

(PCB with **0.4mm** BGA, high pin count, via in pad – costly)

12 Layer PCB

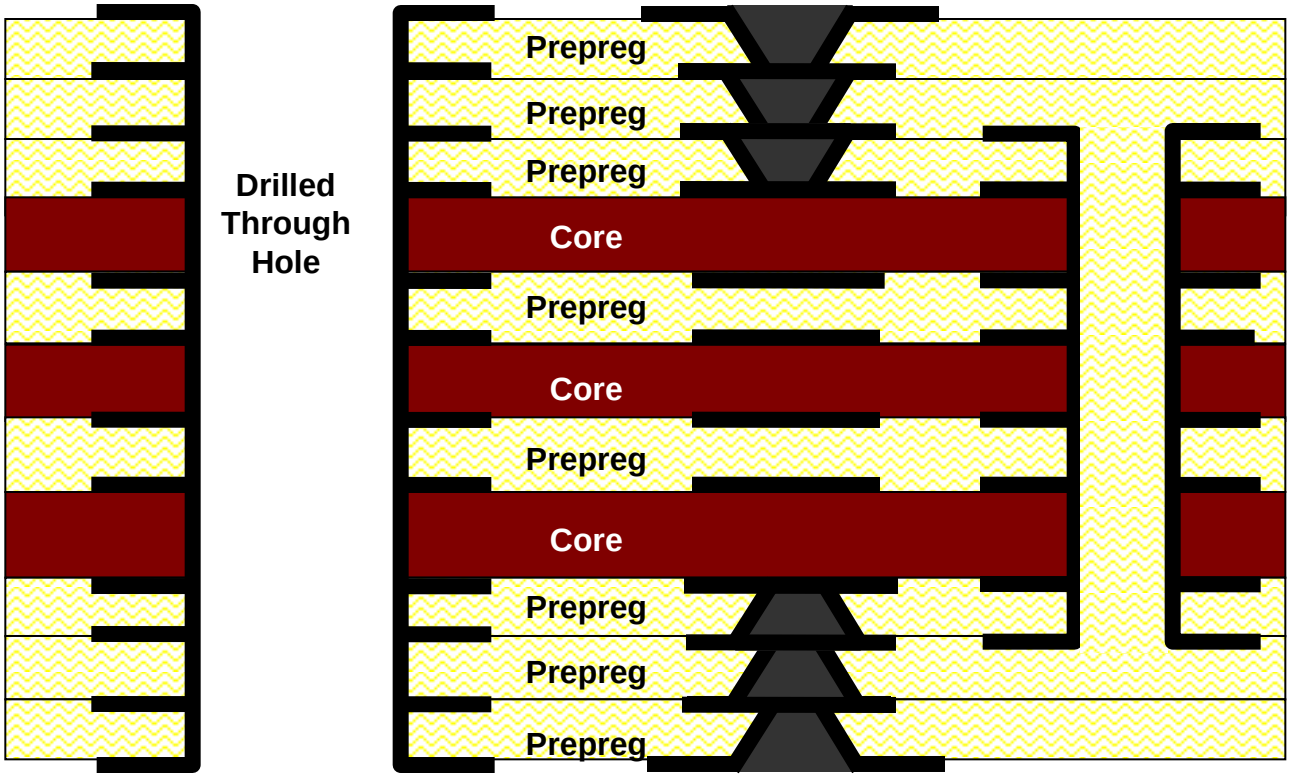


4	Inner layer processing
2	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
2	SMV plate process
2	**Lamination**
2	Mechanical drilling
4	Laser drilling
Index Total	16

Via Structure: Through hole and SMV L1-2, L2-3, L12-11, L11-10, with L2-11 buried via

(PCB with 0.4mm BGA, high pin count, via in pad – preferred)

12 Layer PCB

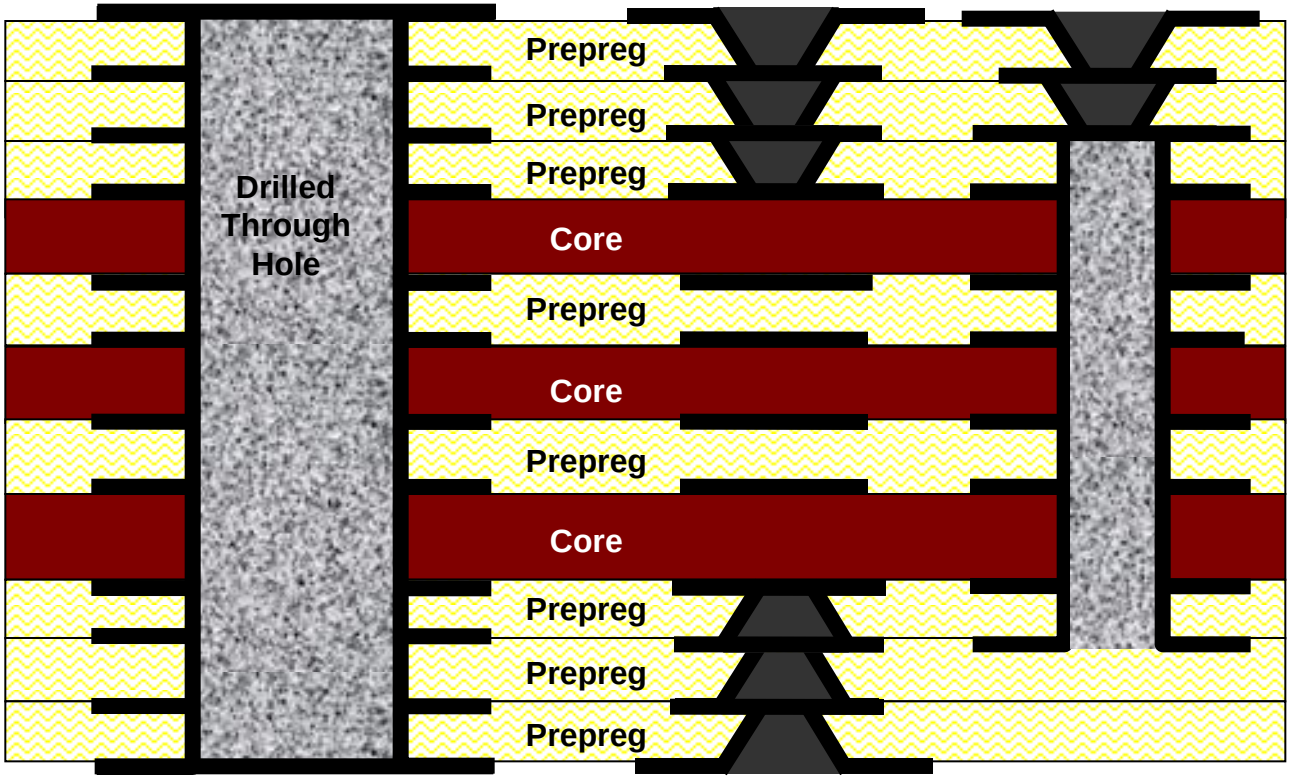


3	Inner layer processing
3	Cu pattern plated layer
0	VIP wrap plate = 2x 0
0	BV wrap plate
3	SMV plate process
3	**Lamination**
2	Mechanical drilling
6	Laser drilling
Index Total	20

Via Structure: Thru hole & SMV L1-2, L2-3, L3-4, L12-11, L11-10, L10-9, & bur via L3-10

(PCB with 0.4mm BGA or less, very high pin count, via in pad – preferred)

12 Layer PCB



3	Inner layer processing
3	Cu pattern plated layer
2	VIP wrap plate = 2x 4
0	BV wrap plate
3	SMV plate process
3	**Lamination**
2	Mechanical drilling
6	Laser drilling
Index Total	24

Via Structure: Through hole and SMV L1-2, L2-3, L3-4, L12-11, L11-10, L10-9, all via-in-pad plus a buried via L3-10 with fill and copper over-plate

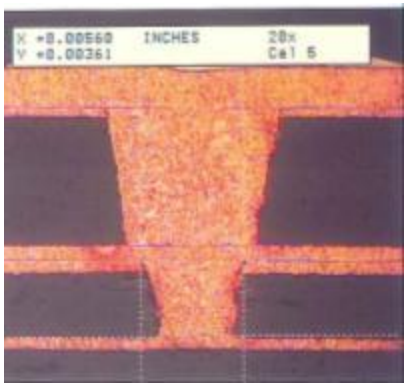
(Extreme!)

Microvia Sub-lamination Interface Techniques

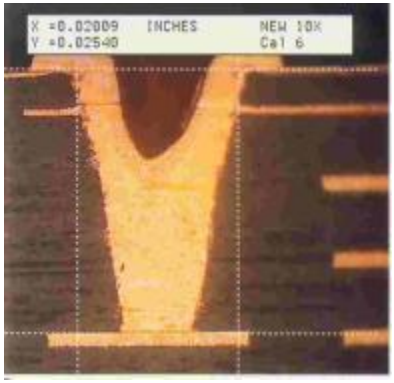
TTM Enabling Solutions

SMV®

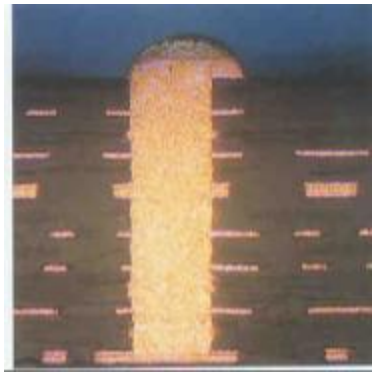
DpMV™



DpSMV®



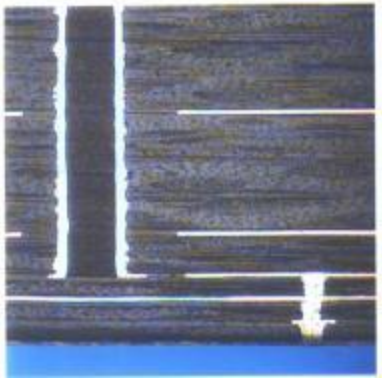
DpBV™



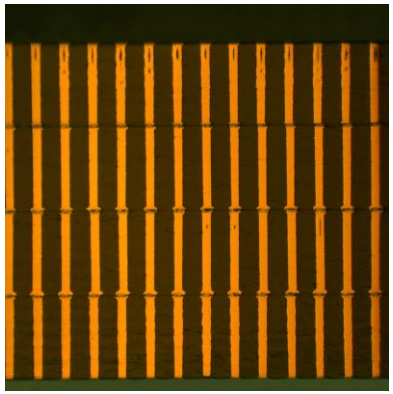
*ThermalVia™

FLAT-WRAP™

NextGen-SMV®



*HDI-Link™



*Sub-Link™

TTM Technologies

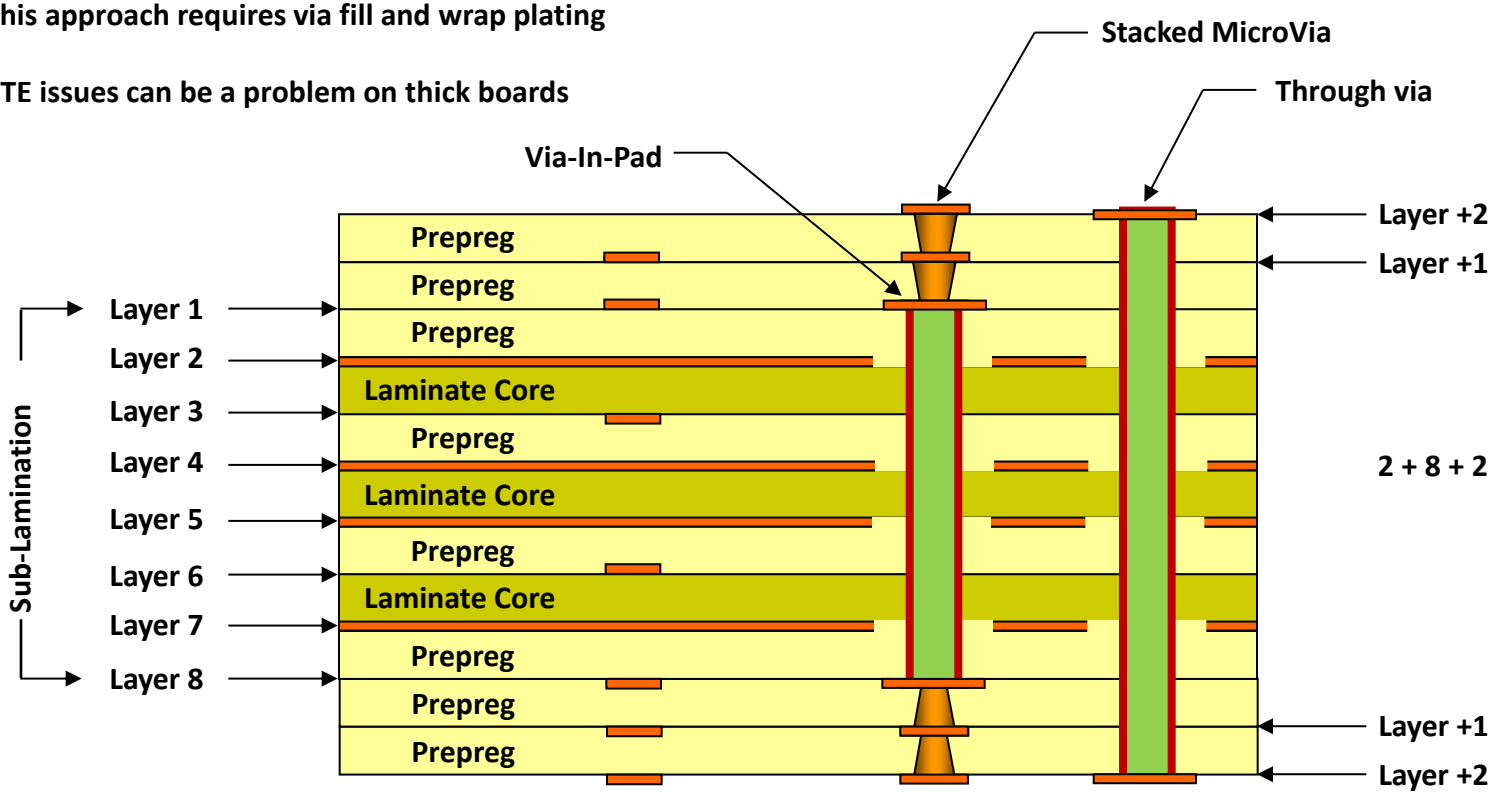
Microvia: Sub-Lamination Interface

Basic design rules for microvia build-up layers:

- Build-up dielectric layers must be balanced on either side of the sub-lamination
- Build-up dielectric layers are generally 0.0025” to 0.003” thick
- The recommended total number of lamination cycles that any one part of the structure should experience is 3 and 4 for advanced structures
- Microvias stacked on buried mechanical vias should be avoided due to wrap plating requirements and excessive stress on thicker substrates
- Solid copper mechanically drilled vias can be used on thin sub-lamination cores in place of wrap plating

Microvia Sub-Lamination Interface: Stacked On Sub-Via

- This approach requires via fill and wrap plating
- CTE issues can be a problem on thick boards

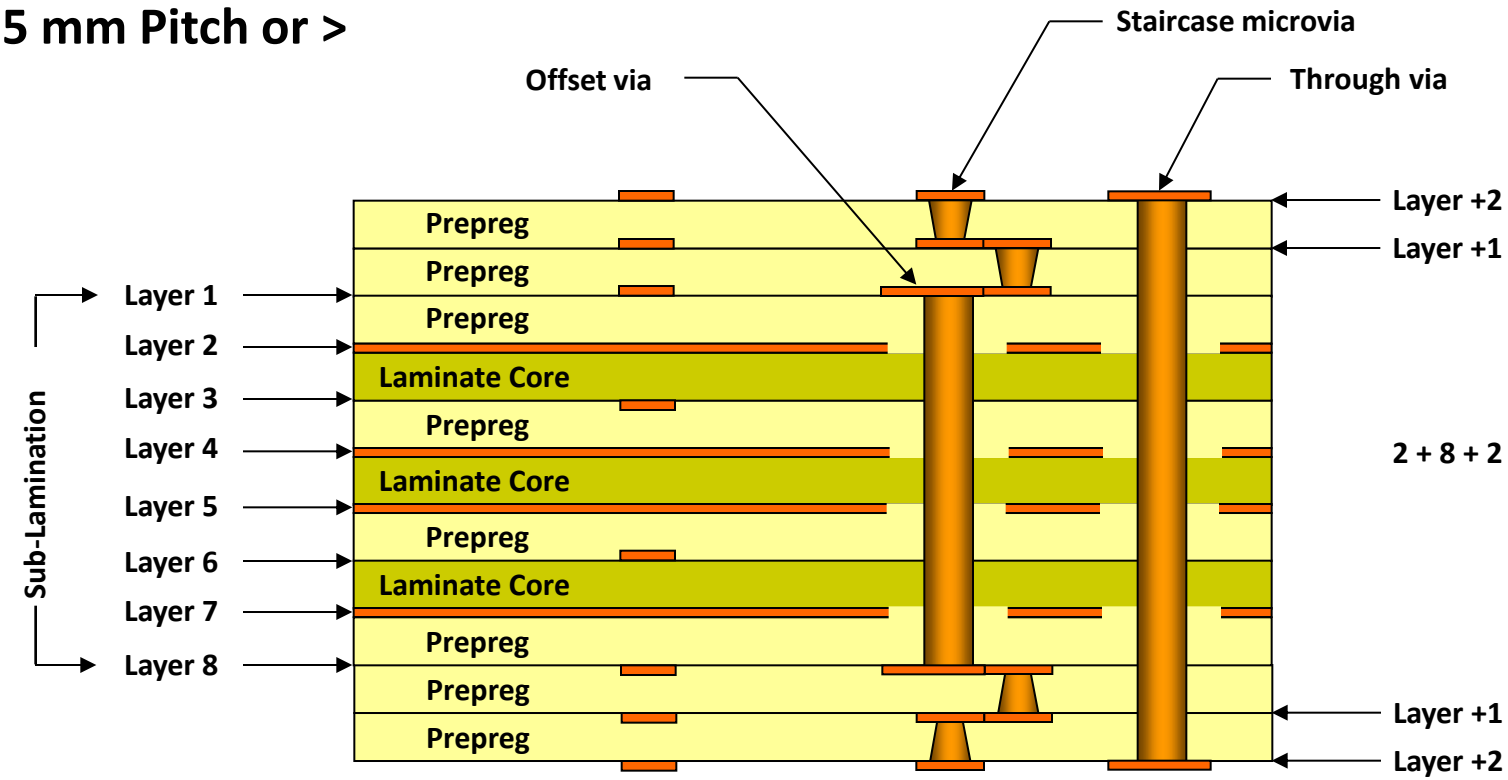


Not Recommended on all designs: Contact engineering

TTM Technologies

Microvia Sub-Lamination Interface: Offset Via

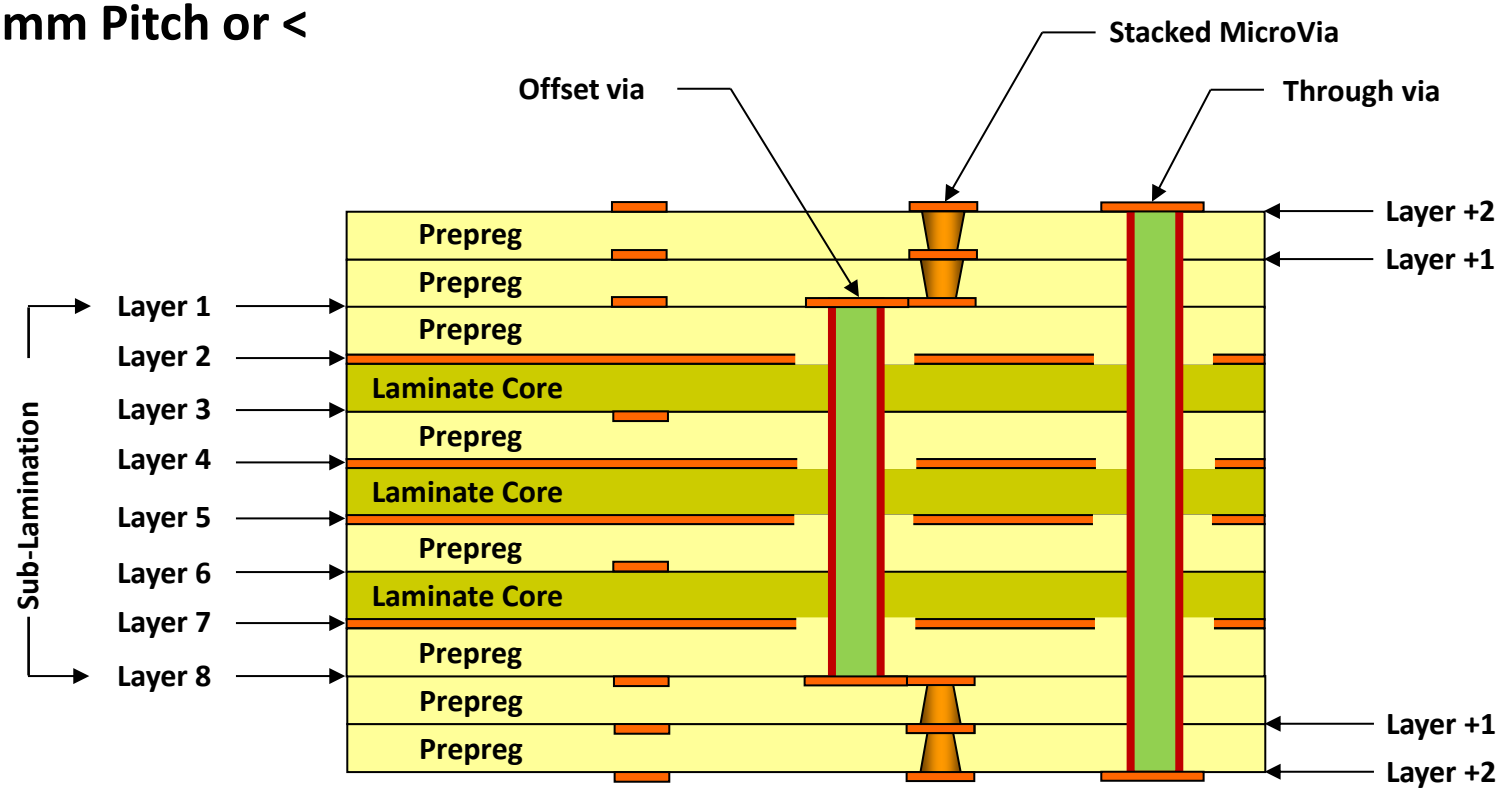
0.5 mm Pitch or >



Preferred Construction

Microvia Sub-Lamination Interface: Offset Via Stacked

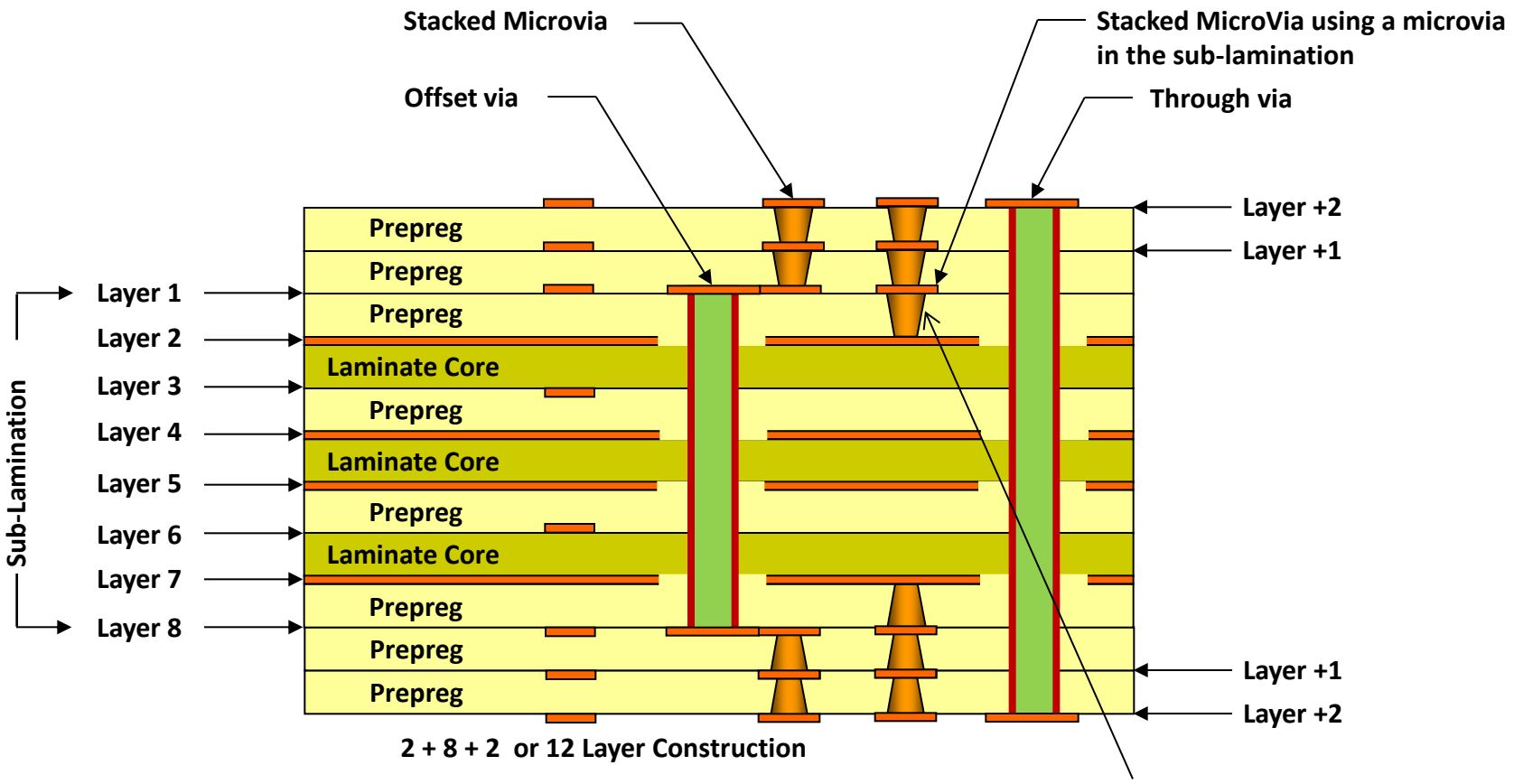
0.4 mm Pitch or <



Preferred Construction

TTM Technologies

Microvia Sub-Lamination Interface: Sub-Lam Microvia



Preferred Construction with additional low cost Microvia to layer 4

Exotic Process Operations

- Buried resistor technology (2 imaging & etching operations)
  - Process Cost index 2 per core
- Buried capacitance
  - 2 mil ZBC 2000 (Thin core processing & registration issues)
    - Process index 1 per core
  - Dupont HK-4, Farad Flex (Thin core processing & registration issues)
    - Process index 2 per core
  - 3M Cply (Thin core processing, sequential lamination & two imaging operations are required when both sides of the dielectric are unsupported by copper in the design)
    - Process index 3 per core
- Cavity constructions i.e. recessed regions of the PCB. This process requires many additional tooling and process operations
- Buried resistor layers, this requires rather expensive material and special etching chemistry

Keys to Success

Rules of Thumb for Cost

- Investigate how PCBs will **fit** into a production panel to ensure that maximum material utilization occurs
- Use a ***smaller line width/space*** **before** adding layers
- Use ***smaller holes*** **before** adding layers
- When using tighter impedance tolerances, ensure that the build doesn't cancel out these gains (glass styles, line widths)
- Add ***laser blind vias*** (one or two sides) **before** buried vias
- ***Laser and buried vias*** allow for **better yields** than mechanical blind vias
- Add ***staggered laser vias*** **before** stacked vias
- Consider **hybrid** builds for a performance/cost benefit

Always work with your fabricator on cost mitigation strategies

Summary and Conclusion

- **Cost is driven by Engineering and Design!**
- For optimum results, PCB cost control really needs to be addressed in the **early phases** of product development
- **Panel Utilization** is critical to producing PCB's at the lowest cost
- Keep it **simple**! Complex PCB designs can add many costly manufacturing operations as well as longer lead times
- Manufacturing **yield** should be considered in the design process and **concurrent engineering** with vendors can improve yields
- IPC Class 3, 3A, and IST **requirements** can have a large impact on PCB cost due to large numbers of coupons, documentation, lab time, as well as, panel utilization

Thinking Outside the Board
TTM DFM Intro

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Global Presence | Local Knowledge

June 15, 2016

Objectives:

- Introduce DFX for Printed Circuit Board Design
  - Design for Fabrication
  - Design for Assembly
  - Design for Test
  - Design for Quality
- Initial considerations for best cost with highest reliability
- Pre-planning
  - Reduce prototype spins by planning ahead
  - Reduce prototype to mass production modification delays and TQs
  - Keep Purchasing Department happy

What Your Company Can't Afford

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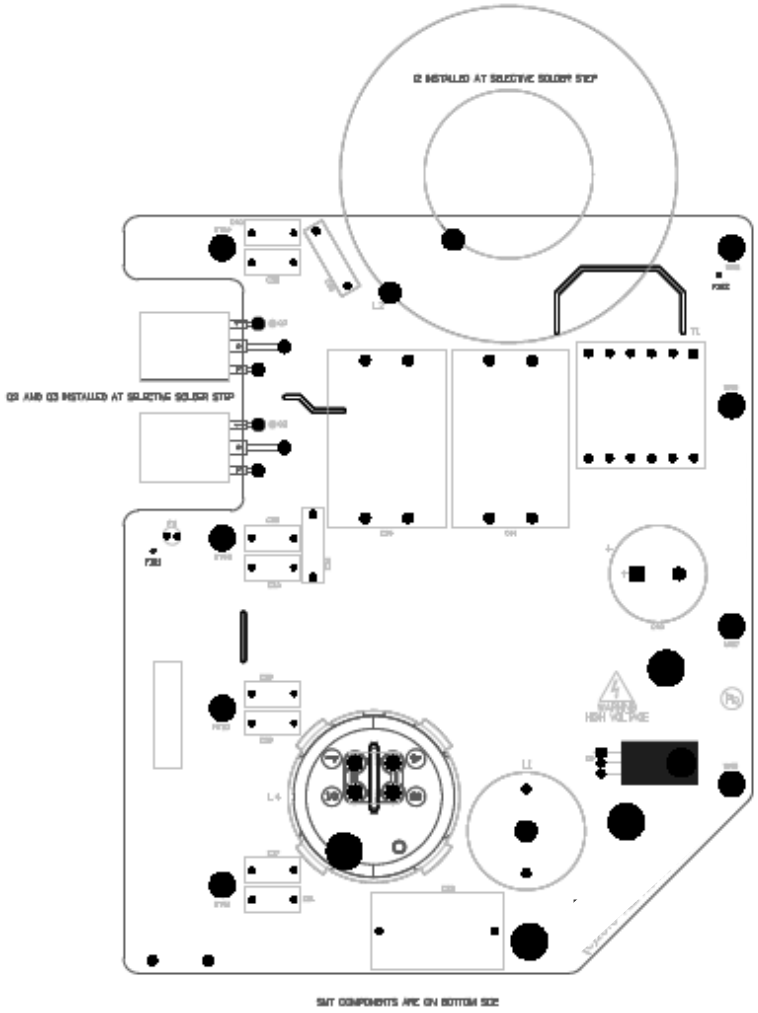
Many PCB-related Design Inputs are Outside the Board

- Circuit Board Attributes, Layer count, Thickness, Dimensions, Holes, Lines/spaces, Blind/buried Vias
- Component pad size/pitch/density drive design complexity and technology
  - Smallest feature sets price of whole PCB
  - Design the rest of the features as large as possible
- Via in pad solder mask or fill protection required during soldering
  - Cu-cap plated filled vias are 30% more expensive
- PCB Technical difficulty – which fab site fits?
- Fabricator Design Guidelines for Site / technology
- Fab Panel Utilization
- Assembly Panel (Arrays) Utilization
- Assembly Requirements
  - Rails for conveyance
  - Stability of array
  - Over-Size limited by SMTA platforms, such as solder paste printers
- Material
- Stack-up
- DFX (Design for Fabrication, Assembly, & Test); Follow the KISS principle
- Migration path prototype (local) to mass production (Asia)

Design Team:

- Electrical & Mechanical Design Engineers
- Test Engineers
- Quality Engineers
- Supply Chain Management & Supply Chain
- Contract Manufacturers or Company Manufacturing

Assembly Requires Design Teamwork



How will this go down the line?

How many up on an array for SMT?

- Rails?
- Panel utilization killer?

What do we do about the overhanging parts during assembly?

Can a vision system read a broken edge?

Shock to the overhanging part solder joints during operation?

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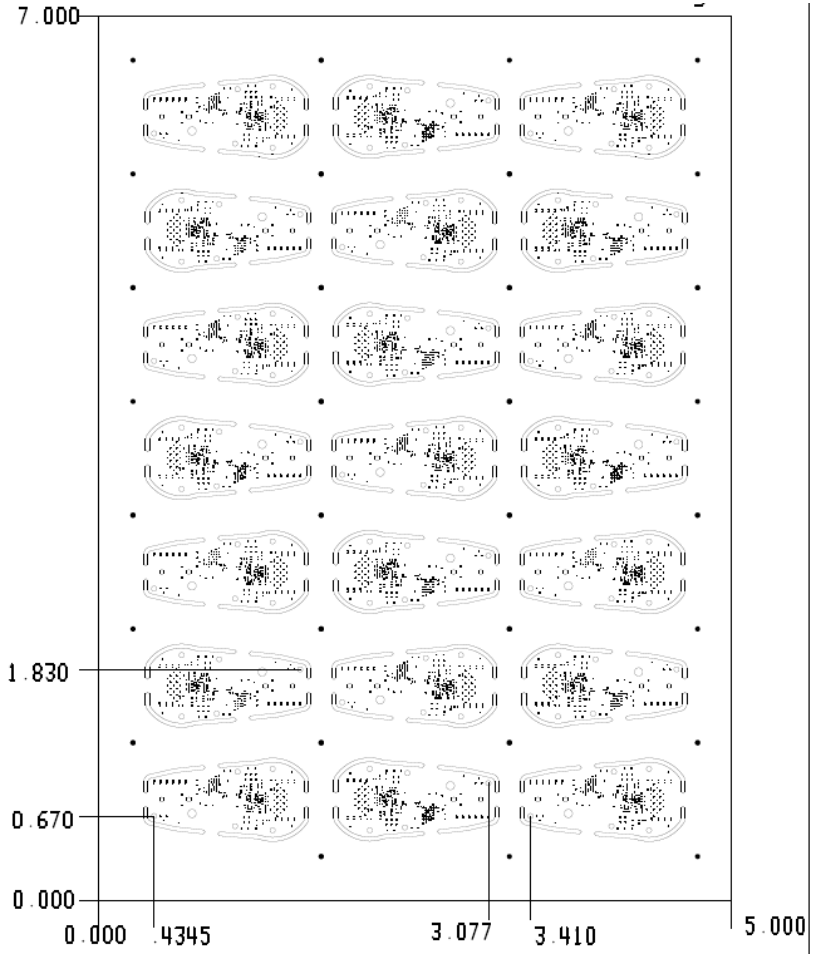
Dimensions: Fab Panel Utilization Biggest Cost Factor

- The cost of a production panel is stable, with additional units adding slightly additional cost – get as many up on a production panel as possible
- Plan the PCB size to include rails for over-hanging components and/or clearance for assembly
- Utilize TTM standard panel sizes (inch):
  - 18x24 20x24 21x24 16x20 16x18 16x21 16x24

5” X 7” Panelization Example

Use an 18” x 24” or 21” x 24” production panel? (consider working panel tooling)

Reduce space between parts by 0.10” and add 3 more units – a 14% unit increase/panel



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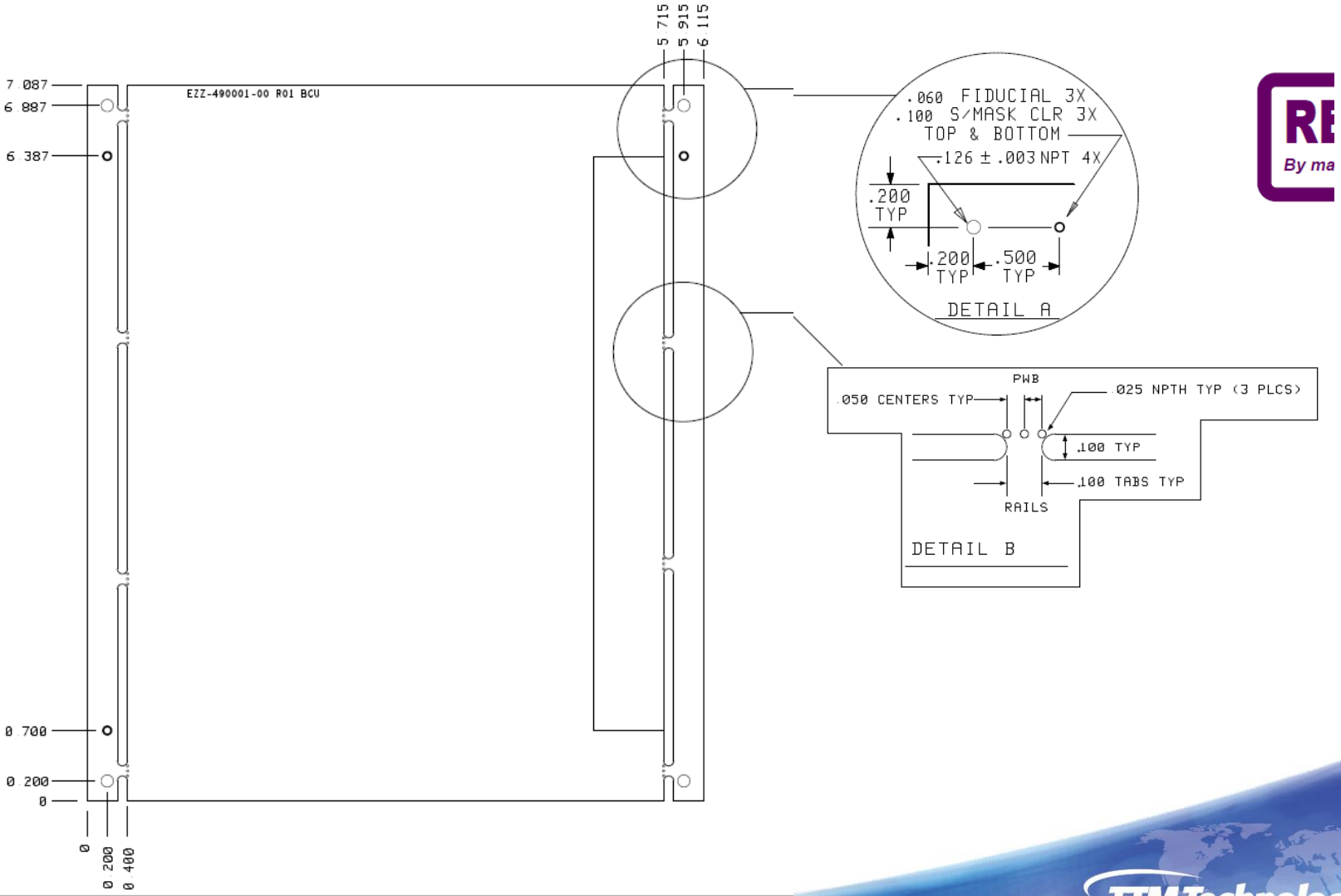
Panelization Example yields 6 PCBs on 18”x24”

A 2 x 1 array, approx. 11” x 8” would fit 8 per production panel by reducing to approx. 5.2” side



Standard TTM Automotive Materials

- Isola 370HR is TTM standard for High Tg FR-4
- Isola 370HRS is CAF-improved, TTM-required for High Voltage applications
- Immediate Cost Reduction Options
  - Use EM-827 for:
    - 0.5 oz, 1 oz. Cu designs
    - Where no High Voltage is required
      - Already used on 1033983-00-B ADAS, NCAP, Camera Control Module
- Additional Materials Under Consideration
  - Isola 180 with Baotek glass for High V
  - ShengYi Autolad for stacked microvia designs (lower CTE)

Stack-ups for China Should Be Confirmed Before Routing

- Select materials most used by the production site – not reference design stack-ups
  - Higher volume pricing
  - Better availability
  - Site more familiar with material characteristics
- Glass weaves are different
  - Engineers don’t like approving different stack-ups
  - Controlled impedance adjustments
- Lamination equipment presses differently
- Up-front approval reduces production approval
- Potential cost savings with efficient stacks

Utilize Asia DFM Guidelines for Mass Production

TTM-Via Asia DFM Checklist
Last Update: 30-April 2015
Version 1.1

Characteristic		DFM Standard (minimums)	Guangzhou Minimum	Huiyang Minimum	Zhongshan Minimum
Inner Layer Etch Capabilities	1/2 oz. trace/space	4 mil/4 mil	3 mil/3.5 mil	3 mil/3.5mil	4 mil/4mil
	1 oz. trace/space	4 mil/4 mil	3 mil/3.6 mil	3.5 mil/4 mil	4 mil/4mil
	2 oz. trace/space	7 mil/7 mil	6 mil / 6 mil	5 mil/6mil	6 mil / 6 mil
	3 oz. trace/space	9 mil/9 mil	8 mil / 8 mil	7.5 mil/7.5 mil	8 mil/8 mil
	4 oz. trace/space	9 mil / 9 mil	9 mil/11 mil	no	10 mil/10 mil
	5 oz. trace/space	11 mil / 11 mil	11.5 mil/13.4 mil	no	12 mil/12 mil
	6 oz. trace/space	13 mil / 13 mil	14 mil/15.6 mil	no	13 mil/13 mil
	12 oz. trace/space	28 mil / 28 mil	no	no	26 mil / 26 mil
Outer Layer Etch Capabilities	Outer Layer Thickness after Plating				
	1.3 - 1.5 mil	3.5 mil/4 mil	3 mil / 3.5 mil	3.5 mil/4 mil	4 mil/4 mil
	1.8 - 2.0 mil	4 mil/4 mil	4 mil/4 mil	4 mil/5 mil	5 mil/4 mil
	2.5 mil	5 mil/5 mil GZ	4 mil / 4 mil	5 mil/5.5 mil	6 mil/6 mil
	3.0 - 3.2 mil	7 mil/7 mil GZ	6 mil/6.5 mil	6 mil/6 mil	8 mil/8 mil
	3.8 - 4.4 mil	9 mil/9 mil	9 mil / 9 mil	no	8 mil/8 mil
	5.4 - 5.8 mil	11 mil/11 mil	11 mil/11 mil	no	9 mil/9 mil
Drilled Via Size	Drill/Pad Diameter **[for Tangency]**	10 mil/20 mil	10 mil/19 mil </= 0.062"	10 mil/19 mil </= 0.062"	10 mil/22 mil </= 0.062"
			10 mil/19 mil </= 0.120"	10 mil/19 mil </= 0.120"	12 mil/24 mil </= 0.093"
	(Class 3: IL + .002 / OL + .004)		12 mil/22 mil </= 0.160"	12 mil/22 mil </= 0.160"	14 mil/26 mil </= 0.125"
			14 mil/24 mil </= 0.190"	14 mil/24 mil </= 0.190"	
Aspect Ratio	Drill Diameter				
	8 mil	8:1	8:1	8:1	no
	10 mil	10:1	12:1	12:1	8:1
	12 mil	10:1	14:1	13:1	8:1
	13.5 mil	10:1	14:1	13:1	8:1
Mechanical Hole Edge to Copper	Hole Edge to Conductor	8.5 mil	8 mil	8 mil	8.5 mil
Mechanical Hole Edge to Copper	Hole Edge to Cu on Anti Pad	10. mil	10. mil	10 mil	10. mil
Microvia Edge to Adjacent Copper		9 mil	8 mil	6 mil	no
Conductor [Cu] to board edge		15 mil	10 mil	10 mil	10 mil
Microvia	Microvia Diameter	5 mil	4 mil	4 mil	no
	Pad Diameter	drill + 8 mil	drill + 8 mil	drill + 9 mil	no
	Aspect Ratio	0.5:1	0.8:1	0.85:1	no
SMD to SMD Spacing	½ oz	8 mil	7 mil	8 mil	8 mil
	1 oz	8.5 mil	9.5 mil	9.5 mil	9.5 mil
	2 oz	9 mil	11.5 mil	11.5 mil	11.5 mil
	3 oz	10 mil	12.5 mil	12.5 mil	12.5 mil
Solder Mask	Minimum dam width	4 mil	2 mil	2.5 mil	3 mil
	Minimum s/m-defined pad	12 mil	12 mil	10 mil	10 mil
Non-Conductive Via Fill / Cap Plate	Min - Max Drilled Hole	10 - 18 mil	10 - 18 mil	8 - 20 mil	no
	Aspect Ratio	10:1	12:1	12:1	no
Flatwrap		no	no	no	no
Copper Fill		no	no	no	no
LDI Mask		no	no	no	no
Ink Jet Nomen		no	no	no	no
Plated Hole Spacing	DHW to DHW [CAF]	30 mil	25 mil	25 mil	25 mil
Plated Hole Spacing	DHW to DHW [Eye brow cracks]	12 mil	11 mil	11 mil	11 mil
Dimensional Tolerances	Score off set	+ / - 5	5 mil (jump) / 4 mil (normal)	+/ - 2 mil	+ / - 5 mil
	True position	+ / - 5 mil	+ / - 4 mil	+ / - 5 mil	+/- 5 mil
	Routed Profile & Cut out	+ / - 5 mil	+ / - 4 mil	+ / - 4 mil	+ / - 4 mil
	Largest non plated drill diameter		257 mil	250 mil	257 mil
	Edge connector Bevel Depth	+ / - 5	+ / - 5 mil	+ / - 8 mil	no
Cu Disribution: Thieving	Common Voided areas IL & OL		1 sq inch or > area	1 sq inch or > area	1 sq inch or > area
Operator	Name	Date			
CAM					

Pre-Design Communication Reduces Technical Queries!

Procedures for Prototype Transfers to China

- Global Supply Chain to cc TTM Engineering on RFQs:
  - Quick-turn N. America PCB Prototypes
  - Procurement by a CM: state if panelization is required for fast QTA
  - Review site-proposed stacks for mass production
  - Review proto arrays for mass production – change if needed when going to Asia
- Asia production orders TBD, but plan accordingly

Conclusion: Working Together Initially Saves $$$$

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Thank you!

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