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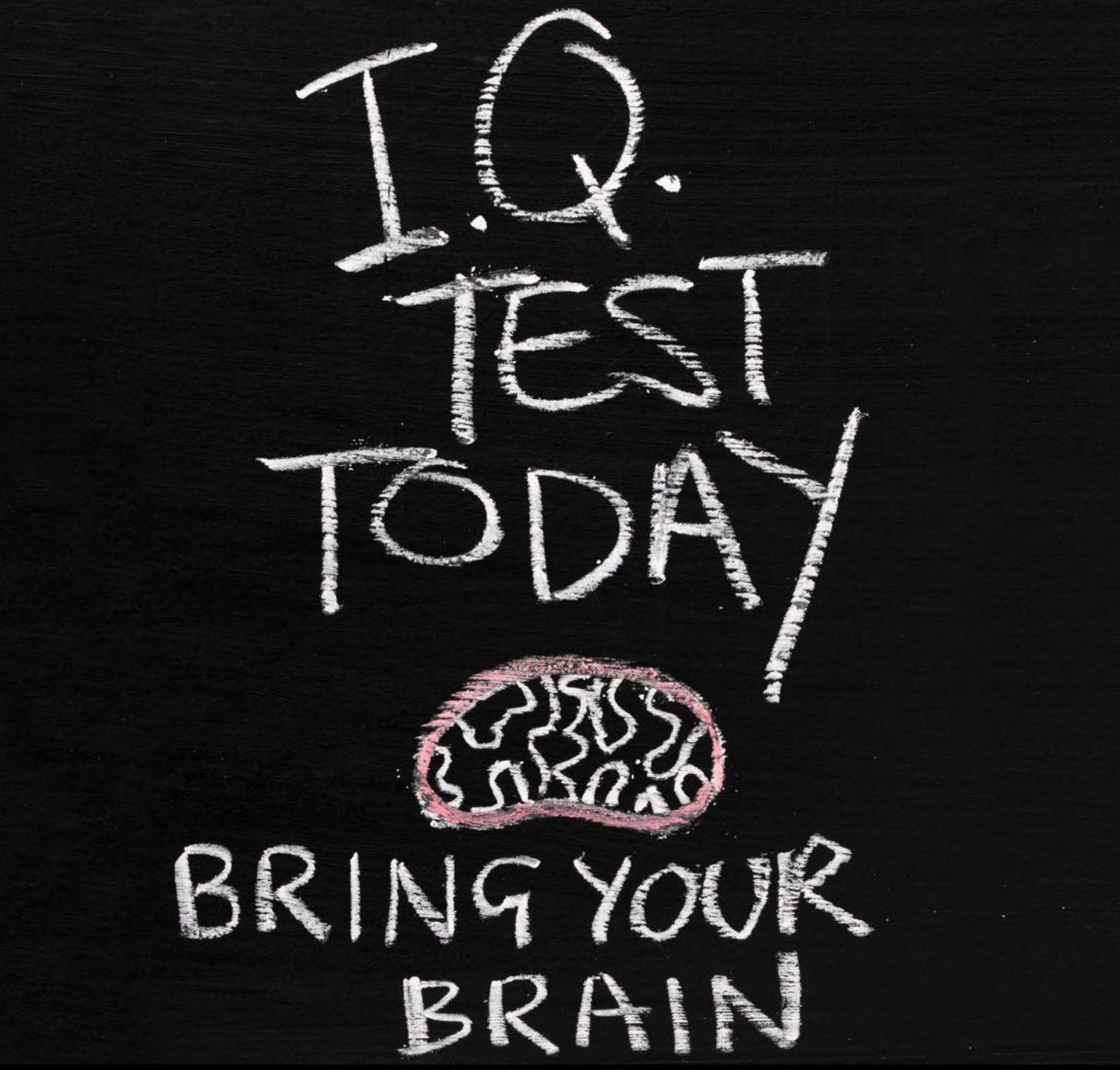

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THE pcb design MAGAZINE
December 2015

THIS MONTH'S FEATURE ARTICLES

The Designers Council Issue

It's been almost 25 years since the first Designers Council meeting in Atlanta. Now, the council has chapters around the world, with thousands of members. This month, we bring you interviews with some of the people who helped make the Designers Council what it is today: Gary Ferrari, Anne Marie Mulvihill, Rick Hartley, Mike Creeden, and Scott McCurdy. Happy holidays!

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CTE Z-axis (50 to 260°C)	2.90%	2.90%	2.80%	2.90%
T-260 & T-288	>60	>60	>60	>60
Halogen free	Yes	No	No	No
VLP-2 (2 micron Rz copper)	Standard	Standard	Available	Available
Stable Dk and Df over the temperature range	-55°C to +125°C	-40°C to +140°C	-55°C to +125°C	-55°C to +125°C
Optimized Global constructions for Pb-Free Assembly	Yes	Yes	Yes	Yes
Compatible with other Isola products for hybrid designs	Yes	Yes	Yes	For use in double-sided applications
Low PIM < -155 dBc	Yes	Yes	Yes	Yes

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The Designers Council: Elevating PCB Design, and Designers

by Andy Shaughnessy
I-CONNECT007

It was a different time.

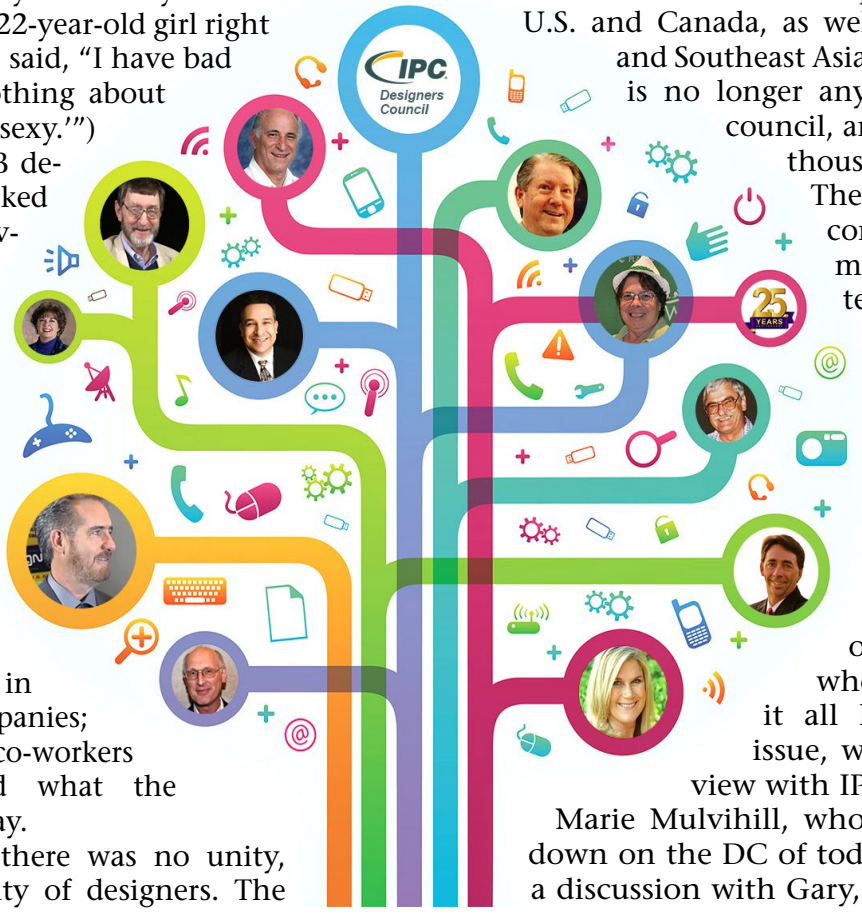
When the seeds of the Designers Council were first sown in 1991, PCB designers were still considered red-headed stepchildren, earning less respect than Rodney Dangerfield. The PCB was seen as just an interconnect platform, soulless and boring. And PCB designers were dinosaurs toiling away on a "mature" technology that would soon be replaced by multichip modules, or some other cool technology.

Back then, the integrated circuit was king; IC design was considered "sexy" and IC designers were the rock stars of electronics design. (Years ago, I told that story to a newly hired assistant editor, a cute 22-year-old girl right out of college. She said, "I have bad news for you: Nothing about this industry is 'sexy.'") But the lowly PCB designer was looked down upon by everyone.

It didn't help that PCB designers were spread out across so many various segments of the electronics industry. It's a vertical occupation in a horizontal industry. Designers often felt like outsiders in their own companies; none of their co-workers really understood what the designers did all day.

Worst of all, there was no unity, no real community of designers. The Internet as we know it was still a few years away. PCB West had just launched; it was the only organized PCB design event, and the only chance for designers to do any networking. What was a designer to do?

Then, as the "Founder of the Designers Council" Gary Ferrari recounts in this month's issue, Dieter Bergman asked him what IPC could do for PCB design. They traveled around the United States, talking to designers and getting a feel for their interest in forming a design organization. Yes, there was plenty of interest. And by 1992, the first DC chapter had formed in Atlanta, followed by dozens more in rapid succession.



Now there are DC chapters around the U.S. and Canada, as well as Australasian and Southeast Asian chapters. There is no longer any fee to join the council, and the DC counts thousands of members. The local chapters are completely autonomous; some chapter meetings draw huge crowds, and a few chapters are nearly dormant.

As the Designers Council enters its 25th year, we decided to talk to some of the people who helped make it all happen. In this issue, we have an interview with IPC's tireless Anne Marie Mulvihill, who gives us a rundown on the DC of today. We also have a discussion with Gary, who takes us all

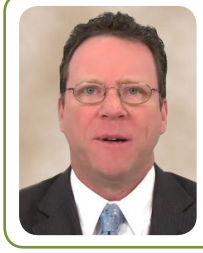
the way back to the beginning and shares a little "inside baseball" on the forming of the council.

Design instructor Rick Hartley discusses how he helped start a DC chapter in Ohio, and he lays out the many educational and networking benefits of being involved with your local chapter. San Diego PCB's Mike Creeden talks about his work with the DC, and he explains how the executive board functions as well.

And Zentech's Judy Warner interviewed Freedom CAD's Scott McCurdy, president of the Orange County Designers Council Chapter. The Orange County chapter meetings routinely draw nearly 100 attendees, and Scott was happy to share his "playbook" for starting and sustaining an active DC chapter. I think Scott spends part of each week planning the next DC chapter meeting, but the results speak for themselves.

It's been quite a year. In 2015, we covered a lot of big news. We also said goodbye to some good people, like Gary Smith and Steve Weir. In this issue, don't forget to check out the most popular PCB design articles and news items of 2015.

I hope you have a great holiday. I'll see you in 2016! **PCBDESIGN**



Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 16 years. He can be reached by clicking here.

Quantum Physics Problem Proved Unsolvable

A mathematical problem underlying fundamental questions in particle physics and quantum physics is provably unsolvable, according to scientists at UCL, Universidad Complutense de Madrid—ICMAT and Technische Universität München. The findings show that even a perfect and complete description of the microscopic properties of a material is not enough to predict its macroscopic behaviour.

The study, published today in Nature, investigated the problem of the 'spectral gap' – the energy needed for a material to transfer from its lowest-energy state to an excited state. When this energy becomes very small (i.e. the 'spectral gap closes'), it becomes possible for the material to transition to a completely different state and the properties of the material can undergo dramatic changes. For example, when a material at a very low temperature transitions from insulating to superconducting, this dramatic change is the result of its spectral gap closing.

Co-author Dr. Toby Cubitt from UCL Computer Science, said, "Alan Turing is famous for his role in cracking the Enigma code, but amongst mathematicians and computer scientists, he is even more famous for proving that certain mathematical questions are `undecidable' – they are neither true nor false, but are beyond the reach of mathematics.

"What we've shown is that the spectral gap is one of these undecidable problems. This means a general method to determine whether matter described by quantum mechanics has a spectral gap, or not, cannot exist."

The researchers are now seeing whether their findings extend beyond the artificial mathematical models produced by their calculations to more realistic quantum materials that could be realised in the laboratory.

IPC DESIGNERS COUNCIL:
Serving PCB Designers for Almost 25 Years

by Andy Shaughnessy

You may have seen Anne Marie Mulvihill at the Design Forum during IPC APEX EXPO, rounding up the speakers and PCB designers and basically keeping everyone happy, often with a sarcastic comment or two. As the PCB design program manager for IPC, Anne Marie is in charge of making the train run on time for PCB designers, a task I would compare to herding cats. When I told Anne Marie that we were covering the Designers Council for this issue, she jumped at the chance to help us out.

Andy Shaughnessy: *What is the Designers Council's basic mission?*

Anne Marie Mulvihill: The Designers Council's mission is to provide technical education that connects the design community. This connection makes technology interchange more efficient.

Shaughnessy: *How does the executive board function?*

Anne Marie Mulvihill

Mulvihill: The Designers Council Executive Board is a blue-ribbon group, i.e., open by invitation only. These thought leaders in the design community have all been working at the advanced level for more than 20 years, and are drawn from every market sector. They volunteer their time and thoughts to serve as the Steering Committee for IPC Design Programs.

Members of the group meet twice every year in person with IPC staff, and consult informally throughout the year about the direction for IPC programs like Designer Certification, the Designers Council, development of industry standards focused on design, technical courses, and events associated with design.

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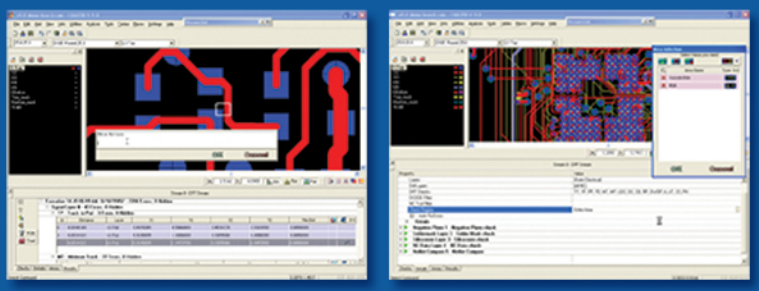

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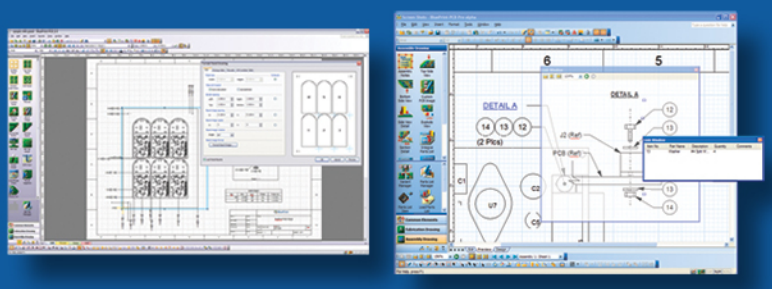

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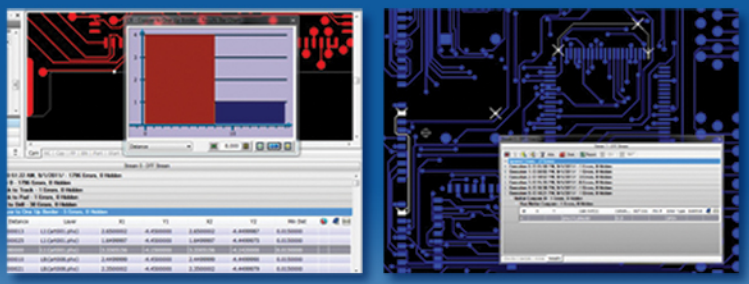

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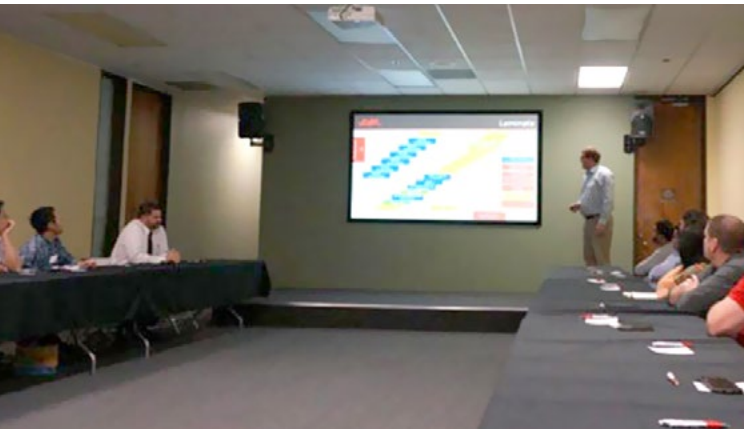
IPC DESIGNERS COUNCIL: SERVING PCB DESIGNERS FOR ALMOST 25 YEARS



***Shaughnessy:** What are your membership stats: industry segments, job descriptions, regions of the world, total membership, etc.?*

Mulvihill: The IPC Designers Council is an international society for all individuals with interest in design. Participants are drawn from all over the world, from every market segment. They hold a variety of job titles; those with "design" or "designer" in them are the majority.

***Shaughnessy:** Do you host any events?*

Mulvihill: Absolutely.

a. IPC presents the Design Forum every year, within the premier industry event IPC APEX EXPO. This activity features technical presentations from industry thought leaders, in a full-day conference format that allows for both education and networking. The Design Forum 2016 runs on Monday, March 14, 7:30 a.m. – 1:30 p.m. in Las Vegas, at the Convention Center with IPC APEX EXPO.

b. Half-day and full-day technical courses with an emphasis on design are also on the Professional Development slate at IPC APEX EXPO. Courses of particular interest to designers run on March 13–14, Sunday and Monday afternoon. More information about Professional Development courses and the Design Forum can be found at www.ipcapexexpo.org.

c. Designer Certification sessions consist of two days of instruction, plus one day of review with an exam. These sessions are delivered by IPC-licensed training centers, in classrooms all over the world. Successful completion of the courses results in the award of highly respected professional designations: CID (Certified Interconnect Designer) and CID+ (advanced level).

***Shaughnessy:** What are the top 2-3 benefits you bring your membership?*

Mulvihill: First would be our design community connections, such as the electronic bulletin board. Designers interested in subscribing should visit our site. We also provide IPC e-mail broadcasts. And the Designers Council chapter meetings allow members to connect with other designers and learn new processes and techniques though periodic "Lunch 'n' Learn" events.

Second would be the discounts DC members can apply to designated IPC industry standards, events, and programs with a focus on design.

***Shaughnessy:** How much does DC membership cost?*

Mulvihill: There are no fees associated with participation in the IPC Designers Council.

***Shaughnessy:** Tell us about the CID and CID+ certifications. I understand the curriculum has been "updated," if that's the right word.*

Mulvihill: That is the right word! Course content for both the CID module and the CID+ module have been updated, to help meet design challenges of today's environment. The 2016 editions of CID and CID+ modules are available.

- New content has been added to the course textbook (the Study Guide), slides used for classroom presentation, and the exam. For example: the latest lead-free and other environmental regulatory issues associated with materials.
- Information has been re-organized, for improved flow.
- Exam format has been aligned with today's best practices in testing.

***Shaughnessy:** Is there still a plan to add HDI CID certification?*

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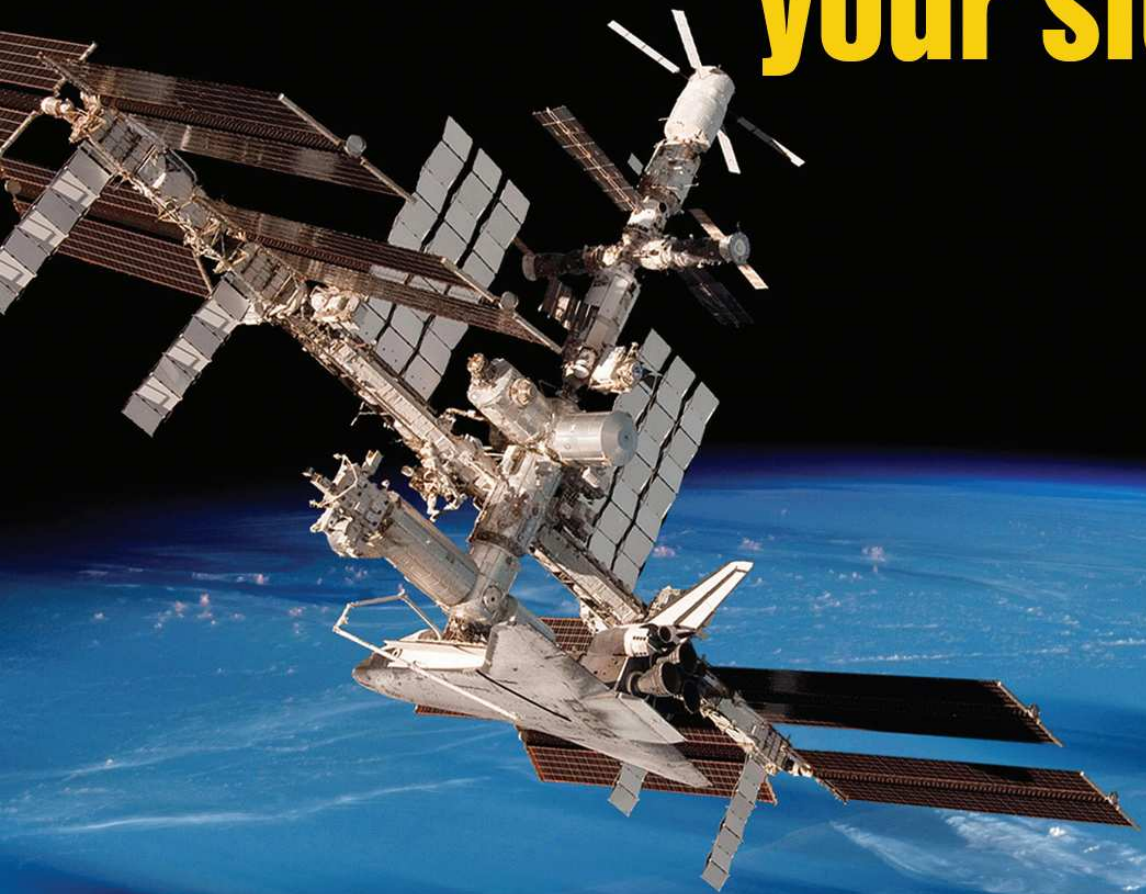

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Mulvihill: Not at this time. When the program was first developed 20+ years ago, the original plan was to expand the offering to a course module on HDI, and one on high-speed design. These topics are introduced in the 2016 edition of CID, and covered in more depth within the 2016 edition of CID+. Publication of a formal certification module takes a long time, due to requirements for multiple reviews. Developments in HDI and high-speed design happen so fast that formal certification module content could be outdated as soon as it is published.

For the most up-to-date information on HDI and other technologies that require advanced-level design, individuals concerned with design are encouraged to participate in tutorials, courses, and technical conferences. Examples include the professional development courses at IPC APEX EXPO, and the recent IPC Flexible Circuits-HDI Forum.

Shaughnessy: *Many of our readers feel standards and certifications should be free to members. How do you address the "free" contingent?*

Mulvihill: While it would be possible to construct a membership fee that would include all standards and certifications, the fee would be too high because not every employee of every member company would utilize all IPC products and services constantly. It is understandable that this question might be raised, as the incredible amount of time and effort that goes into association "products" like standards and certifications is not always apparent at first glance.

Shaughnessy: *What resources (book stores, etc.) are most important to your members?*

Mulvihill: IPC industry standards are our core offering. We are the only association in this electronics manufacturing industry to provide a platform for development and application of standards for all phases of product realization: design, manufacturing, inspection and test. IPC standards focus on manufacturability and reliability of the finished product, notably the high reliability required of products for the automotive, medical, military and aerospace sectors, as well as products like satellites and servers.

Shaughnessy: *How do you satisfy members' need for technical information?*

Mulvihill: Our mission is to provide industry standards and technical education, including training and certification, education with a design focus.

Shaughnessy: *Highlight some of the Designers Council's success stories.*

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Mulvihill: Veteran designers tell us that IPC Designer Certification is the best educational program for design practices in the industry. The CID and CID+ are professional designations respected throughout the industry, specified for major projects and utilized by major corporations for selection and promotion.

Shaughnessy: Do you have partnerships with other industry organizations?

Mulvihill: IPC works on projects in partnership with other industry organizations, notably:

- CALCE (Center for Advanced Lifecycle Engineering—University of Maryland)
- SMTA (Surface Mount Technology Association)
- EIPC (European Institute of Printed Circuits)
- FED (Fachverband für Design, Leiterplatten- und Elektronikfertigung—association for PCB design and manufacturing)
- AIA (Aerospace Industries Association)
- NAM (National Association of Manufacturers)
- WECC
- SEMI
- DDMII

Shaughnessy: Does the DC help members deal with government agencies?

Mulvihill: No. The IPC Government Relations team handles issues associated with environmental and governmental regulations that affect the electronics industries.

Shaughnessy: What are your most successful programs and why?

Mulvihill: The IPC 2581-Consortium was formed nearly 10 years ago. Persuading all of the major CAD software vendors to put aside their differences and bringing them to the table for good of the industry was a major effort. Drawing in OEM users to provide input and consent to utilize the standard for beta-testing was the next step. The next phase will be to apply the IPC-2581 to a larger number of facilities, using a variety of CAD software design and assembly tools.

This industry standard consists of generic protocols for consistent capturing and transmission of design data through all phases of product manufacture—the Holy Grail. This is a great achievement, culminating in a quiet revolution that could result in quality and efficiency improvements throughout the entire electronics industry.

Shaughnessy: Why should someone join the DC? It sounds like there are no risks, only rewards.

Mulvihill: Individuals in the electronics industry should have an awareness of the importance of design. Up to 75% of a product's cost and performance can be attributed to design.

Shaughnessy: Is there anything else you would like to share?

Mulvihill: For more information on the IPC Designers Council, please contact Kris Roberson, manager, Certification Development at 1-847-597-2846 or KrisRoberson@ipc.org.

Shaughnessy: Thanks for your time. See you at APEX!

Mulvihill: Thank you. **PCBDESIGN**

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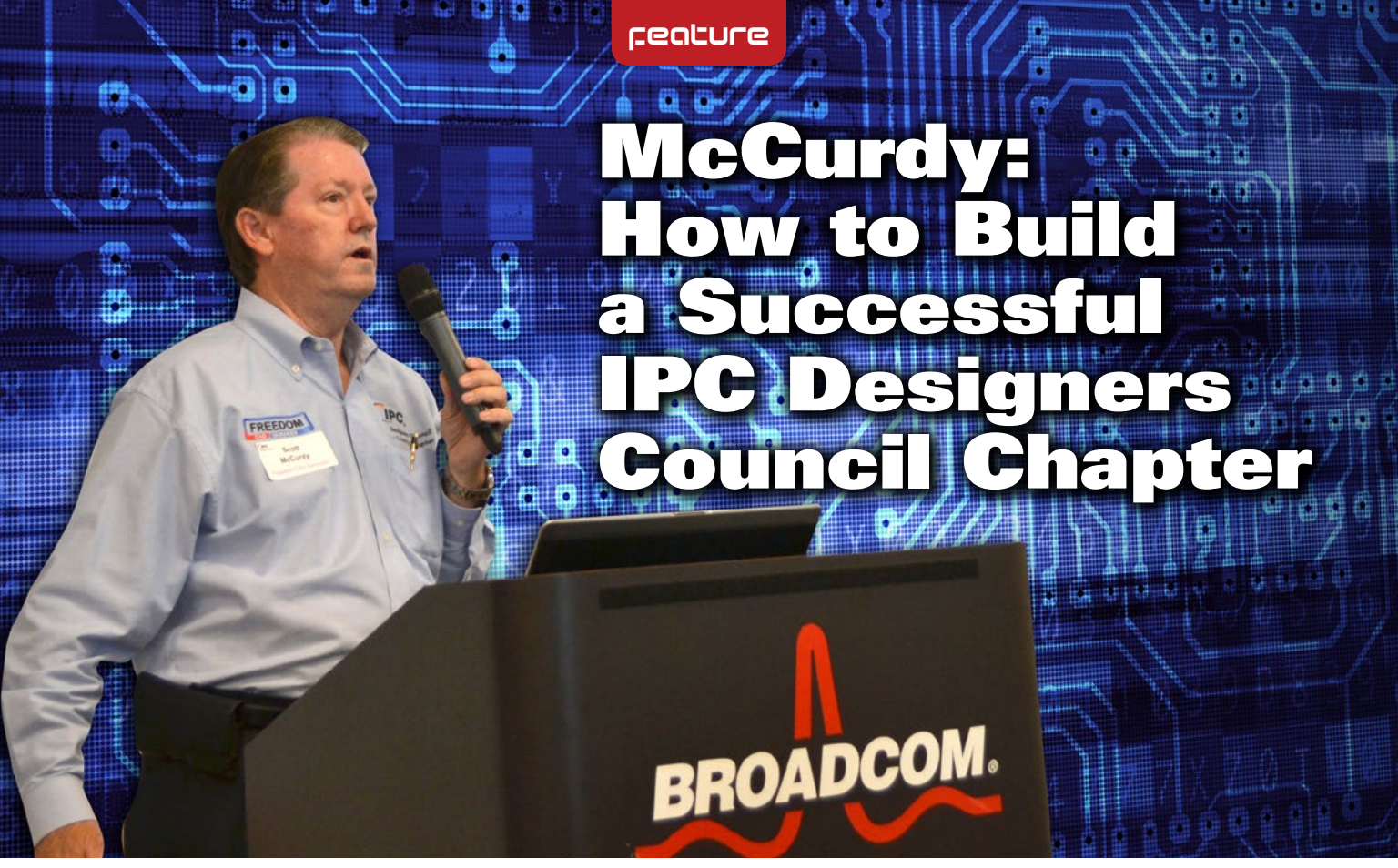


McCurdy: How to Build a Successful IPC Designers Council Chapter

by Judy Warner
ZENTECH MANUFACTURING

As a Southern California native and an industry veteran, the name Scott McCurdy is a familiar one for me. Scott has been in the electronics industry for 40+ years. Thirty-two of those years were spent building and running McCurdy Circuits, a successful PCB fabrication facility in Orange County. These days, Scott is focused on the design side of things as the director of sales and marketing for Freedom CAD Services, the largest independent design bureau in the nation.

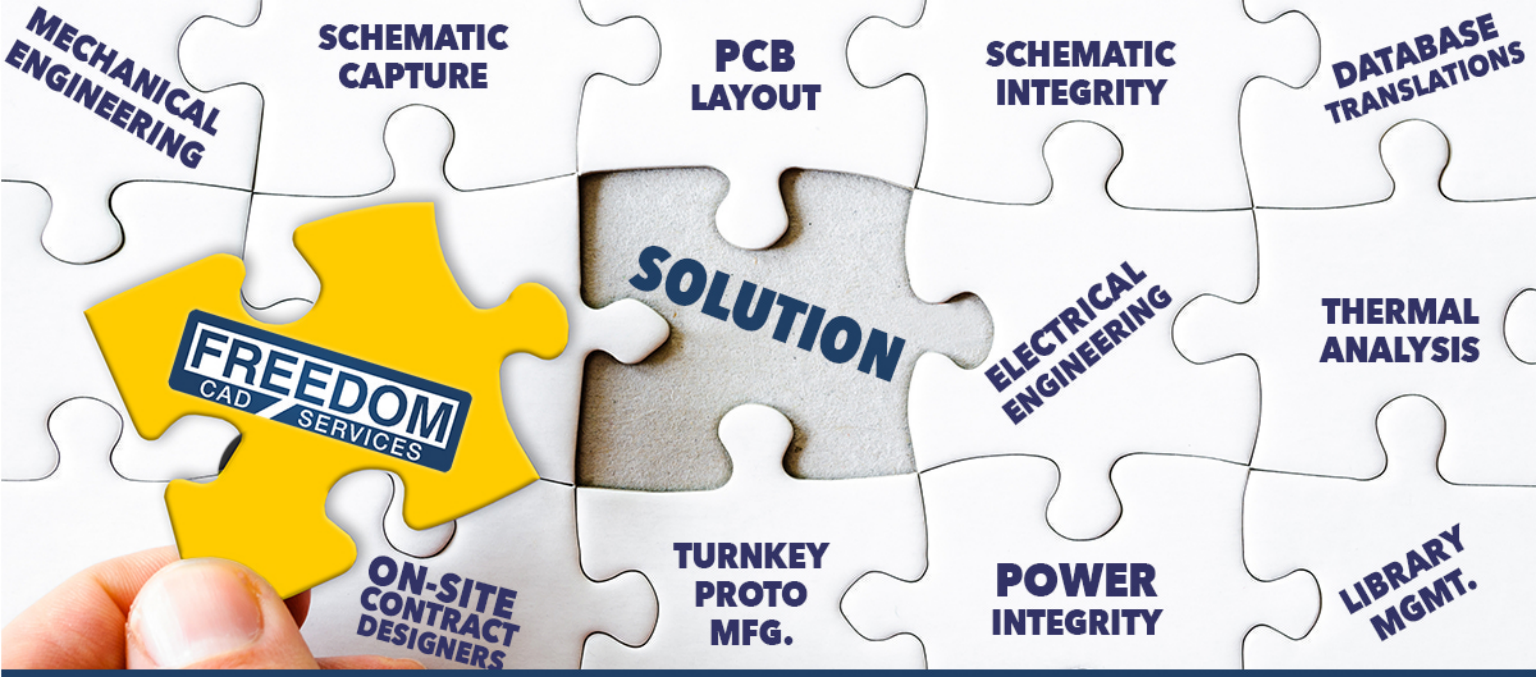
In his not-so-spare-time, he is also the president of the largest chapter of the IPC Designers Council in the country. Despite the fact that I've known about Scott since the mid-1980s, we only just met within the last year. Shortly after meeting Scott, he began encouraging me to attend the local Designers Council meetings that he hosts approximately 3–4 times per year in Irvine, California. Thankfully, although I stood him up for a couple of meetings, he persisted (a little friendly harassment) and eventually, pushing skepticism aside, I got around to finally experiencing what he was so enthused about.

Scott McCurdy

From Reluctance to Raving Fan

When I finally made that first meeting last March, I arrived late. As I tried to slink in the door unnoticed, I awkwardly realized there wasn't an empty seat in the house--until one magically appeared in the back of the room. I was awestruck by the attendance of 77 otherwise busy designers and electronics professionals who filled the room. Tom Hausherr of PCB Libraries was the featured speaker for my first meeting.

The next meeting was held in June at a member location, Broadcom. That meeting featured two speakers: Matt Isaacs, technical director of Broadcom and Julie Ellis, a field application engineer with TTM; nearly 100 people attended. My third meeting, which took place at Harvard Park Community Center in Irvine on Novem-



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ber 18, broke the attendance record for their home meeting location, topping out at 89 attendees. Chris Heard of CSH Consulting gave a rich and granular talk about signal integrity and power issues relative to routing guidelines and layout features. At these meetings, I witnessed designers being granted access to a very high level of educational and networking opportunities that deeply enriched and inspired them to grow as professionals. In some cases, it has inspired them to even further their formal education or certifications that helps them compete in a fierce global marketplace. In a matter months, I had been transformed from skeptic to a raving fan!

On Becoming the Accidental Chapter President

After the last meeting, I had the opportunity to talk at length with Scott about his 13-year tenure as the Orange County chapter president. It's clear that he is absolutely passionate about the value of the Designers Council and the immense educational value and resources it can deliver to the industry in a convenient, low cost and regional context. In our time together, he openly shared his "playbook" on how to build and run a successful Designer's Council chapter, which he is eager share with others who may be interested in launching a local chapter would like to emulate his success. The excitement and generosity he showed instantly compelled me to pass on both his story and his recipe for success.

When Scott made his transition from PCB fabrication to a PCB layout focus, about 13 years ago, he accepted an invitation to attend our local IPC Designer's Council. Shortly after, he was recruited to serve on the group's steering committee. At that time, 20–25 people were regularly attending the meetings. Within 3–4 months, the chapter's president made an unforeseen move to Arizona and he asked Scott to take his place.

Since that time more than 12 years ago, he has continually served as the chapter's president and has grown it into the nation's largest chapter. He is quick to give credit to the tremendous support he has had from Terri Kleekamp of Mentor Graphics, and Kathy Palumbo of Production Analysis and Learning Services, who have faithfully supported the chapter since before he arrived. They have both been an invaluable help as chapter secretary and treasurer, respectively.

Although this role came along unexpectedly, Scott immediately rolled up his sleeves and went to work to raise awareness of the meetings to our local PCB design and electronics community. He began by e-mailing invitations and making face-to-face appointments with design professionals and personally inviting people to attend and participate in the local events. The meetings were held at Mentor Graphics 4–5 times per year. In short, Scott built the local Orange County chapter by building relationships one at a time through some hard work and his signature dogged persistence.

Meeting attendance doubled almost immediately, causing them to eventually outgrow the Mentor Graphics office and move to its current location. With the support of Terri and Kathy, attendance grew, in fits and starts, until it became what it is today.

McCurdy's Playbook for Success

For those of you who may have considered starting a local chapter, or who currently run a Designers Council chapter, here is some basic information from McCurdy's playbook, which he has been improving for nearly 13 years.

First of all, IPC Designers Council membership is free, and you can register here. To find out more about starting a local chapter contact

IPC by clicking here. Kris Roberson is the point of contact for Designers Council chapters at IPC.

The essentials of running a good meeting consist of the following:

- Although some chapters hold evening meetings, Scott has found that holding the "Lunch and Learn" events from11:30 a.m. – 1:30 p.m. works well. This makes little impact on a busy professional's working hours, and does not infringe on personal or family time in the evenings. Traffic patterns in busy cities are also lighter in that time slot. Most companies will support time away from the office when it is the equivalent to a long lunch to serve continuing education.
- Find relevant speakers who are valuable to the PCB design community. Choose one speaker to talk for 80 minutes, or two speakers to talk for 40 minutes each.
- Meeting times run two hours; 80 minutes are reserved for speakers. Lunch and announcements account for another 30 minutes, and the remainder is set aside for questions, raffle and closing.
- Always make name tags that are easily readable and that also include the company name for ease of networking.
- Provide box lunches from a local sandwich shop, and charge approximately $10 at the door to help cover costs of facility and food/drinks.
- Proactively network between and during meetings to build rapport and keep a growing database for the chapter.
- Occasionally take on-site field trips to provide learning opportunities and to raise awareness of member companies (i.e., PCB fabrication facilities, design bureaus, OEMs, or contract manufacturers).
- Get member companies to sponsor some simple prizes to raffle at the end of the meeting.
- The president should greet members as they arrive and as they depart, and thank them for attending.
- Get help from a few volunteers to help shoulder the work involved. It takes a team to grow a chapter!
- If you can, get a member company to open up a meeting space at no charge to help keep costs to a minimum.
- Include opening slides that include:
  - A greeting and welcome
  - IPC information and website link
  - Information and links for industry magazines/news sources
  - Share information regarding upcoming local events, such as tradeshows
  - Open the floor to ask if anyone is hiring or looking for a design job in order to make potential matches
- Encourage feedback and ask attendees about topics and speakers they would like to hear from.
- Give handouts to gather contact information about the attendees, and add new info to the database.
- Provide the website links mentioned in the opening slides in written form.
- Ask the speakers to provide the slides from their talk, removing any proprietary information, and forward to the attendees via email or a customized website.

Give with Purpose: Educate, Network, Inspire

While Scott McCurdy's "recipe" is a fairly simple one, there is one intangible quality that I observed that appears to have contributed greatly to his success with the Orange County

Chapter: He's a giver. Scott doesn't give to get something in return—he gives for the joy of contributing to our industry. And he has surrounded himself with like-minded contributors like Terri Kleekamp, Kathy Palumbo and others. He enjoys providing designers with resources that will educate, inspire and allow them to network with their peers. Subsequently, designers become better at what they do, which empowers them to compete well globally. Generosity and altruism are at the heart of Scott's and his team's success.

If you want to follow in Scott's shoes and set up your own Designers Council chapter, be a purposeful giver. Beyond that, carve out some time to build relationships in order to support your efforts and to grow meeting attendance. No matter how much we rely on our electronic devices to inform and connect us, nothing compares to the power and value of meaningful face time. Scott's playbook, and his support of local design professionals, are keys to his chapter's success. **PCBDESIGN**

Judy Warner is director of business development for the Western Region and RF/microwave markets for Zentech Manufacturing.

Nanostructured Metal Coatings Let the Light through for Electronic Devices

Light and electricity dance a complicated tango in devices like LEDs, solar cells and sensors. A new anti-reflection coating developed by engineers at the University of Illinois at Urbana Champaign, in collaboration with researchers at the University of Massachusetts at Lowell, lets light through without hampering the flow of electricity, a step that could increase efficiency in such devices.

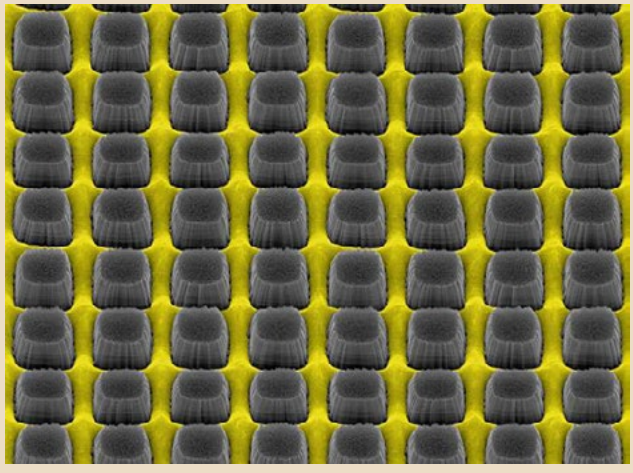
The researchers, led by U. of I. electrical and computer engineering professor Daniel Wasserman, published their findings in the journal Advanced Materials.

At the interface between two materials, such as a semiconductor and air, some light is always reflected, Wasserman said. This limits the efficiency of optoelectronic devices. If light is emitted in a semiconductor, some fraction of this light will never escape the semiconductor material. Alternatively, for a sensor or solar cell, some fraction of light will never make it to the detector to be collected and turned into an electrical signal. Researchers use a model called Fresnel's equations to describe the reflection and transmission at the interface between two materials.

"It has been long known that structuring the surface of a material can increase light transmission," said study co-author Viktor Podolskiy, a professor at the University of Massachusetts at Lowell. "Among such structures, one of the more interesting is similar to structures found in nature, and is referred to as a 'moth-eye' pattern: tiny nanopillars which can 'beat' the Fresnel equations at certain wavelengths and angles."

Although such patterned surfaces aid in light transmission, they hinder electrical transmission, creating a barrier to the underlying electrical material.

The researchers demonstrated that their technique, which results in metal covering roughly half of the surface, can transmit about 90 percent of light to or from the surface.



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Designers Council Viewpoint: Gary Ferrari

When we started putting together our coverage of the Designers Council, we knew we'd have to get the real scoop from Gary Ferrari. He's been helping to raise the status of the PCB designer for decades. As co-founder and long-time executive director of the Designers Council, as well as an IPC Master Instructor, Gary has dedicated a big part of his career to PCB design. After decades of service, he was inducted into the IPC Hall of Fame at IPC APEX EXPO this year.

I caught up with Gary and asked him to fill us in on the creation of the Designers Council, and some of the changes he's seen in the organization in the last 24 years.

***Andy Shaughnessy:** You're often referred to as the "Founder of the Designers Council." How did you get involved and who else helped get the DC started?*

Gary Ferrari: As you know, Dieter Bergman and I worked together on many of the standards that affect designers. We also did several designer-oriented workshops. One day, Dieter asked me what more IPC could do for the design community. My answer was very simple: "Mechanical engineers have the ASME, electrical engineers have IEEE, and the designers have sore eyes from staring at their monitors. What we need is a society for board designers, and anyone with a vested interest in board design."

Gary Ferrari

In 1991, we hit the road and traveled throughout the U.S. to introduce a new design standard. It also gave us an opportunity to poll the attendees to hear their comments on whether an IPC Designers Council was a good idea. We also asked them what they felt its charter should be. The primary feedback was designer education, a forum to discuss common interests, and network building. In summary, they liked the idea of a designer society.

However, an issue was IPC's membership structure. Their membership is company-based, whereas a society is generally individual-based, similar to SMTA. After consulting with IPC's legal counsel, we were able to structure the Designers Council as a chapter-based entity, thus allowing for individual membership.

***Shaughnessy:** Where was the first official DC meeting held, and when?*

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IPC DESIGNERS COUNCIL VIEWPOINT: GARY FERRARI

Ferrari: Its official birth was in 1992. Dieter and I were making the rounds doing design-related workshops at that time, and spreading the word. Chapters started forming at a tremendous rate. We were up to 29 chapters within several months.

What is interesting to note is that a group of Atlanta designers had been meeting together for about a year under the leadership of Fred Pescitelli, at Phoenix Designs. They met to learn from each other, learn about new technologies, etc. Sounds familiar doesn't it? They listened to what we offered, voted, and Atlanta became the first official chapter of the IPC Designers Council.

No matter where I traveled, the local designers basically said the same things. One that comes to mind was in Atlanta. One of the well-known designers, when asked the how he felt designers were viewed, indicated that the attitude was that designers were "pond scum." We can certainly laugh at his colorful description, but I received similar answers no matter where I traveled.

Shaughnessy: What are the biggest changes you've seen at the DC in the past 24 years?

Ferrari: There are fewer registered chapters in the U.S., whereas we have seen a much larger growth internationally. However, we have recently witnessed a few new chapters starting up. We are also seeing more and more engineers taking the certification courses. I recently taught a class that consisted of over 90% engineers. In addition, we see a growth of new, younger designers taking the courses.

Two reasons may be attributed to these observations. The first is that technology has become more sophisticated, and engineers are being asked to move further into the layout end of the development cycle. The second is that the average age of the designer keeps climbing up, resulting in much larger numbers getting ready for retirement. Companies are finally waking up to the fact that they will be losing a significant part of their product development team, better known as the PCB designer.

Shaughnessy: What do you think are the biggest benefits that the Designers Council offers designers, and the industry?

Ferrari: This answer is three-fold. The first is exposure to industry standards, which includes many important processes that are affected by design. Let's face it, with today's technologies, the designer cannot ignore what his design may do to the fabrication, assembly and test segments.

The second is obtaining a professional credential that has international recognition.

The third is building a network of experts that one may call on when faced with a new or difficult design issue.

Shaughnessy: What's exciting about the DC today?

Ferrari: In the certification program, we see many new design challenges facing the designer. These are worldwide challenges that create new horizons. In other words, I see plenty of growth for those who are coming into the field, as well as those who have been around for a while. As chairman for several IPC design-related standards, I look for a path into the standards for these challenges, and ultimately into the designer certification courses. For me, I have to mention all the designers I have met and helped in one way or another. To see them grow and be successful is amazing.

Shaughnessy: Why should someone consider joining the DC?

Ferrari: Technology does not wait for designers to catch up. It moves forward and designers need a venue that enables them to keep up with these technology changes through education and networking. Being involved in a local Designers Council chapter may provide the catalyst for their employers to allow them to attend various conferences and help expand their knowledge.

Shaughnessy: Thanks, Gary.

Ferrari: Thank you. **PCBDESIGN**

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Designers Council Viewpoint: Rick Hartley

by Andy Shaughnessy

Rick Hartley has been in involved in PCB design and design education for decades, so it's no surprise that he started working with the IPC Designers Council early on. Now retired from his day job at L-3, Rick still teaches PCB design and shows no sign of slowing down. I asked him to discuss his work with the Designers Council, and what the group means to the design community.

Rick Hartley

Andy Shaughnessy: *How and when did you get involved in the Designers Council?*

Rick Hartley: I first learned about the Designers Council at an IPC conference in the early 1990s. Shortly afterward, I was contacted by another central Ohio designer, Candice Antrett, of Battelle Research Institute. Candice was also interested in the DC and suggested we collectively start a chapter. Pete Waddell had Printed Circuit Design magazine do a mailing for us to help get the word out, and we have always been grateful for that generous act. We held our first meeting at Battelle, and were off and running. Our membership area was mainly Columbus, Dayton and Cincinnati.

Shaughnessy: *What are the some of the most important benefits that the Designers Council offers designers, and the industry?*

Hartley: For those chapters that are still going strong, the benefits are massive. There is NO formal education in PCB design. For the most part, colleges do not teach the profession. Some colleges barely even mention the existence of PC boards, much less tell their students anything meaningful. IPC and the active DC chapters are doing a wonderful job of training the industry

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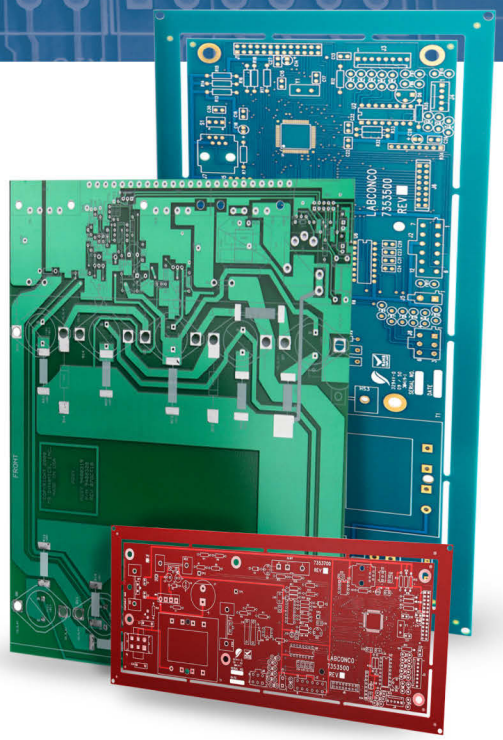

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IPC DESIGNERS COUNCIL VIEWPOINT: RICK HARTLEY

about the many issues we need to understand; I don't mean just designing to make boards function, but incredibly important issues like DFX (i.e., design for fabrication, design for assembly and design for testability). For people who do not live in the area of an active chapter, there is the IPC APEX EXPO conference and other wonderful educational resources, such as PCB West Design Conference and online webinars from multiple sources, including IPC.

***Shaughnessy:** What's exciting about the DC today?*

Hartley: All the items mentioned earlier. And, of course, there is the CID (Certified Interconnect Designer) and CID+ (Advanced) training and certification. This can be a very valuable asset to designers and EEs. One of the greatest benefits I derived from chapter membership was networking. I could write a book on the value of networking with others in your profession. Those folks lucky enough to still have a local chapter and those who network at conferences know exactly what I mean.

***Shaughnessy:** We've covered a few DC meetings and "lunch and learns" lately, and they've had good attendance. Are the local chapters becoming more active, like they were a few years ago?*

Hartley: The chapters that are active are very active. A great example is the Orange County chapter in Southern California. These guys are doing a fantastic job of training and educating designers, fabricators and assembly people. I cannot say enough about the great work that Scott McCurdy and the other officers of the Orange County chapter are doing.

Unfortunately, in recent years, a number of other chapters have become less active, the Greater Ohio chapter included. We did not lose interest; we were mainly a self-education group and, after 14 years, simply ran out of things to tell each other. We were fortunate to have a fair number of people with something valuable to say, and we did it for 14 years. We have been talking lately about possibly rekindling the flames. It's been just long enough that we believe we have new things we can teach each other. Anyone who wants to know more about the Designers Council can find information on IPC's website. If you want to get more involved in education for the industry, don't just join the DC; start a local chapter and help to educate others.

***Shaughnessy:** You're the vice chair for the DC. Where is the group headed in the next few years?*

Hartley: We are constantly updating and improving the CID and CID+ training. These are complex training programs and they are ever-developing. Also, there has been talk for years about Focus Modules that would be used to train people in specific disciplines related to CID and CID+ (HDI, EMI, etc.). We continue to discuss these possibilities. We are always looking for ways to educate the industry.

***Shaughnessy:** In addition to the benefits you mentioned earlier, why else should someone consider joining the DC?*

Hartley: Education and networking! When I decided 23 years ago to teach at our local chapter meetings, I had no clue how much I would learn in the process of developing training material to educate others. If your goal is to better yourself, don't just go to conferences. Get involved!

***Shaughnessy:** Thanks, Rick.*

Hartley: Thank you, Andy. **PCBDESIGN**

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Designers Council Viewpoint: Mike Creeden

by Andy Shaughnessy

When covering the IPC Designers Council, one quickly learns that it's the volunteers who make the train run on time. San Diego PCB CEO Mike Creeden, CID+, is one such volunteer, and as a member of the Designers Council's Executive Board, he was a must-have for this issue. I tracked him down and asked him to give us a rundown of his involvement with the DC, and to explain why designers might want to get involved with their local DC chapters.

***Andy Shaughnessy:** How and when did you get involved in the Designers Council?*

Mike Creeden: Around1993, I was presented by a fellow designer an invitation to attend a new meeting called the "IPC Designers Council," which was being held at Qualcomm. I had known of IPC for most of my career of 17 years, but I did not know anything about a Designers Council. So, being curious by nature, I attended this meeting and immediately saw several fellow designers I was well acquainted with, and then I met several new people whom I still see to this day. There was some good food and it was an event outside of work, so I really started to enjoy the meeting.

What came next was profound. I was exposed to IPC standards and the value they brought to my designs, my company and ultimately my career! I saw that the charter of these meeting was to bring this education out to the designer in the workplace as a form of education. So being the naïve person I am, I asked, "What are we doing to get this message out there to those that don't know about this Designers Council chapter?" The response was simple. "What do you think we should do and how would you like to go about it?" I was nominated as the Education board member and had the privilege to serve for several years.

***Shaughnessy:** What do you think are the most important benefits that the Designers Council offers designers and the industry?*

Creeden: The Designers Council is a multifaceted organization and as such has been several different things to me over the years. I assume this must be true for other people as well. The primary benefit that the DC brings is improve-

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IPC DESIGNERS COUNCIL VIEWPOINT: MIKE CREEDEN

Mike Creeden

ments to the products in our industry. It does so by way of improving the knowledge base of each designer who attends and participates. The products we design become more reliable by applying the proven standards as determined by the experts in the industry, from a cross-section of the marketplace.

When we as designers bring improvements to our company, we're recognized by our peers and by our employers. We may not always be rewarded, but as your value goes up, maybe it's time to find a company that would recognize and reward your value. Another aspect that I mentioned earlier is the opportunity to network with others in your profession. This can be in the form of meeting old friends or making new friends. Maybe it is a time when you can learn some helpful methods to deal with technical issues or a professional response to something that was occurring in your workplace. Often, business connections and business deals can occur based on the contacts that you make through the Designers Council. When someone sees you attending, participating, and contributing in a public forum, they may become interested in services you offer, your expertise, and your ability to use it well.

Shaughnessy: *What's exciting about the DC today?*

Creeden: What I find very exciting about the Designers Council is the wealth of knowledge that is presented and exchanged by the members of the group, not to mention the guest speakers that present at the chapter meetings. Our chapter has been known to take field trips to various manufacturing companies; they often provide an educational tour of their facilities and explain the process flow. The fabricators teach us how to avoid common mistakes and better understand the process. With the rapid pace that technology is moving it is imperative to stay current with the industry trends and technical requirements.

Shaughnessy: *You're on the executive board for the DC. How does the board operate?*

Creeden: The executive board is a group of individuals who understand the value of service. Almost everyone participates at the expense of personal time and resources. Their commitment to the improvement of our industry is humbling to watch at times. They do not serve for the reward or prestige of office. They seem to serve for the betterment of their industry and the growth of knowledge.

The board meetings themselves are often very casual events that include food, a lot of good jokes, and several intriguing stories. But when it comes down to business, it is professional and orderly. A few officers are voted into positions for a term. The executive board defines and supports the Designer Certification Program (CID and CID+) as owned by IPC and facilitated by companies like EPTAC. The board members are typically significant contributors to IPC efforts and industry-related technical training sessions held across the country each year.

All local Designers Council chapters are autonomous. Groups have a general charter as defined by the executive board and posted on IPC's website. Each local chapter tends to take on its own identity based on the participation of each group.

Shaughnessy: *Mike, thanks for your time.*

Creeden: Thank you. **PCBDESIGN**

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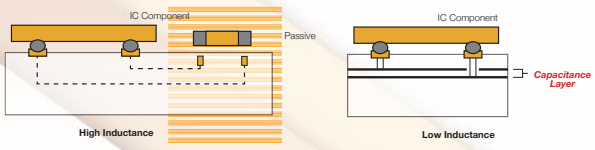

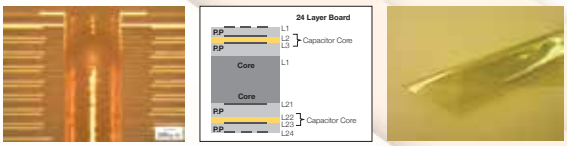

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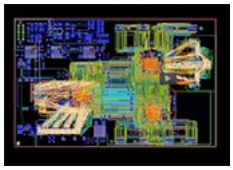
Engineer Steve Weir Has Passed Away

Steve was a power and signal integrity guru with a variety of patents to his name. A fixture of DesignCon and a constant presence on the SI-List signal integrity forum, Steve wrote over a dozen papers on power integrity. He also had a crazy, irreverent sense of humor that you don't find among most engineers. He will be missed.

Mentor Graphics Launches New HyperLynx SI/PI Product



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Sunstone Circuits Chooses InSight PCB Software for Pre-CAM and Sales

Sunstone Circuits has purchased Orbotech's InSight PCB pre-sales and pre-engineering software. InSight PCB is a web-based tool for managing and assessing incoming customer PCB data for salespeople and engineers who are not CAM experts. From automatically retrieving comprehensive product information to generating precise summary reports, InSight PCB empowers sales and engineering people to work more independently, efficiently and profitably.

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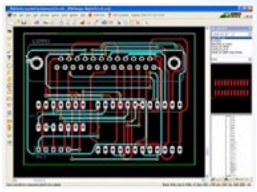

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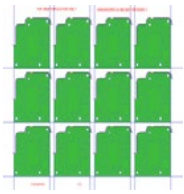


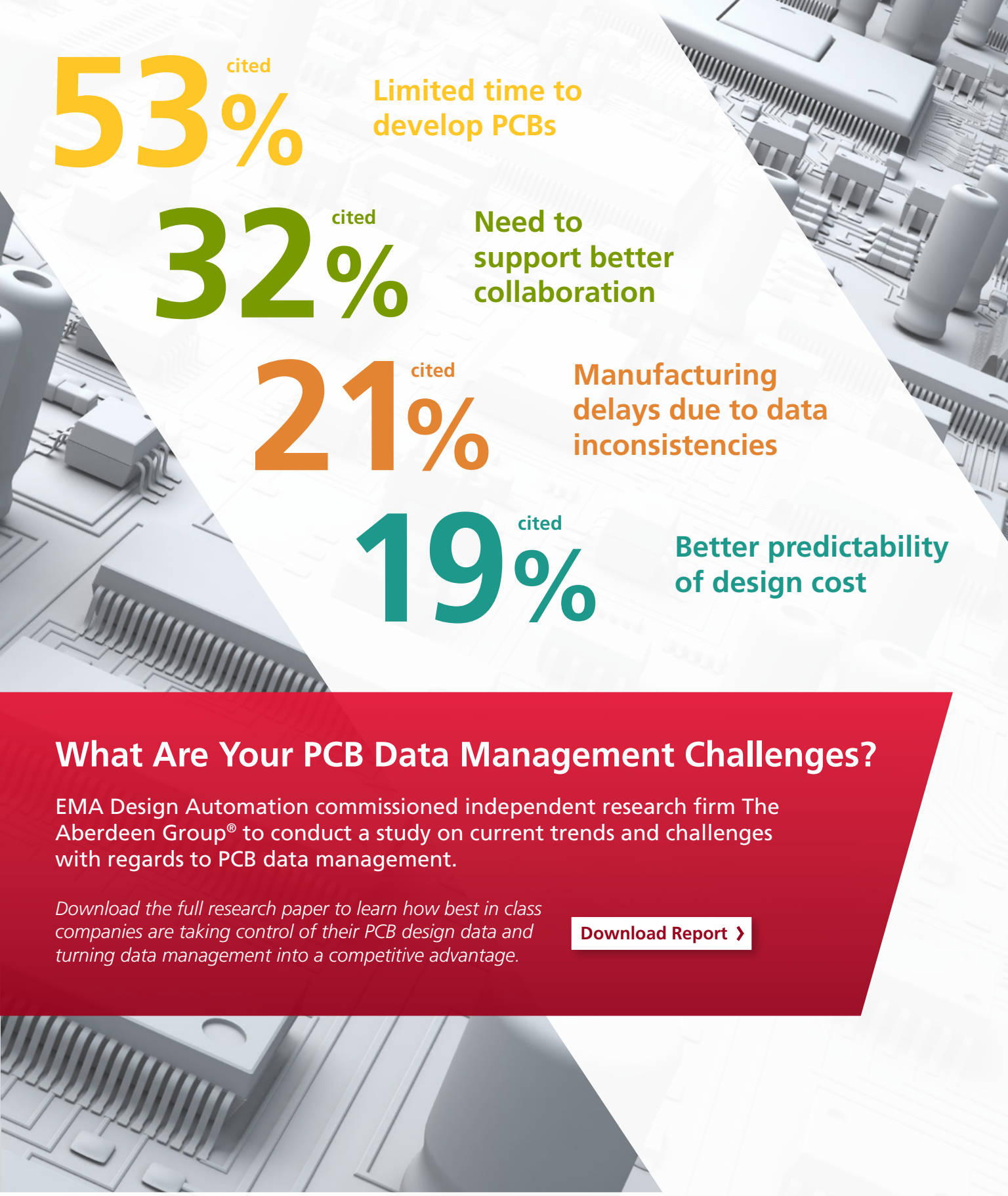
WestDev Ltd. has released the latest version of Pulsonix 8.5, Build 5902. This maintenance update is issued as part of our on-going process of product improvement and response to customer feedback. In addition to bug fixes, the latest release contains several additions to the Report Maker function.

Exception PCB Solutions Design Service Boosts CID+ Qualifications

Heading up the design service is Neil Day, who has completed the IPC PCB Designer Certification Program and became qualified as an Advanced Certified Interconnect Designer (CID+). In addition, Technical Support Manager Paul Beech has completed the IPC CID training course and attained CID certification.

Polar Instruments Launches New Language Versions of The Speedstack PCB Layer Stackup Design System

Polar Instruments has launched new language versions of Speedstack, the industry's best-selling PCB layer stackup design system. In addition to English, Speedstack is now available in German, Japanese, simplified Chinese and traditional Chinese versions. Speedstack allows PCB fabricators to fine-tune the stackup design by assessing the impact of different PCB materials on cost, performance and manufacturing yield.



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Plane Crazy, Part 1

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD AUSTRALIA

A high-speed digital power distribution network (PDN) must provide a low inductance, low impedance path between all ICs on the PCB that need to communicate. In order to reduce the inductance, we must also minimize the loop area enclosed by the current flow. Obviously, the most practical way to achieve this is to use power and ground planes in a multilayer stackup. In this two-part column, I will look at the alternatives to planes, why planes are used for high-speed design and the best combination for your application.

Back in the mid-eighties, when I worked at the University of Western Australia, one of my duties was to fix the departmental mainframe: the dreaded DEC PDP-11/40. When it broke down, it was a two-week sentence to solitary confinement in the frigid computer room. This monster machine had card after card with rows of TTL logic chips. Figure 1 illustrates a typical Unibus board. It had 8K, 16-bit word core memory, which I believe could be expanded to 80K if the need ever arose. The core had a 400ns access time, which means the system clock would have been a blazing 2.5MHz.

I always used the "divide and conquer" methodology. First, eliminate the power supplies then start dividing the system in half, then half again until the fault was localized within a small circuit. But, as it took about half an hour to reboot, with a specific sequence of octal latches, it was a very time consuming process. Plus, there were always numerous engineering students banging on the window, to the terminal room, enquiring when the "mother" might be fixed so they could complete their assignments.

The boards were double-sided and used a power finger, type A or B layout configuration on the top side of the board, as shown in Figure 2. The bottom side could then be used entirely

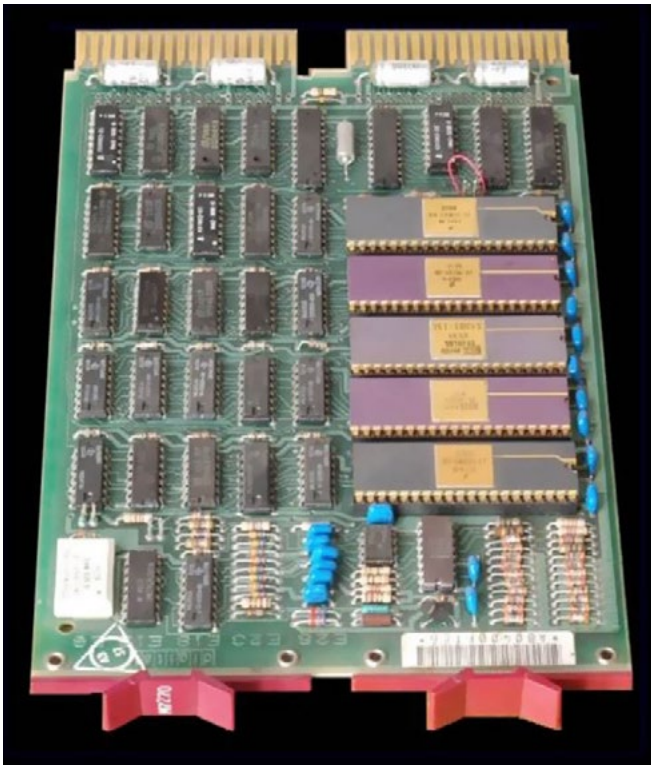

Figure 1: Unibus board (courtesy of DEC).

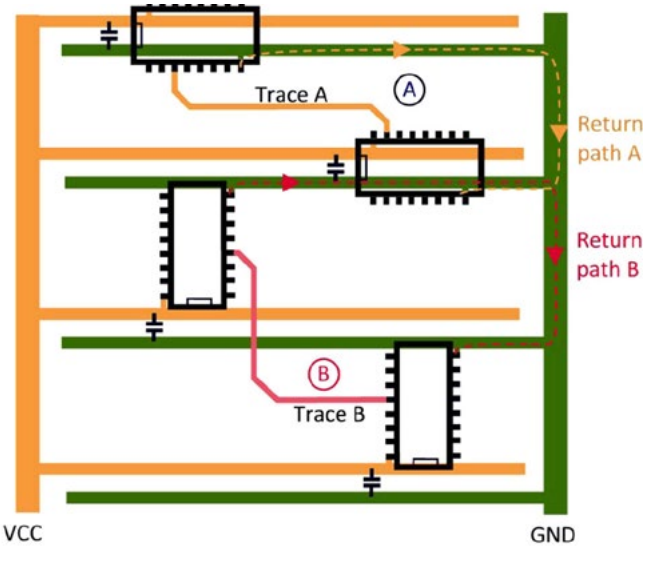

Figure 2: Power finger configuration.

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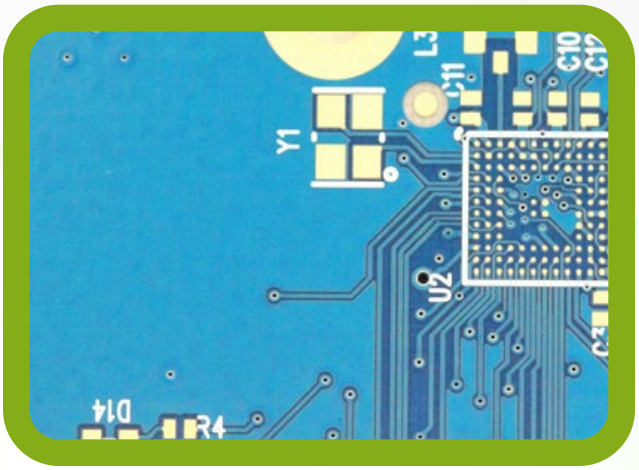

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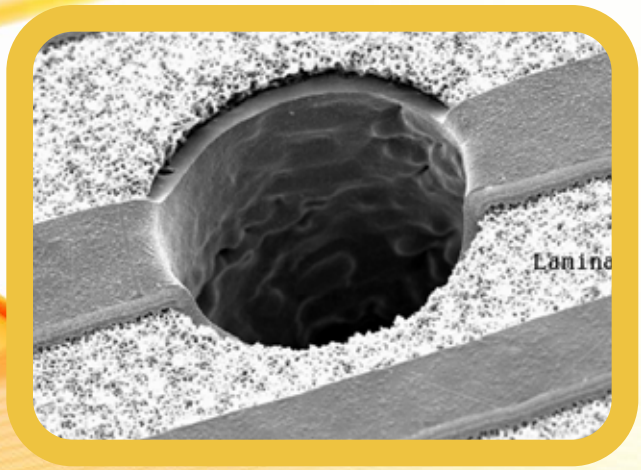

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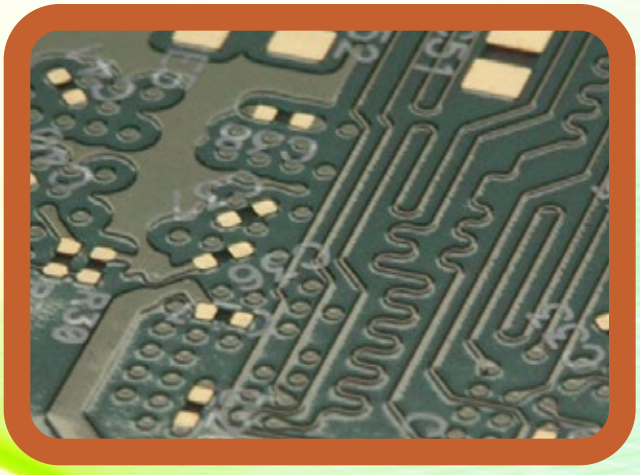

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for routing. This provided some mutual inductive coupling between the wide power and ground traces and saved on board area. However, it meant that the return current had to flow all the way around the board perimeter, creating a large loop area. Fortunately, the PDP-11/40 was manufactured way before the era of FCC-mandated radiation guidelines. Needless to say, this is not a good supply configuration for high-speed design. Don't try this at home!

The power and ground grid configuration of Figure 3 also saves on board area, but at the expense of increased mutual inductance. In this case, the ground (GND) traces are horizontal on the bottom of the board, while the power (VCC) traces are vertical on the top side. Connecting the two supplies, at every intersection, with a decoupling capacitor forms a cross-hatch pattern. Current returns equally well, to its source, along either the ground or power traces. The down-side here is that the capacitors used should be of particularly good quality (low ESL) as the return current must traverse several capacitors to return to the source. If you are limited to a double sided board, then this is the best approach for providing power to the network of chips. But, solid copper planes, in a multilayer configuration, are of course a much, much better solution for high-speed design.

Although it is true that a plane has significantly less inductance than a trace, plane inductance is not negligible. The mechanism by which a plane reduces the inductance is by allowing the current to spread out, effectively creating numerous parallel paths. But at high speeds, return currents flow the path of least inductance which tends to direct the current directly below the signal trace.

Also, due to skin effect, high-frequency currents cannot penetrate a plane, and therefore, all currents in conductors are surface currents. This effect will begin to occur at frequencies above 30 MHz for 1 oz. copper layers in a PCB. Therefore, at high frequencies, a plane in a PCB is really

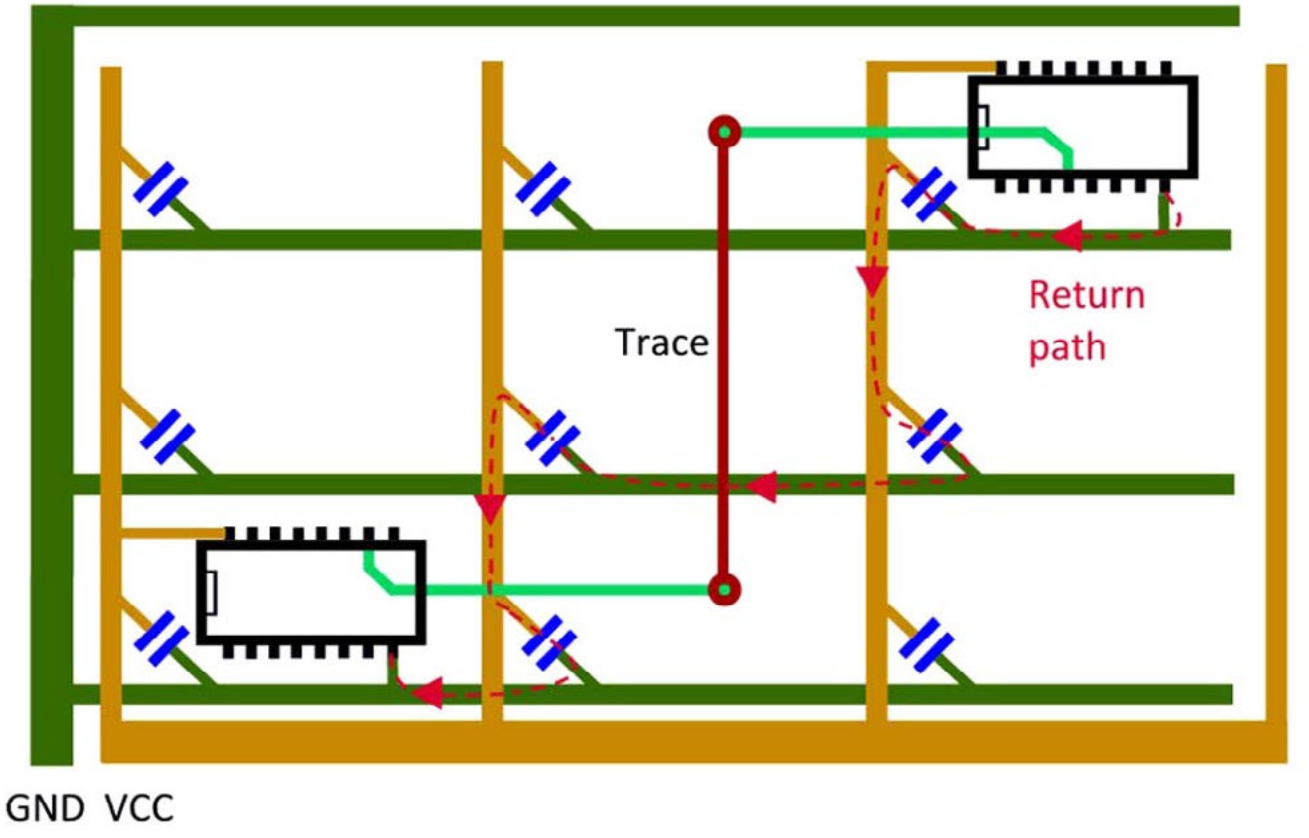

Figure 3: Power and ground grid configuration.

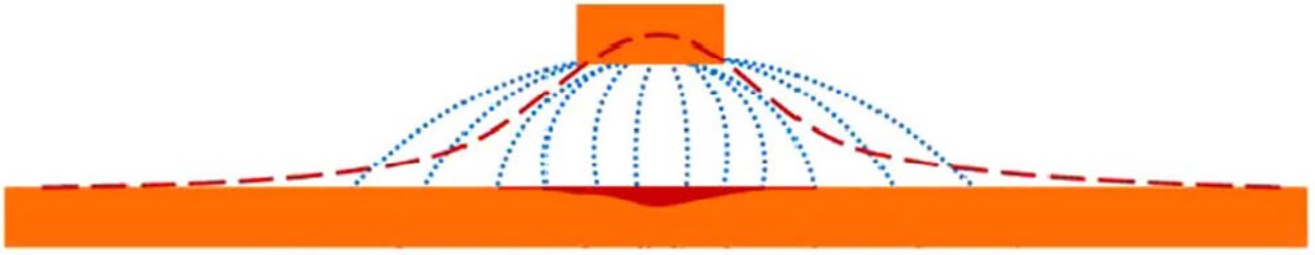

Figure 4: Microstrip plane return current distribution.

two conductors—not one conductor. There will be a current on the top surface of the plane, and there can be a different current or no current at all on the bottom surface of the plane.

Figure 4 illustrates the cross-section on a microstrip (outer layer) trace and its associated plane return current distribution (red). Where the electric fields (blue) are more tightly coupled to the plane—directly below the trace—the return current also exhibits tighter coupling. But where the field spreads out from the trace, the larger loop area, between the signal and the return current path, increases the inductance. Return current tends to couple to the signal conductor and on the same side, of the plane nearest the signal, falling off in intensity, with the square of increased distance. A stripline (inner layer) return current distribution is narrower with the fields more intense above and below the trace.

Any voltage drop across a ground plane will excite cables terminating on the board, which causes them to radiate as dipole or monopole antennae. The amount of current needed to cause the radiation to exceed the FCC Class B emission requirements, in a one meter long antenna, is extremely small—in the vicinity of just a few µA. Therefore, even the smallest ground noise voltage is significant, since it only takes a few mV of potential to produce currents of this magnitude. Power and ground planes reduce the loop area and hence the inductance and the impedance, which in turn reduces the noise.

Although single-sided and double-sided boards have been used successfully in unshielded enclosures at frequencies of 20–25MHz, these cases are the exception rather than the rule. A design of this type, also requires a high level of EMC expertise and thus is time consuming and risky to produce. Above 10MHz, multilayer PCBs with at least two plane layers should be seriously considered.

Multilayer boards reduce radiated emissions by more than 10 db compared to a double-sided board—all other factors being equal. Embedding signals between the planes also reduces susceptibility to radiation, as well as providing ESD protection. So not only do we prevent noise from being radiated, but we also reduce the possibility of being affected by an external source.

The planes in a high-speed, digital board perform five crucial functions:

1. Allow the routing of controlled impedance transmission lines in both microstrip and stripline configurations.
2. Provide a reference voltage for the exchange of digital signals.
3. Distribute stable power to all logic devices.
4. Control crosstalk between switching signals.
5. Provide a shield for electromagnetic radiation on internal layers.

Next month, I will look at why solid power and ground planes encompass a distributed system of surprising complexity and how we can best use planar capacitance to reduce AC impedance of the PDN.

Points to Remember:

- Inductance may be reduced by minimizing the loop area enclosed by the current flow.
- Double-sided boards, using a power finger layout configuration, should be avoided as they create a large loop area for the return current.

- The power and ground grid configuration is the best approach for providing power delivery on double sided boards.
- Solid copper planes are a much better solution for high-speed design.
- At high speeds, return currents flow the path of least inductance which tends to direct the current directly below the signal trace.
- At high frequencies, a plane in a PCB is really two conductors, not one conductor, due to the skin effect.
- Any voltage drop across a ground plane will excite cables terminating on the board, which causes them to radiate as dipole or monopole antennae.
- Above 10MHz, multilayer PCBs with at least two plane layers should be seriously considered.
- Multilayer boards reduce radiated emission by more than 10 db compared to a double-sided board. **PCBDESIGN**

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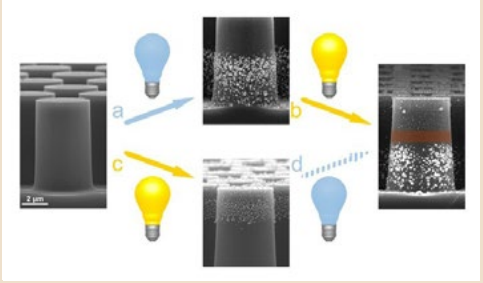
Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

University of Twente Develops Versatile Method for Developing New Materials

Researchers at the University of Twente research institute MESA+ have devised an elegant method for fitting various functional coatings to silicon microwires. The research has been published today in the prestigious scientific journal Advanced Materials.

Microwires made of the semi-conductor silicon are used in numerous fields. It is generally necessary to 'functionalize' them, by adding a layer of metal or a layer of a catalyst. In most cases, the wires are given a single layer, but in specific instances it is useful to put a different material on the bottom and on the top of the wires. However, creating these wires proved very difficult and the process of making them involved many steps. Researchers from the University of Twente have now developed a new method that makes creating wires of this kind easy. According to University of Twente Professor Jurriaan Huskens, this has provided chemists with a versatile method for creating new materials.



In their experiments, the University of Twente researchers first made microwires with a PN junction halfway along the wires. In the experiment, the wires were submerged into a solution containing platinum in the dark, causing the 'P side' of the wire to be covered in platinum. In the next stage, silver was added to the other side in the light. The result was a microwire with silver on the top and platinum on the bottom. The wires can be very valuable for the purpose of generating energy from sunlight or purifying water with the help of sunlight.

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Systematic Estimation of Worst-Case PDN Noise: Target Impedance and Rogue Waves

by Istvan Novak
ORACLE

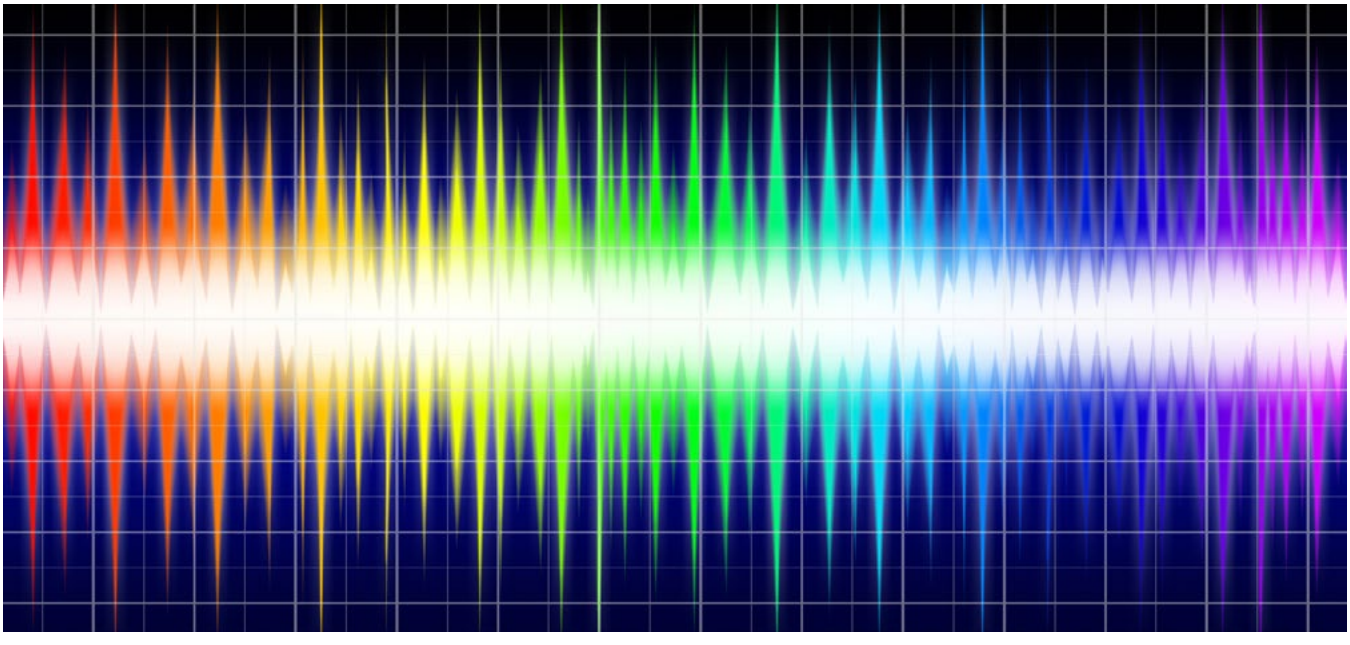
In the dark ages of power distribution design, the typical advice was to use a bulk capacitor and one 0.1uF bypass capacitor for every power pin on the digital circuit. This was very unscientific, but served the industry reasonably well in low-density and low-speed circuits. As the designs got more demanding, the target impedance concept was developed [1]. Using a target impedance, designers had a metric and a design goal to guarantee that the voltage transients stay within specified limits.

Strictly speaking, the target-impedance concept is valid only for flat self-impedance profiles; however, most of our practical designs do not have that luxury. With non-flat impedance profiles, the noise is different. Surprisingly and counterintuitively, keeping the same maximum impedance, the more we deviate from the flat impedance by pushing the impedance down in certain frequency ranges, the higher the worst-case transient noise becomes. This raises the question how to do a systematic design and also gives rise to speculations about rogue waves [2]. But there is a systematic, fast and efficient way of calculating the worst-case noise for any arbitrary impedance profile.

The target impedance concept assumes that the power distribution network is hit by a series of current steps, each current step having a magnitude of DI and fastest transition time of t_{tr}. If up to the BW bandwidth of the excitation the PDN impedance is Z_{target}, the resulting voltage transients are within the DV limits.

$$BW = \frac{1}{\pi\, t_{tr}}$$

$$Z_{target} = \frac{\Delta V}{\Delta I}$$



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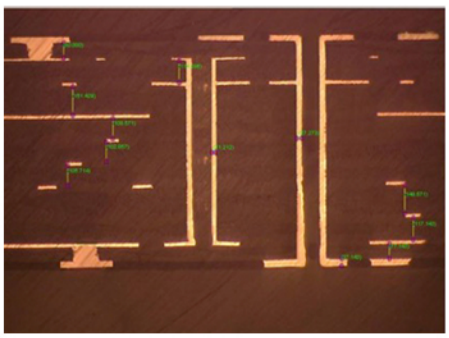
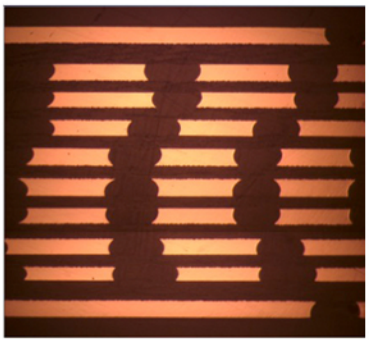
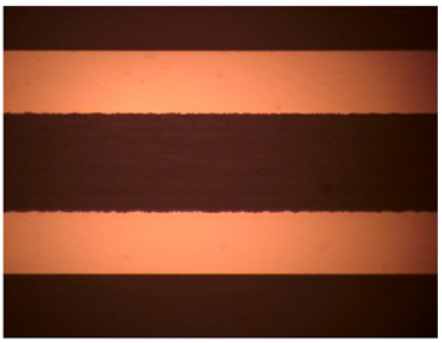


Via in Pad Technology (Micro-via)



10 Layers: 140µm copper finished in each layer (4oz cu) with Buried via (L2- L9) and PTH (L1- L10)



2 Layers: 525µm copper finished in each layer (15oz cu)

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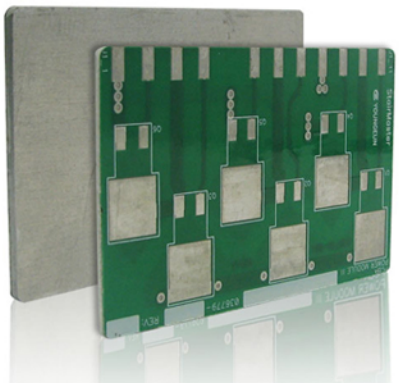

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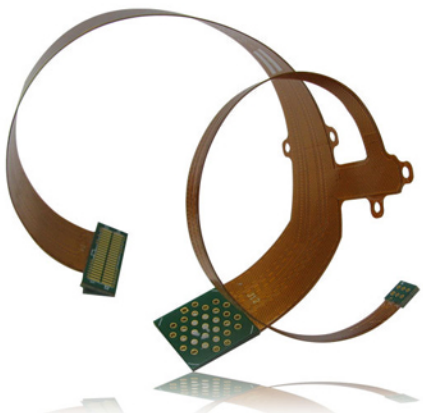

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SYSTEMATIC ESTIMATION OF WORST-CASE PDN NOISE

The target-impedance concept and these expressions assume a linear and time-invariant (LTI) PDN; moreover, assume that the PDN impedance is flat, frequency independent, from DC up to the BW bandwidth of the excitation.

Interestingly, if the impedance profile is not flat, but still stays at or below the Z_{target} limit, the worst-case transient noise gets bigger. For some of the typical PDN impedance profiles, this was shown here [3]. When the impedance profile is not flat and the worst-case transient noise is different from what we can expect from the target impedance formula, we need to determine what the excitation pattern that yields worst-case noise is and what its value is. Recently modified target impedance approaches have been proposed (for instance [4]), or as I have written [3], a conservative correction factor can be used based on the degree of non-flatness of the impedance synthesis method. Using a conservative correction factor from the beginning makes it possible to follow a straightforward design process without the need of iterations.

For LTI PDNs with flat or any non-flat impedance, a process called reverse pulse technique was published in 2002 [5]. Without the need of an optimization loop it provides a guaranteed way to determine the absolute worst-case transient noise and its corresponding excitation pattern, what we still may call rogue wave. To illustrate the power and usefulness of the process, we take the rogue-wave example circuit in [2] and calculate the worst-case noise with the reverse pulse technique.

Figure 1 shows the schematics from [2], redrawn in a free circuit simulator [6]. Note that this particular simulator has the capability to represent a full RLC model of a single component, but for sake of clarity the schematic shown here explicitly calls out all parasitic elements and their own parasitics are set to zero. For example, component L_2, having an inductance value of 2nH, has no series resistance or parallel capacitance. The series resistance of L_2 is separately called out by R_2 with 2mOhm value.

We can run an AC simulation on this circuit to find out its impedance. For this purpose we run an AC sweep of the I_1 current source with a current magnitude of 1A. The V_2 voltage source with a voltage of zero is included only for convenience so that we can also plot the current

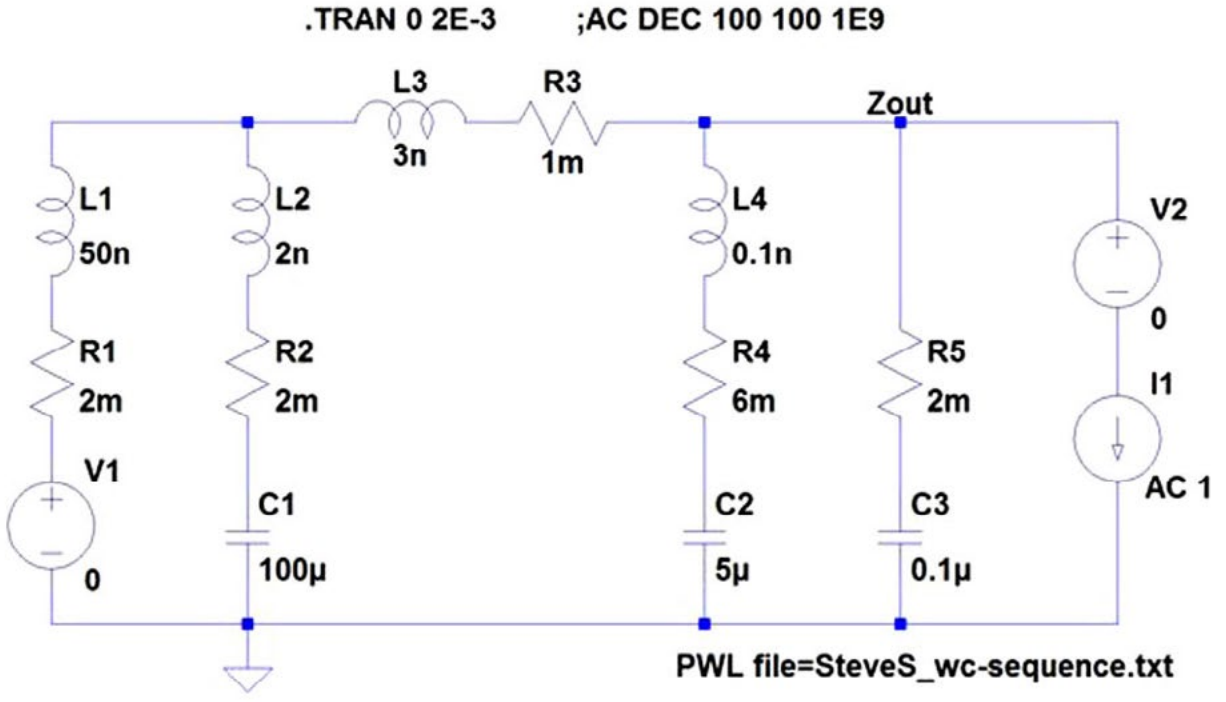

Figure 1: Rogue-wave example circuit from Steve Sandler's DesignCon 2015 paper [2].

going through our circuit. The voltage as a result of the 1A swept-frequency sine-wave excitation gives us the complex impedance. Figure 2 shows the impedance magnitude and phase at node Z_{out} in the frequency range of 100Hz and 1GHz. The sweep was logarithmic with 100 frequency points per decade.

The impedance profile shows three peaks with almost the same peak value, all slightly above 100 mOhm. The series loss values are very low, 1–6 mOhm, resulting in deep valleys in between the impedance peaks. The antiresonance frequencies spread across almost three decades of frequencies. While this impedance profile would be very rare in practice, and would most likely be the result of either careless design or lack of any systematic design whatsoever, we cannot rule out either the possibility that this could represent an actual circuit. Making use of the three distinct peaks separated by deep valleys, Sandler uses a semi-heuristic approach to find what is called a rogue wave: it defines three repetitive bursts hitting the peak impedances one after the other, leaving the timing adjustment to an optimizer to find the biggest noise.

The result is 750 mVpp for a series of 2A current step, which is equivalent to 375 mVpp/A. Compared to a perfectly flat impedance profile matching the largest peak, 126 mOhm, the optimization from Sandler's paper predicts a worst case of almost exactly three times of that value. The question is: is this really the worst case, or is it possible to find a different sequence of current steps that would produce an even bigger transient noise? We can turn to the reverse pulse technique to get the answer.

The reverse pulse technique starts with the step response of the circuit. Since the basic assumption is that the PDN is linear and time invariant (LTI), it does not matter whether we look at the response for a positive or negative going current step excitation; they are mirror images of each other. Figure 3 shows the step response for a positive going current step. Without restricting generality, we assume that the DC voltage on the supply rail is zero and therefore most of the transient response will be neg-

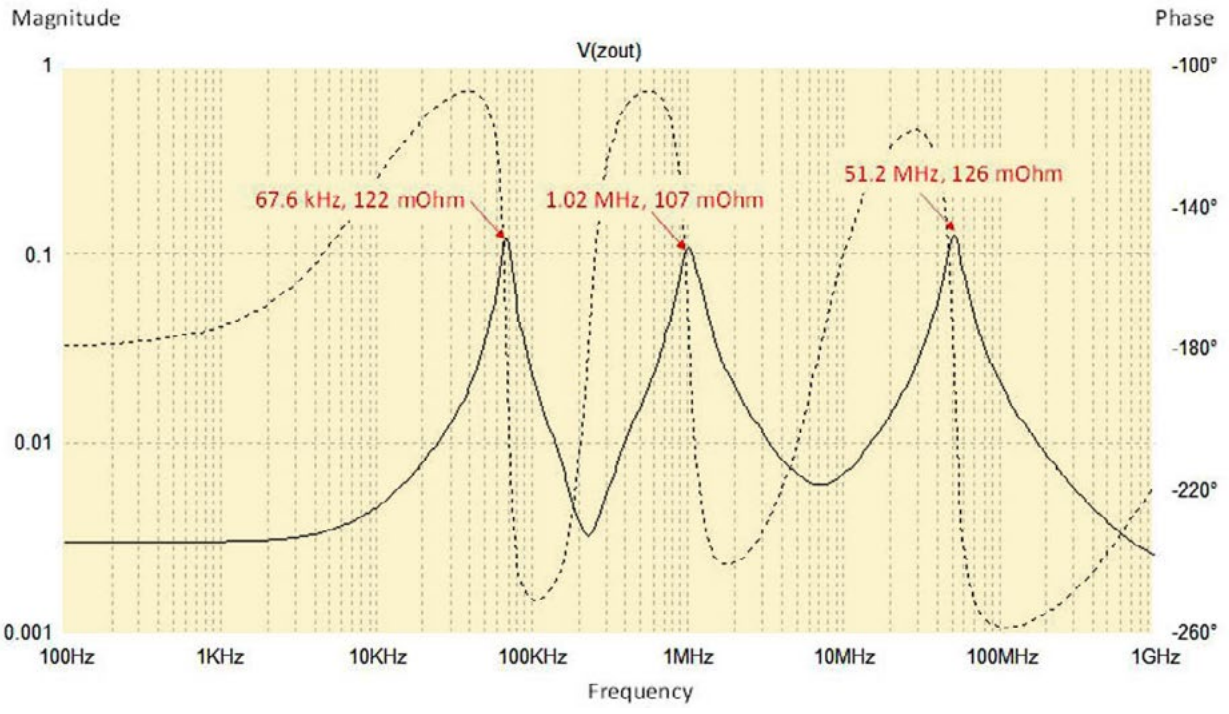

Figure 2: Impedance magnitude and phase from the circuit shown in Figure 1. Note that both axes are logarithmic; in particular, the frequency scale is logarithmic to clearly show the resonance peaks separated by three orders of magnitude.

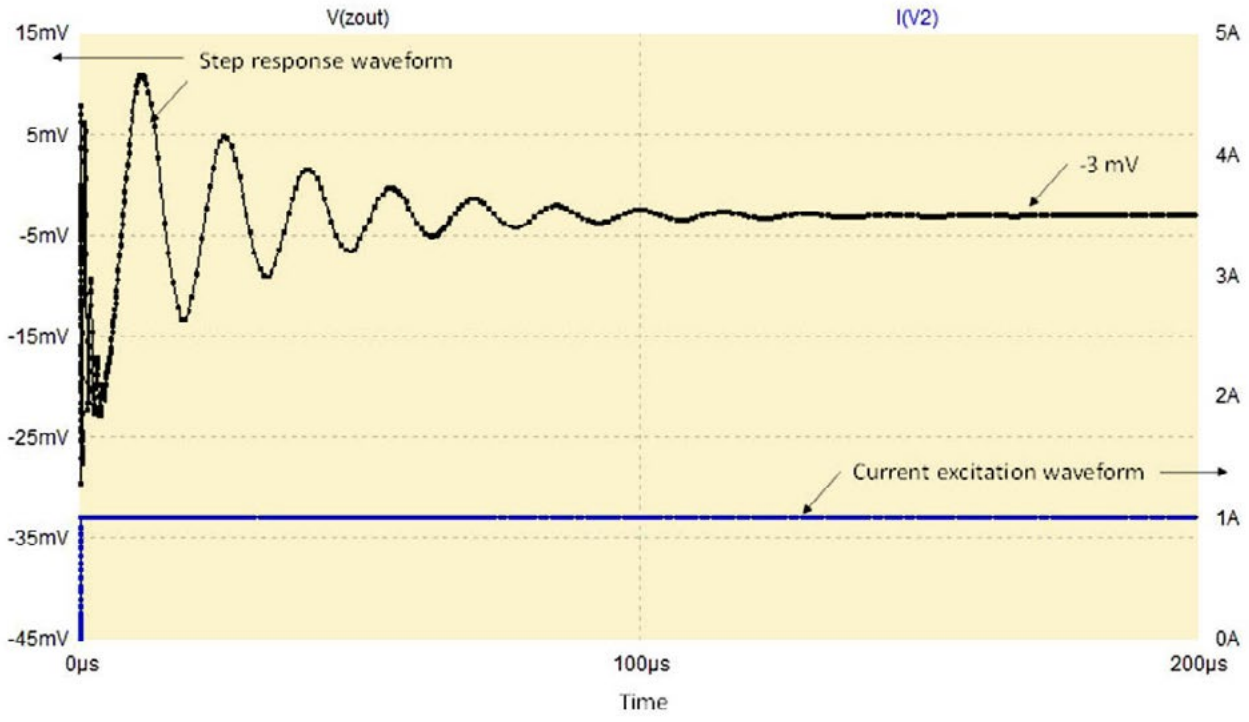

Figure 3: Simulated step response of the circuit shown in Figure 1. Note that both axes are linear, as it would be shown on an oscilloscope or by a default simulation setup. Horizontal axis shows the full 0 to 0.2 µs time interval.

ative. Because of the LTI assumption, any DC voltage on the rail can be taken into account as a simple shift.

The excitation current is a single current step, stepping up from zero to one ampere with 1 ns rise time. Note that the 1 ns rise time corresponds to about 300 MHz excitation bandwidth, where the impedance profile has a capacitive downslope and therefore the actual rise or fall time of the excitation is less critical.

The step response is shown up to 200 µs, where it settles out to a -3 mV DC value. This is the result of the series equivalent of R_1 and R_3. The main signature we see on this scale is a damped sinusoid ringing with approximately 15 µs period; this corresponds to the 67.6 kHz lowest-frequency peak in the impedance profile. We see more rapid changes near the left vertical axis, but we don't see any details. To see more details of the faster transients, we need to change the time scale.

Figure 4 shows the result. It is the same data, except now we show only the first ten microsecond time interval. On the right half of the plot the step response has a smooth rise; this is the beginning of the 67 kHz ringing. The left half of the response has a damped sinusoidal ringing with approximately 1 µs period; this is originated from the 1.02 MHz impedance peak. We see some further fast transients near the left vertical axis, but on this horizontal scale we still can't see the details. We have to make another adjustment to the horizontal scale to see those details as well.

In Figure 5 we further zoom into the waveform and show only the first one microsecond interval. From 0.1 to 1 µs we see a slow sine wave in the response; this is the 1MHz damped sinusoid. Near the left vertical axis now we see another damped sinusoidal waveform with approximately 20 ns period; this comes from the 51 MHz peak.

To see all signatures on the same plot, we need to switch to logarithmic horizontal axis, as shown in Figure 6. The logarithmic time axis, just like the logarithmic frequency axis

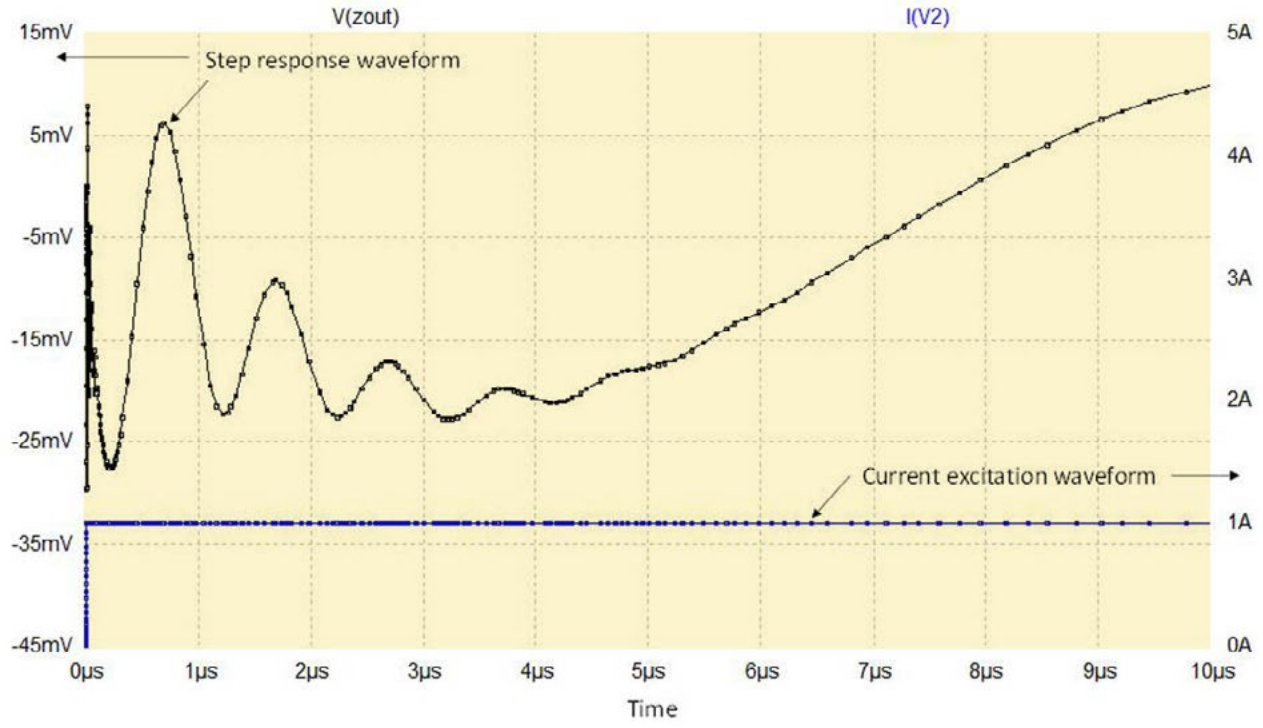

Figure 4: Simulated step response of the circuit shown in Figure 1. Both axes are linear. The horizontal axis shows the first 0 to 10 µs time interval.

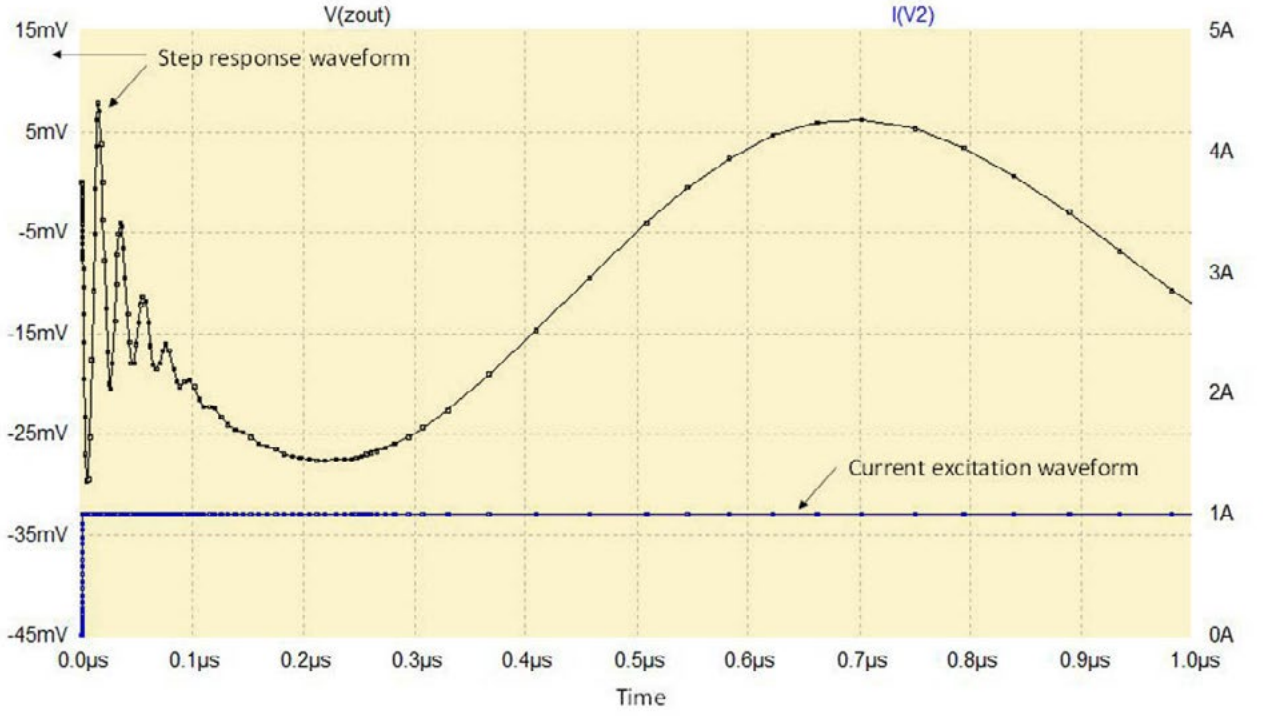

Figure 5: Simulated step response of the circuit shown in Figure 1. Both axes are linear. The horizontal axis shows the first 0 to 1 µs time interval.

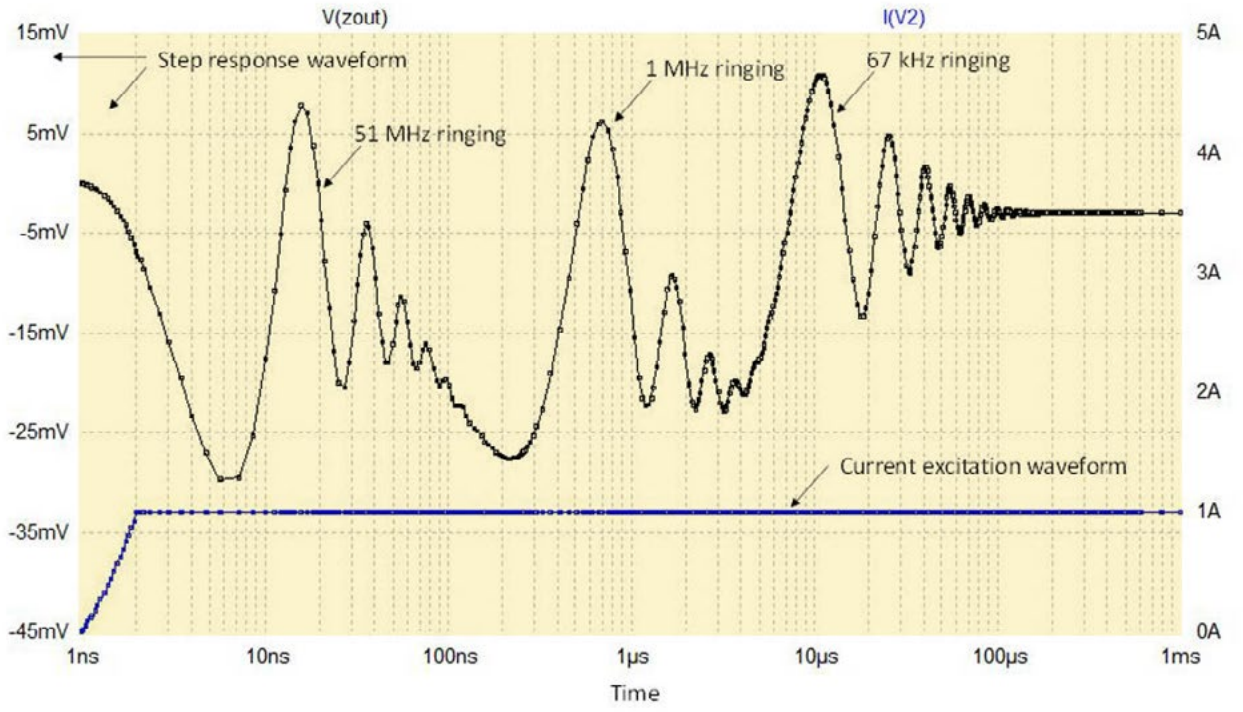

Figure 6: Simulated step response of the circuit shown in Figure 1. Vertical axis is linear; the horizontal axis is logarithmic.

on the impedance plot, allows us to see very different signatures on the same plot. We now clearly see side by side all three damped sinusoid responses.

With the step response data in Figures 3 through 6 we can continue the process of the reverse pulse technique. (Note that Figures 3–6 show the same exact data only in different forms.) Next, we have to identify the steady state and the peaks and valleys in the step response. We have to do it in reverse order, starting with the right-most first extremum (peak or valley) and step through the peaks and valleys one by one from right to left until we reach the excitation time instance. Figure 7 shows the time stamps and voltage values of the peaks and valleys identified in the step response. Note that in simulated waveforms, like in this case, identifying the peaks and valleys automatically is relatively easy; it would become more difficult when we need to process step response waveforms obtained by measurements. The measurement noise makes the peak/valley identification a little trickier.

With the data points in Figure 7 we can continue in two different ways. If we do not need to identify the pattern of the rogue wave excitation and we need only the worst-case transient noise magnitude, we just need to sum up the peaks and valleys and take the difference. The sum of the peaks is -78 mV; the sum of the valleys is -275 mV. The difference is -197 mV. The -197 mV value is the absolute worst-case one-sided noise when an arbitrary sequence of 1A current steps hits the PDN. The worst-case two-sided transient noise is twice of this value minus the DC steady-state value (-3 mV in this case). These numbers give us 391 mVpp worst-case transient noise. The other possible way of continuing with the data points from Figure 7 is to determine the time-domain sequence of excitation edges creating the worst-case noise (the rogue wave) and to actually simulate the time-domain noise.

With the timing sequence from Figure 7, Figure 8 shows the simulated waveforms on logarithmic horizontal scale. The blue wave-

Time [ns]	Peak [mV]	Valley [mV]
137012.9		-3.1
129952.8	-2.8	
122328.4		-3.2
116025.0	-2.7	
107579.3		-3.4
99748.4	-2.5	
92487.5		-3.7
85109.5	-2.1	
77730.4		-4.2
69926.0	-1.4	
62905.3		-5.1
55320.8	-0.3	
47920.9		-6.5
40274.7	1.6	
33340.8		-9.0
25591.5	4.9	
18351.7		-13.3
10894.3	10.8	
4172.1		-21.2

Time [ns]	Peak [mV]	Valley [mV]
3724.9	-19.8	
3226.7		-22.8
2691.4	-17.2	
2262.0		-22.5
1697.3	-9.3	
1226.4		-22.2
701.0	6.2	
217.3		-27.6
97.5	-19.7	
89.7		-20.3
76.6	-16.2	
67.8		-18.6
56.2	-11.4	
47.6		-18.0
36.0	-4.1	
27.0		-20.4
15.9	7.9	
6.3		-29.6

Figure 7: Peak and valley time stamps and voltages identified in the step response of the circuit shown in Figure 1.

form on the bottom is the excitation waveform; the black waveform on the top is the transient response. The peak-to-peak transient value is 391 mVpp, exactly matching the value that we calculated just from the peaks and valleys of the step response. Note that to achieve the worst-case transient noise, we used 37 current steps and their spacing does not exactly follow the three resonance frequencies. This straightforward process yields the worst-case noise very fast, without the need of an optimization loop and it guarantees to provide the worst-case noise. In this particular example the true worst-case noise is 391 mVpp/A as opposed to the 375 mVpp/A predicted by the rogue-wave optimization from [2].

We can also look at the transient noise by another popular test method: using a repetitive stream of current steps with 1A magnitude and tune the repetition frequency (and possibly also the duty cycle) until we observe the maximum noise. We just change the definition of the I_1 current source to a stepped-frequency square-wave and run the simulations again. As we change the repetition frequency, we find that we get the maximum noise magnitude when the repetition frequency matches one of the peak frequencies. Figure 9 shows the result when we

SYSTEMATIC ESTIMATION OF WORST-CASE PDN NOISE

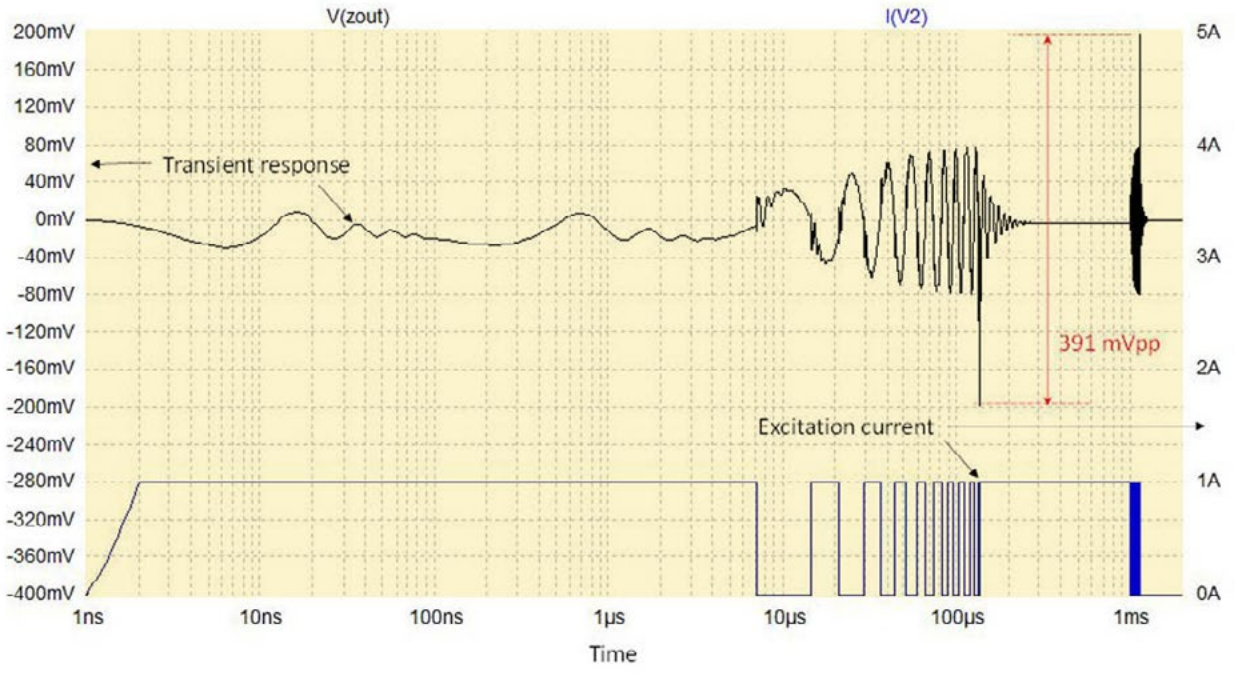

Figure 8: Worst-case response simulated with an excitation sequence calculated from the reverse pulse technique.

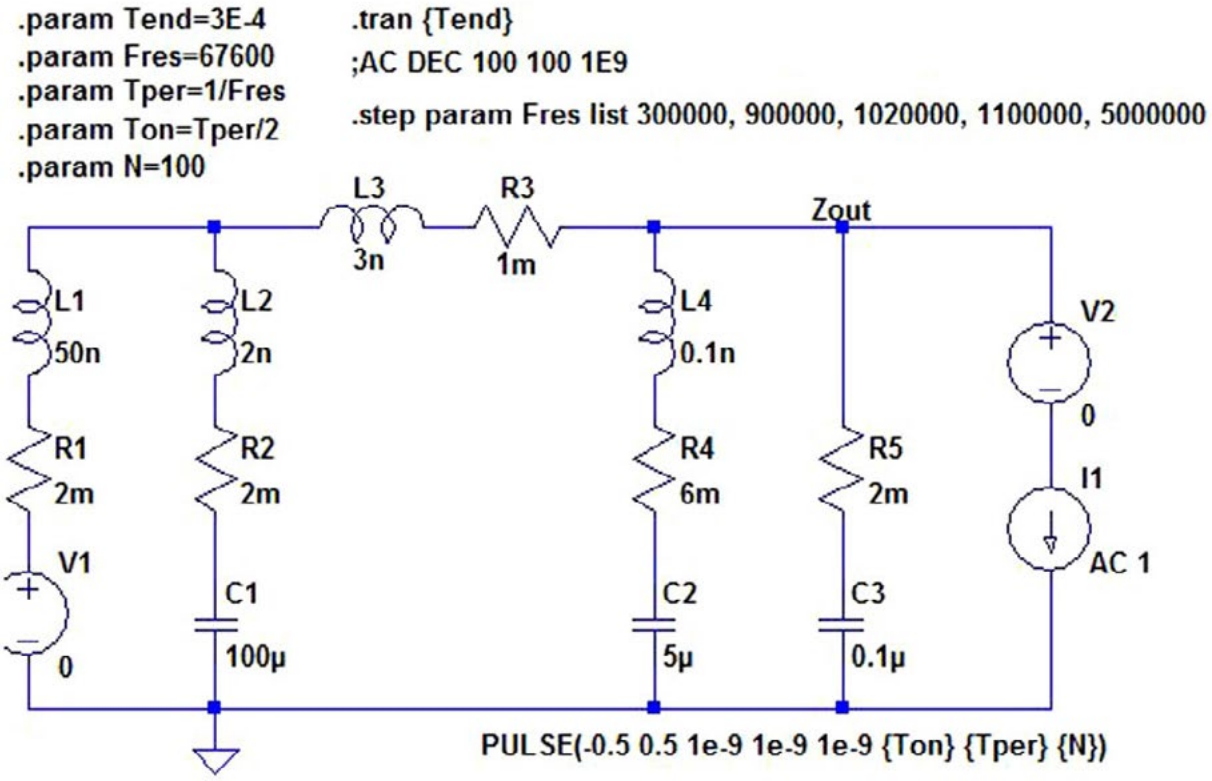

Figure 9a: Schematics with the excitation definitions.

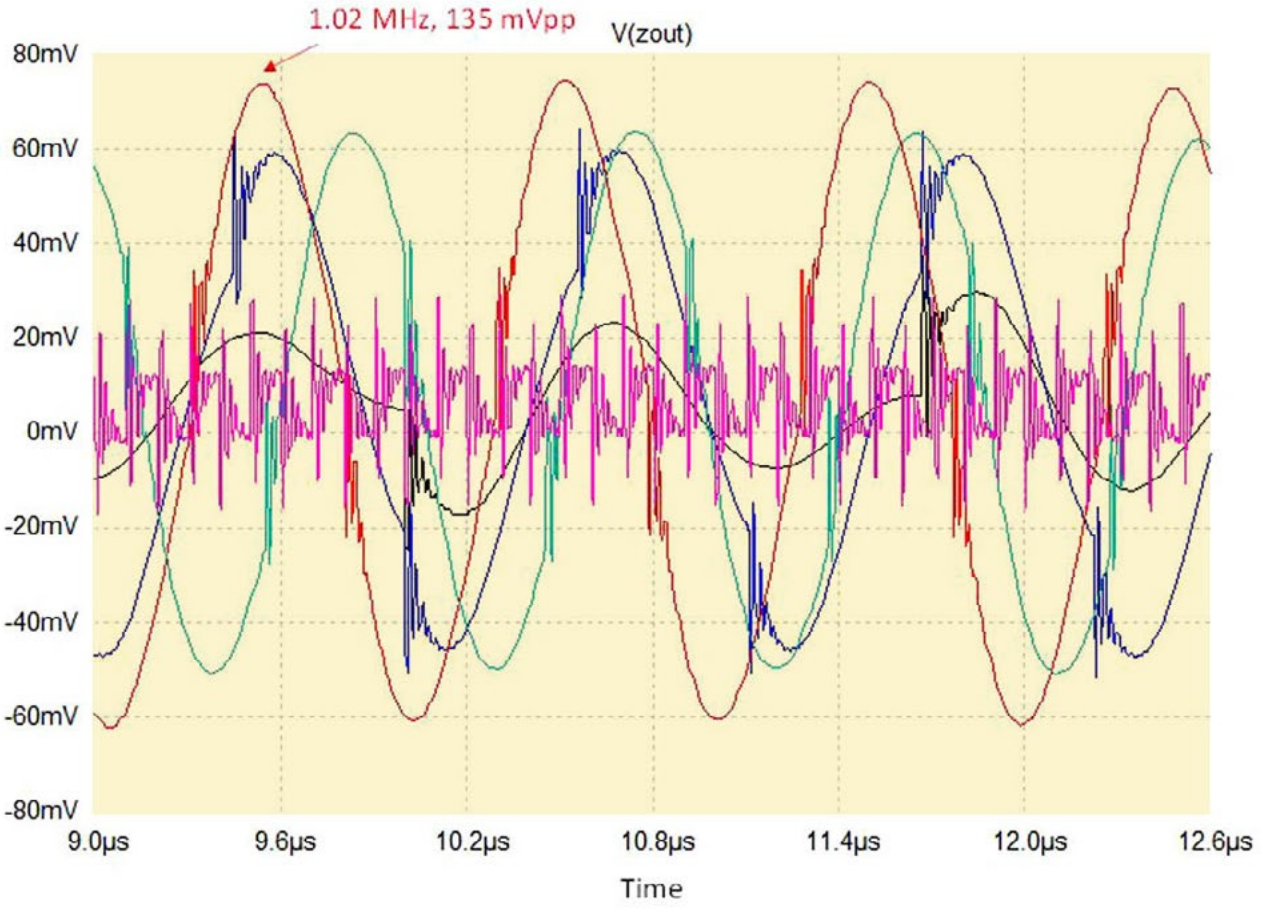

Figure 9b: Response waveforms. Note that the square-wave excitation frequencies map out the middle resonance. The biggest response comes from the 1020 kHz square wave, matching the middle resonance frequency in the impedance profile.

move the frequency around the middle peak in five values: 300 kHz, 900 kHz, 1020 kHz, 1100 kHz and 5000 kHz.

Figure 10 shows the schematics and waveforms for the three repetition frequencies exactly matching the three peak frequencies. We see that in this case the transient noise is higher, actually 4/p times higher, than the product of the impedance peak magnitude and current magnitude. This is because the high-Q peak picks out the fundamental harmonic and greatly attenuates the harmonics. In the Fourier series of a square wave with 50% duty cycle, the fundamental-frequency sine wave has a 4/p times higher magnitude than that of the square wave.

Finally the table in Figure 11 summarizes the characteristic noise signature numbers we obtained. Note that the reverse pulse technique yielded the highest noise, and it is proven to be the absolute worst case. It is also true that the rogue-wave optimization could provide the same (correct) answer, however, in a multi-resonance case like this example, without operator guidance it could take a lot of computing resources and eventually it may not converge.

The first entry in the table is calculated as twice the peak deviation of the step response (from the last row in Figure 7) minus the steady state response. This is the peak-to-peak noise as a result of a single rising edge followed by a single falling edge with a large time separation in between. This estimate is 85.7% smaller than the true maximum. The second entry equals the biggest peak in Figure

SYSTEMATIC ESTIMATION OF WORST-CASE PDN NOISE

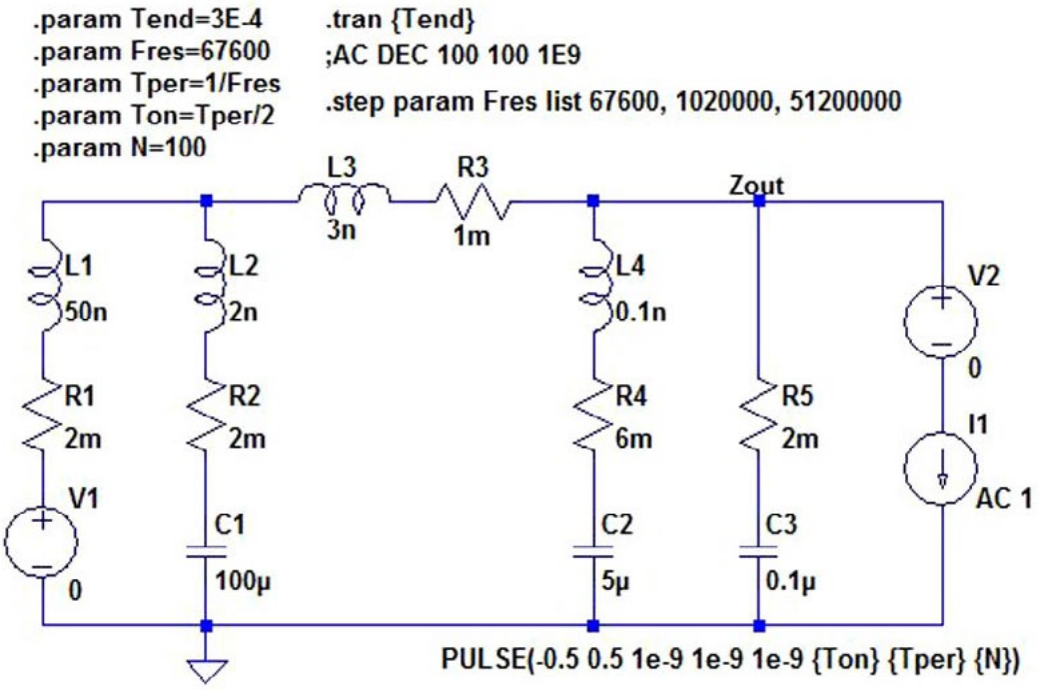

Figure 10a: Schematics with the excitation definitions.

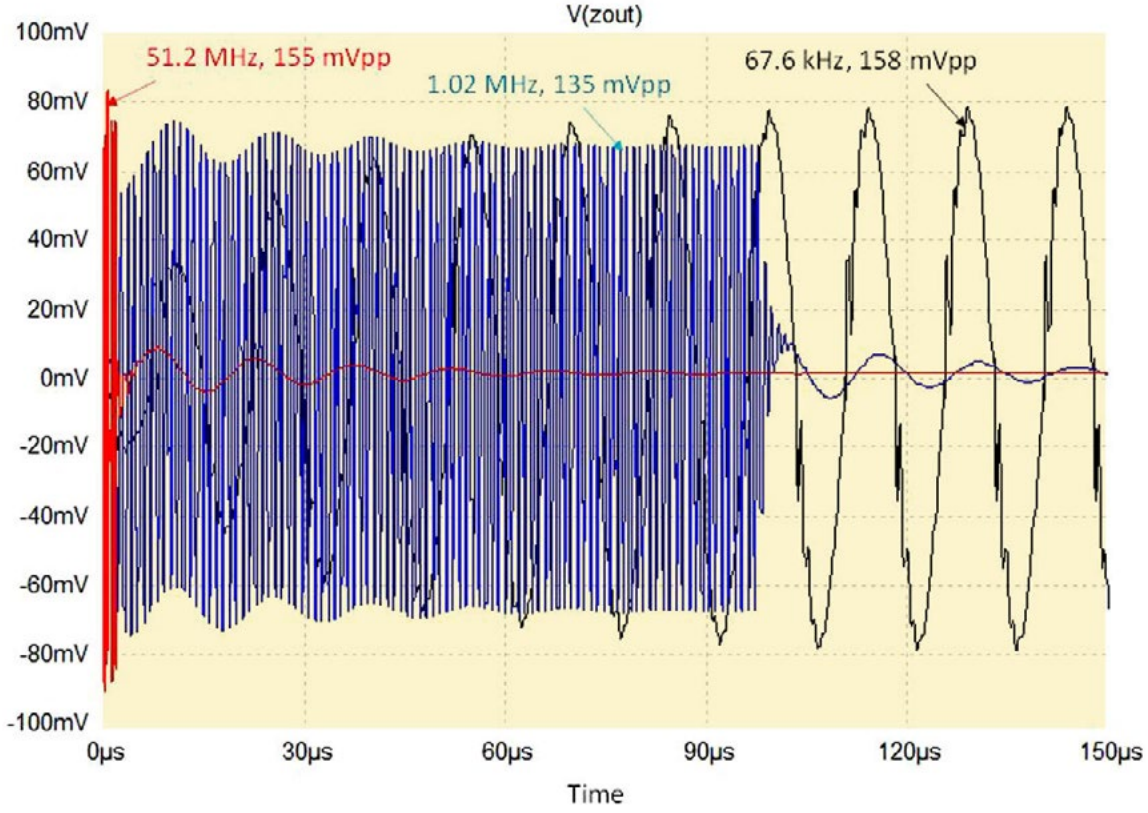

Figure 10b: Response waveforms. Note that the square-wave excitation frequencies exactly match the three resonances.

Worst-case transient noise estimate calculated from:	Peak-to-peak mV	% error
Step Response peak value and steady state	56.2	-85.7
Swept-frequency periodic pulse stream	158	-59.6
Rouge wave optimization	375	-4.1
Reverse Pulse Technique	391	0

Figure 11: Worst-case transient noise estimates of the circuit in Figure 1 based on different calculation methods. All responses assume a sequence of 1A current steps.

2 (126 mOhm at 51.2 MHz) multiplied by 4/p. This is the result of sweeping a periodical current pulse stream to find the maximum noise deviation. This estimate is 59.6% lower than the true worst case. The rogue-wave optimized value is taken from [2]. It is 4.1% lower than the true worst case.

In this particular example, when the impedance profile has multiple, almost equal peaks, the difference is dramatic. Estimating the worst-case noise just from the peak deviation or from swept-frequency periodic excitation hugely under-estimates the worst-case noise. The rogue-wave optimization, in theory, should be able to find the true worst case, but at a price of significant run time and potential convergence failures. With a more flat impedance profile, with fewer peaks and smaller peak-valley ratio, the errors in all of the approximations would be lower. Eventually for a perfectly flat impedance profile all four calculation methods would provide the same result.

If you want to learn more about the subject, follow [7] and [8] at DesignCon 2016. **PCBDESIGN**

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Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To read past columns, or to contact Novak, click here.

Why Do Different Test Methods Yield Different Electrical Values?

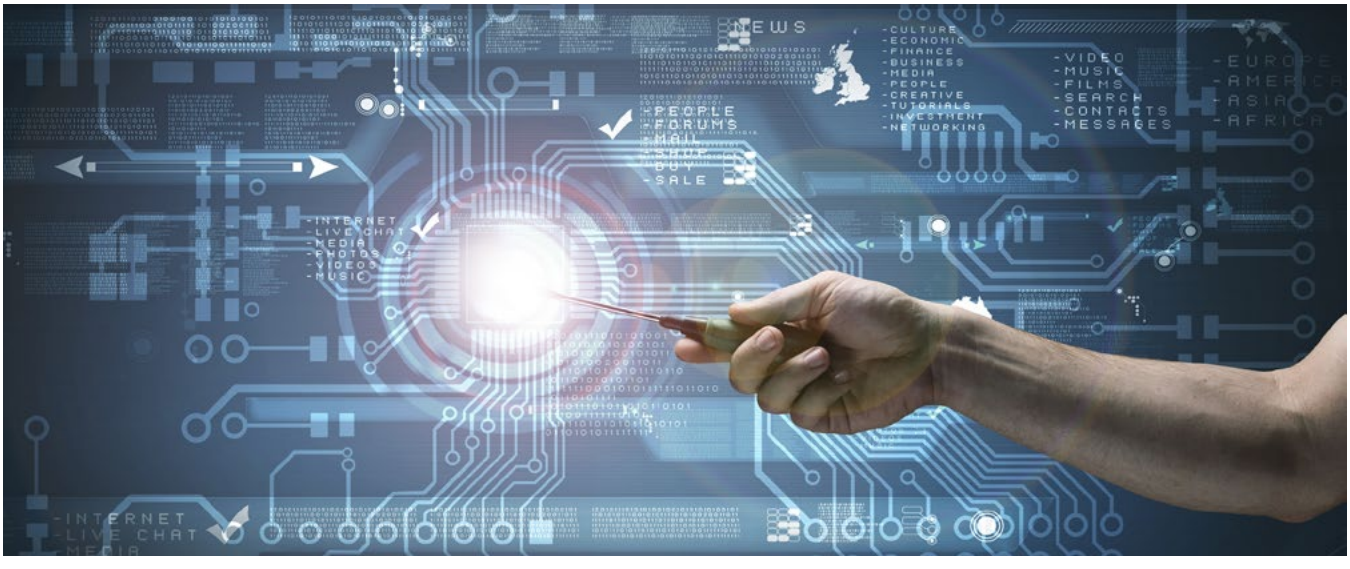
by John Coonrod
ROGERS CORPORATION

A variety of different test methods may be used for any one electrical concern. This article will discuss the issues related to determining the dielectric constant (Dk) and dissipation factor (Df or Tan-Delta). On a data sheet, a designer may see a Dk value for a material to be 3.5, as an example. Once the designer buys the material and performs necessary evaluations, it may be found that the Dk of the material is 3.8. In some applications this difference in Dk is probably not meaningful; however, for many RF and high-speed digital applications, this difference could be very significant. What is really interesting about this example is that the two Dk values may both be correct, depending on the test methods used.

Most laminates used in the PCB industry are anisotropic and this means that the electrical properties are not the same on all three axes of the material. Typically the thickness (z-axis) of the material will have a different Dk value than the x or y axes of the material. The reasons for this depend on what type of material is being considered.

The laminates used in the PCB industry are typically woven-glass reinforced, however there are notable exceptions. The glass reinforcement layer typically has a different Dk and Df than does the raw substrate of the laminate. The standard E-glass most often used in PCB laminates has a typical Dk value of about 6 and a dissipation factor of around 0.004. The common FR-4 laminates use relatively simple resin systems and the resin itself has a Dk that is around 3 and a Df of about 0.03. Different ratios of resin to glass will cause the laminate to have a Dk that is somewhere between the value of the resin and that of the glass. However, the glass-resin ratio impact on Dk is usually considered when evaluating the material through the thickness axis and if the x- or y-axis is evaluated, the Dk value may be very different than the z-axis result.

A large number of test methods are available to evaluate materials for Dk and Df. The methods that are most often used in the PCB laminate industry for making these measurements are typically tailored to evaluating materials in very large volume. Because of this issue,



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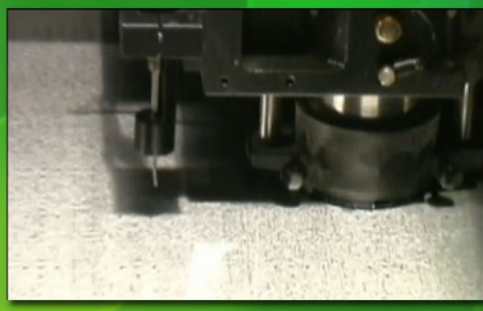

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WHY DO DIFFERENT TEST METHODS YIELD DIFFERENT ELECTRICAL VALUES?

these test methods need to determine Dk and Df relatively fast, have good repeatability, and be used for quality control. A common test method used is the clamped stripline resonator, where a clamping fixture is used to form a stripline structure; the layer structure of a stripline is ground-signal-ground. This test method determines the Dk and Df of the material in the clamped fixture and more specifically, it is reporting these values related to the thickness axis of the material.

Other tests used in high-volume testing include SPDR (split-post dielectric resonator), rectangular cavity and open cavity resonance methods. All three of these methods have electric fields oriented perpendicular to the material, which means these test methods will evaluate the x-y plane of the material and not the z-axis. In the case of the common FR-4 material which is a resin-glass composite, the Dk number can be very different in the x-y plane than in the z-axis due to the impact of the glass.

Returning to the original example, where a material is tested and found to have a Dk of 3.5 and then another test is done on the same material and the Dk is found to be 3.8, both of these numbers can be correct when using two different test methods. These numbers are actually based on real life experience when testing high frequency laminates that are PTFE based with ceramic filler and have woven-glass reinforcement. With this type of material it is possible to have the same piece of material tested in the clamped stripline test and get a value of 3.5 and then tested in SPDR and obtain a result of 3.8. Since the clamped stripline test is evaluating the z-axis of the material and the SPDR is evaluating the x-y plane of the material, both results are obviously different but still correct. Essentially these measurements show to some degree how anisotropic the material is, where the z-axis Dk of the material is 3.5 and the x-y plane Dk of the material is 3.8.

Knowing the anisotropic Dk values of a laminate is typically critical for RF applications with edge coupled features. In the case of high-speed digital circuits, these values can be important for differential pair structures. Having these values can be important, but also having a modeling software which can incorporate these values into predicted circuit performance is an important supplement to the design process.

It is always recommended to contact your material supplier if you have questions about the Dk or Df of a laminate. You should ask which test method is used and which axis or axes of the material is being evaluated. Another good question to ask your material supplier is the frequency at which these values are generated, because the Dk and Df of a material is frequency dependent. Having the most accurate laminate information for the design phase of a project is critical to its success. **PCBDESIGN**

John Coonrod is a senior market development engineer for Rogers Corporation. To read past columns, or to reach Coonrod, click here.

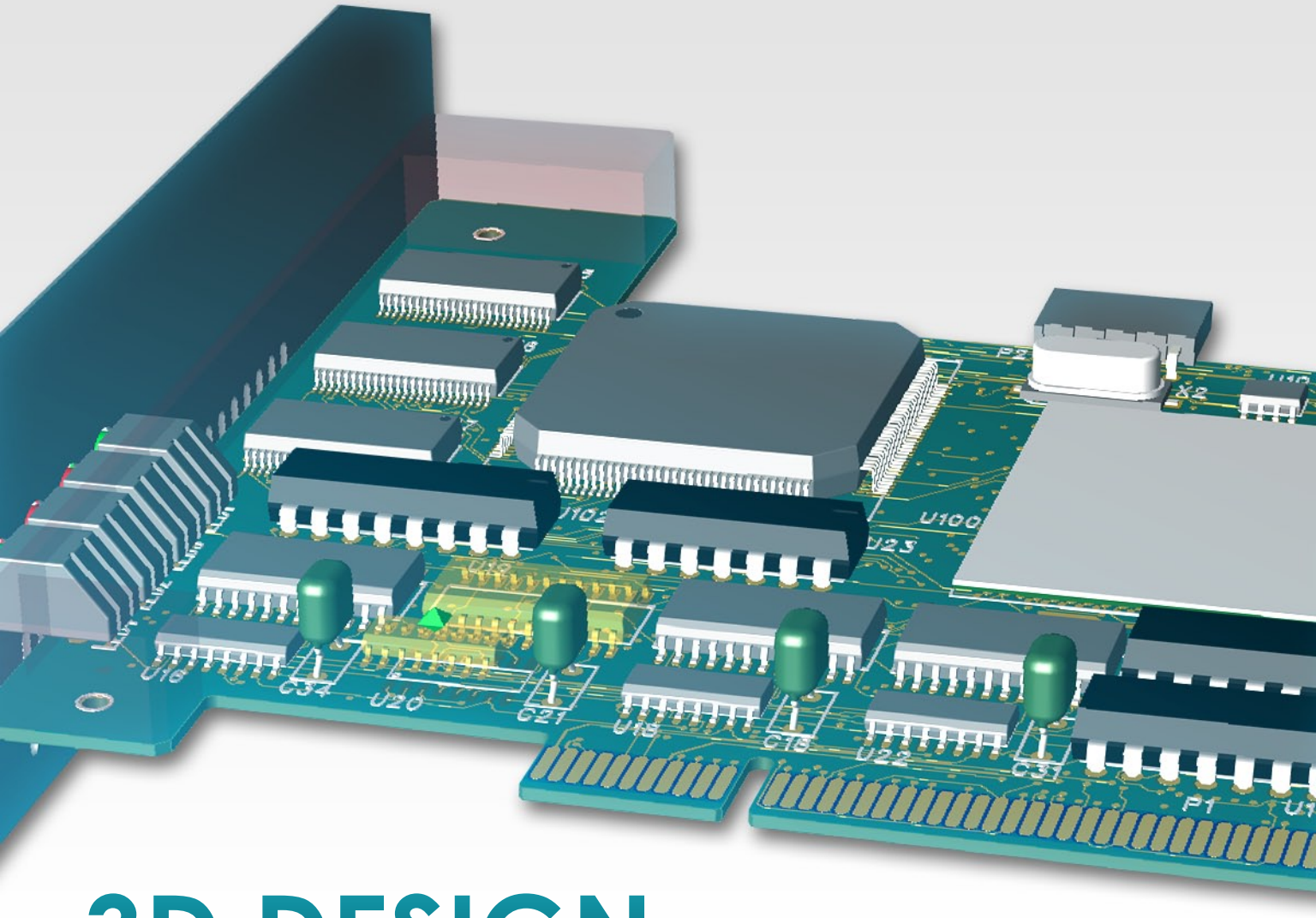
New Nanomanufacturing Technique Advances Imaging, Biosensing Technology

More than a decade ago, theorists predicted the possibility of a nanolens. But scientists had been unable to build and arrange many nanolenses over a large area.

"That's where we came in," said Xiaoying Liu, senior research scientist at the University of Chicago's Institute for Molecular Engineering.

They aligned three spherical gold nanoparticles of graduated sizes in the string-of-pearls arrangement predicted to produce the focusing effect.

The scientists are already exploring using this "hot spot" for high-resolution sensing using spectroscopy. "If you put a molecule there, it will interact with the focused light," said Liu.



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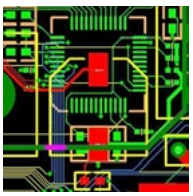
2015's Most-Read ARTICLES

VERY INTERESTING...

EchoStar's Les Beller Shares the PCB Design-to-Fab Process

Recently, Barry Matties had the opportunity to meet and interview Les Beller of EchoStar Technologies. In this interview, Beller focuses on the many challenges circuit board designers face, strategies for bridging the gap between circuit design and fabrication, and the future of circuit designers.

Beyond Design: The Plain Truth About Plane Jumpers



Moats, islands, cut-outs in the ground plane, isolated power planes, floating ground regions, and a host of other intricate layout techniques are often used by PCB designers to reduce crosstalk, EMI, and to otherwise improve overall system performance. But a high-speed signal crossing a split in the plane causes problems along at least three dimensions, including signal quality, crosstalk, and EMI. Barry Olney explains.

Cadence's Brad Griffin Digs Deep Into DDR

Guest Editor Kelly Dack stopped by the Cadence Design Systems booth at DesignCon 2015, where he sat down with Product Marketing Manager Brad Griffin to discuss Cadence's advanced PCB design and signal integrity tools, and the company's focus on DDR.

Trending at Freedom CAD: New Crop of Next-Gen Designers

Scott McCurdy, director of sales and marketing at Freedom CAD Services, expresses his vision for what North America is bringing to the table in the world of circuit design. I-Connect007 Publisher Barry Matties and McCurdy also discuss China, trends in product design, tools, and more.

Material Witness: Low-Flow Prepregs—Defining the Process

Let's try to define "low flow" in terms that will make sense to both suppliers and users of the products. A low-flow prepreg is a prepreg that flows sufficiently to wet out and adhere to bonding surfaces and to fill inner layer copper details, but does not flow so much as to fill in cut-out areas in a heat sink or run unevenly out of the interface between rigid and flexible elements of a rigid-flex PWB.

Make the Right Decisions at the Right Time in the PCB Design Process

Martin Cotton of Ventec explains why the right decisions are not always the easiest decisions, but making them well and as early as possible often avoids errors and addition costs. This is certainly the case in PCB design and a key decision influencing the design process and the eventual outcome is the selection of material and of the materials vendor.

Nick Barbin: From Designer to EMS Company Owner

Many PCB designers would rather do just about anything than pore over a P&L spreadsheet. But Nick Barbin isn't a typical designer. He co-founded the design bureau Optimum Design Associates over two decades ago, and the company later expanded into contract manufacturing and Lean processes. I caught up with Nick recently and asked him how he wound up leading an EMS company on the Inc. 5000 list.

Broadcom PCB Design: Miniaturization on the Cutting Edge

Andy Shaughnessy recently attended the Orange County Designer's Council "Lunch and Learn" meeting, held at the Broadcom offices on the campus of the University of California, Irvine. Afterward, he sat down with Scott Davis, CID, the senior manager of PC board design at Broadcom, to discuss the company's savvy PCB design department and their approach to PCB design.

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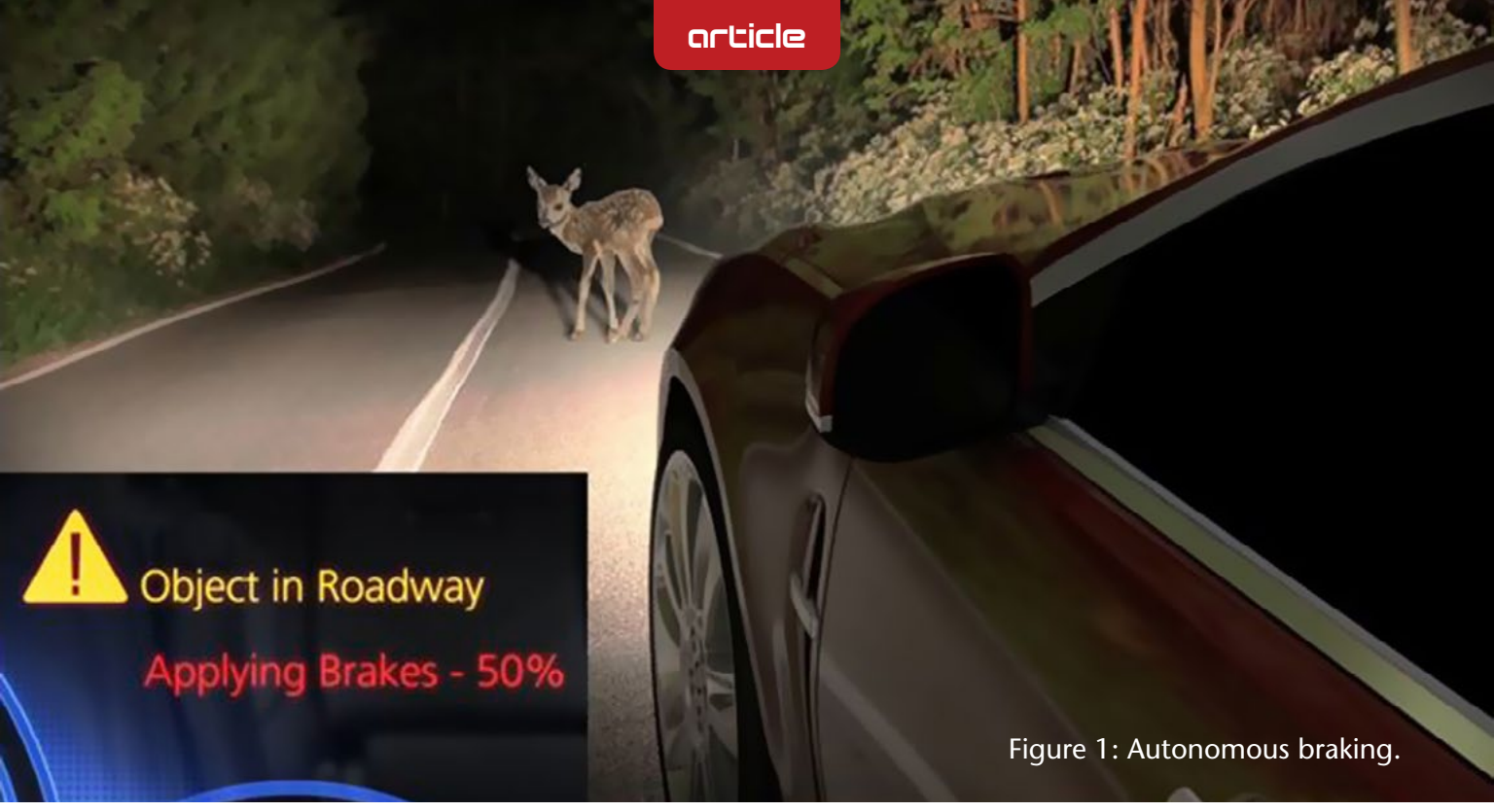

Figure 1: Autonomous braking.

Electrical Design Challenges for Automotive PCBs

by Brad Brim
CADENCE DESIGN SYSTEMS

The automotive world is changing rapidly and the pace of this change is accelerating. Hardly a day goes by without engineering trade news concerning autonomous driving capabilities or IP core selection for future automotive microcontrollers. Even financial news media regularly cover new companies entering the automotive market, speculating as to what they will bring to this long established industry. The very nature of the automobile is changing as internal combustion propulsion is augmented for hybrid vehicles and completely replaced for all-electric cars.

In past decades, evolutionary changes were common. Drum brakes transitioned to discs. Anti-lock braking has become a standard feature and autonomous braking capabilities for forward and cross-traffic conditions are now available as options, as depicted in Figure 1. AM/FM radios now have added support for CDs, USB drives and Bluetooth, video, and DVDs, becoming complete entertainment systems. The advent of automotive Internet access enables a new class of infotainment capability for both passengers and driver. Revolutionary changes are on the horizon, including autonomous vehicles (no driver), autonomous driving and other advanced driver assistance systems (ADAS) capabilities. Automated braking and other available ADAS capabilities can be viewed as evolutionary changes. But whether evolutionary or revolutionary, these changes in propulsion and all other attributes of the driving experience are enabled by electronic systems where PCBs (and PCB design teams) play a major role.

A recent article in *The PCB Design Magazine* by Monica Andrei of Continental Automotive Systems emphasized the systemic nature of an automobile and discussed the characteristics and adoption of software design tools to enable such system-level design. Recognizing that electrical challenges are part of the automotive system-level discussion, this article will present more detail on signal integrity (SI). Future discussion is planned regarding electromagnet-

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ic interference (EMI), power integrity (PI) and thermal integrity (TI).

The Automotive Electrical System

Figure 2 shows an abstract view of an automotive electrical system with a few of the major subsystems included. A single electronic control unit (ECU) is labeled in the figure. This master ECU is supported hierarchically by ECUs with local control over their respective subsystem components. Past generations of automotive ECUs were typically simple two-layer PCBs, even for the master ECU. PCB physical design (e.g., layout) was accomplished with general drafting tools and SI/PI/TI/EMI simulations were not often required. For modern automotive systems, the lowest-level ECUs still typically have small, two-layer PCBs, but a modern master ECU features a complex, multilayer PCB. Subsystem ECUs might also be quite complex; this is the case for an infotainment system that includes multiple high-definition displays, high-definition audio and broadband Internet connectivity. The main ECU integrated circuit is typically called a microcontroller. It has become a complex, high-pin-count, high-speed, multicore processor and is anything but "micro."

Some automotive electrical systems have grown to have as many as 100 ECUs, which implies a very complex system. There is a trend to reduce this large number of ECUs by a factor of two to three. The trend is toward more complex ECUs at the top of each hierarchical subsystem with smart sensors at the lowest level. This trend implies more complex PCBs for each subsystem high-level ECU and potentially no PCB for some of the local sensors. As automotive system components, the master and high-level subsystem ECUs must be absolutely reliable and low cost. Their PCBs must support higher

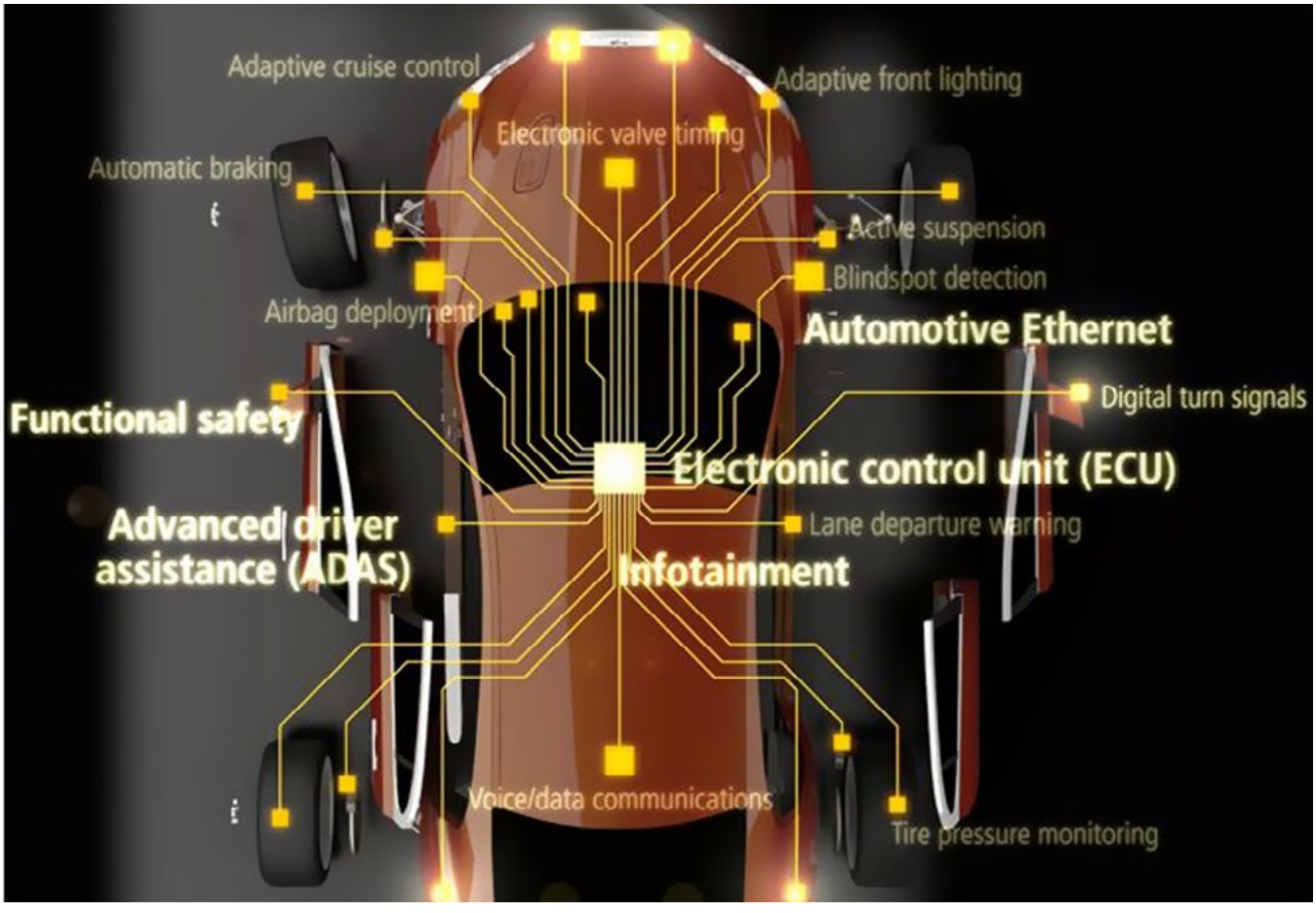

Figure 2: Automotive electrical system.

speed and higher pin-count microcontrollers, greater bandwidth for on-board and off-board data communications, reduced size and weight, and finally accommodate high levels of electromagnetic noise unique to automotive environments. Electrical simulations of system-level SI, PI and EMI effects are now unavoidable for automotive ECU boards.

Though PCB-centric, these system-level simulations involve both on-board and off-board interconnects, including the cable harness and its associated connectors (both inline and to PCB). Two-layer PCBs are inexpensive but not able to support the design complexity and electrical performance required for modern ECUs. Power delivery of multiple voltages with minimal loss and low noise, reduced emissions and lower immunity, as well as controlled impedance interconnect, require multiple plane layers for the power delivery network (PDN) of ECU boards. The on-board interconnect for these multi-layer boards is composed of interlayer vias, microstrip with one PDN plane and stripline with two PDN planes, one above and one below. Off-board high-speed signals are typically serialized (converted from parallel to serial), which reduces cable harness complexity and weight because a single unshielded twisted pair of wires might be applied for cabling.

The system-level simulations must consider the full hierarchy of chip/package/board to properly judge performance as well as represent the actual operating condition of the system. "Bits-to-bits" simulations are performed whether for parallel interconnect between a microcontroller and external memory on the same PCB or for serial interconnect between a transmitter on one ECU board and a receiver on another ECU. Therefore, serial interconnect analyses involve multiple boards as well as the physical signal channel between them.

Signal Integrity

The challenges involved in designing an automotive infotainment subsystem that comprises both in-dash components for the driver and remote components for the passengers, as shown in Figure 3, serve as an excellent exam-

Figure 3: Automotive infotainment system.

ple for system-level SI simulation. The "info" qualifier implies an Internet connection, which might be provided by another subsystem and accessed via a high-speed Ethernet connection or might be implemented by an RF section of the PCB. In either case, it adds significantly to the complexity of the board. The chipset required to decode and process HD video and audio are high-speed, high-pin-count devices, usually requiring a fairly complex board.

On-board memory is required with its associated multibyte parallel bus, thereby indicating the need for controlled impedance and delay-tuned signal routing during physical design as well as timing analysis for performance signoff. The remote passenger displays require a similar level of decoding capability and might be nearly as complex as the in-dash PCB. They also require a high-speed multi-drop interface, such as Ethernet, be available on both the in-dash and remote boards. The design requirements for such systems include complex multi-layer boards and high-speed parallel bus routing, as well as high-speed serial interconnect with multiple boards. Designs must be simulated and analyzed including full serial channel characterization. These challenges for physical design and SI simulation are not unique to automotive applications and are available with enterprise-class PCB physical design software.

> "The chipset required to decode and process HD video and audio are high-speed, high-pin-count devices, usually requiring a fairly complex board."

First consider routing and performance verification of the high-speed memory buses. There are five key aspects of PCB design software for high-speed parallel bus design: (1) constraint-based physical design, (2) automation for bus routing, (3) initial timing enforcement, (4) board-level SI performance assessment and (5) power-aware SI compliance signoff. Constraint-based physical design enables a correct-by-construction flow. Physical as well as electrical constrains are dynamically flagged as routing occurs for instant feedback and on-the-fly correction. The alternative is a much more time-consuming process of iteratively cleaning-up design rule check (DRC) errors after initial PCB routing is completed. Autorouting is critically important and available for individual nets, differential pairs and entire buses. A bit of interactive guidance for the autorouter, a process dubbed "auto-interactive," during device-local breakout routing and bus-level delay tuning greatly speeds these tasks. The electrical parameters of impedance and delay are computed in real time whether routing is performed manually or automatically. These per-net electrical parameters are available to support timing analysis and rapid interactive tuning of the entire bus to comply with standard protocols (e.g., DDR3, DDR4). These tasks are all accomplished by a layout designer before the final completed board design is passed to an SI engineer for performance verification.

PCB design team members first assess the design for operating condition independent characteristics, such as net impedance, coupling among nets and return path discontinuities. The analysis is rapid and very high capacity, enabling the entire board to be considered. The results are available in tables or as color-shaded layout overlays for intuitive assessment. A power-aware analysis (including the effects of the actual current return paths in the PDN) might be performed to narrow down SI issues to individual byte lanes or even a few nets. This rapid assessment applies ideal I/O buffers with piecewise linear signals and examines a small set of SI metrics defined by received signal, far-end crosstalk and intersymbol interference.

SI issues with routing are quickly and reliably identified to be addressed in layout or examined further with more detailed SI simulation. Layout-based detailed simulations of a few nets might be performed relatively quickly to judge performance or validate the performance improvement of design changes. Whole-bus

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compliance-driven SI simulations are performed with protocol-specific system schematics. Broadband power-aware S-parameter models are extracted for the memory bus or byte lanes of interest. Vendor-provided power-aware IBIS models are applied along with 3D extracted package models and used in simulations required for protocol-compliance verification. Simulation results are captured into interactive reports where violations are flagged and waveforms are accessible for each net simulated, enabling issues to be investigated. This signoff-accurate simulation might easily be setup to determine simultaneous switching noise (SSN) effects. For DDR4, this detailed parallel bus analysis might also consider serial channel analysis to determine the requisite bit error rate (BER) compliance checks.

With the mention of serial channel analysis, let's next consider the timely topic of automotive Ethernet in the framework of serial communication between the in-dash ECU and the remote terminals of the infotainment system. Just as memory subsystem design is not unique to automotive applications, serial link design is also common among many high-speed electronics designs. However, unlike memory, automotive serial communications apply unique protocols and physical channel hardware. Each of the system's PCB and physical channel components is designed independently. Vendors provide cables and connectors to form the physical channel and commercially available chipsets are applied, which are likely to use third-party IP blocks. These chipsets and IP blocks might seem to simplify the PCB design process for serial links, but in reality, it is more complex. Design performance must be verified through characterization of the full system, from serialized digital output from the transmitter (TX) to serialized digital input to the receiver (RX). As for memory subsystems, a few nets might be characterized with layout-centric simulation, but these results are not the desired performance and system-level block schematic simulations are a requirement.

Presently available capabilities supported by automotive Ethernet include infotainment systems, sensors and backup cameras. A new IEEE standard, 100BASE-T1, defines 100Mbps automotive communication. Closely related to the 100Mbps prioprietary protocol BroadR-Reach from Broadcom, 100BASE-T1 applies a single unshielded twisted-pair cable as the physical channel. This channel solution is significantly lighter and dramatically cheaper than other alternatives but is susceptible to the unique automotive environment's cable-routing uncertainties and crosstalk, radiated electromagnetic noise and thermal effects. Another IEEE standard, 1000BASE-T1, is under development for 1Gbps (1000Mbps) automotive Ethernet. Future infotainment needs, as well as many envisioned ADAS capabilities, require very high bandwidth communication internal to the vehicle. Though the 1000BASE-T1 standard is only at a draft stage, there have already been product announcements concerning its support. It is therfore important for system SI solutions for automotive applications to have support for 100BASE-T1 and 1000BASE-T1 protocol compliance.

"Future infotainment needs, as well as many envisioned ADAS capabilities, require very high bandwidth communication internal to the vehicle."

The factor of 10 increase in data rate has implications for PCB design and SI simulations required to ensure reliable operation. As previously observed for computing, telecom and mobile designs, as signals approach the gigabit-per-second range, effects that were safely overlooked in the past start to matter. Things like reflections, crosstalk, interconnect losses, and equalization all become critically important.

For serial links, vias are often the largest impedance discontinuity on the PCB, causing potential reflections along the channel and crosstalk between channels. Methodologies to maintain high signal quality for routing within

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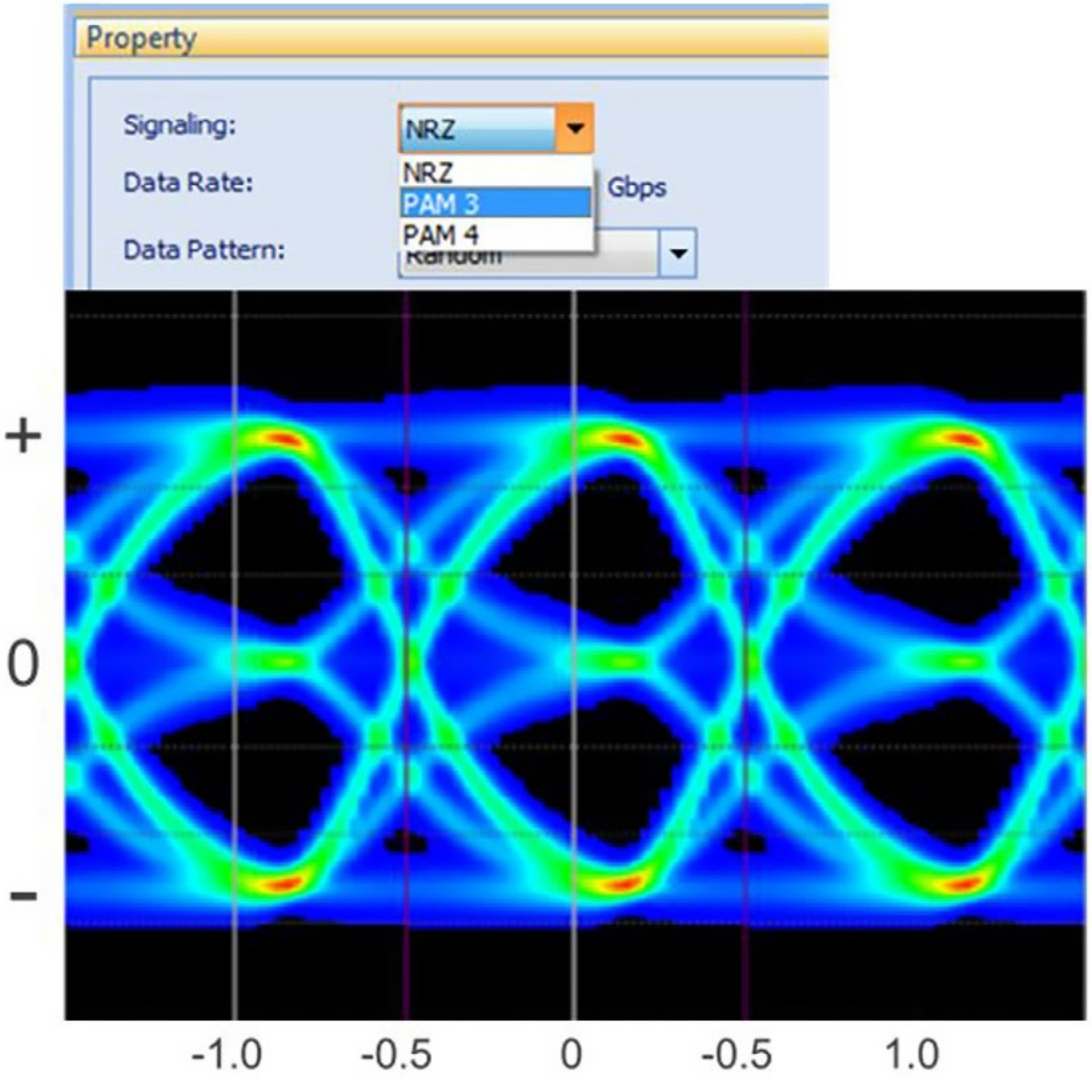


Figure 4: PAM3 simulation.

via fields and to craft transparent inter-layer via transitions have become expected capabilities of PCB design software.

Automotive Ethernet standards allow for up to 15 meters of cable. At gigabit data rates, twisted-pair cables experience significant attenuation due to high-frequency metal loss. Advanced equalization techniques, such as feed forward equalization (FFE) or continuous time linear equalization (CTLE), are applied to compensate. FFE and CTLE are complex DSP algorithms implemented with large and complex transceiver ICs. For PCB system simulations, these algorithms can be addressed with the algorithmic modeling interface (AMI) extension to the IBIS (I/O Buffer Information Sheet) standard. IBIS-AMI models are now readily available from chipset vendors and commonly applied to serial-link simulation of computing and telecom designs. IBIS-AMI models are expected to quickly become equally commonplace for automotive Ethernet transceiver ICs.

Serial links require compliance to a specific BER. For 1000BASE-T1, this value is 1.0e-10, or one error for every 10 billion bits received. Because it is impractical to directly simulate tens of billions bits of data with traditional circuit simulation, high-capacity simulation approaches are applied to simulate hundreds of thousands or even millions of bits to generate

eye diagrams with stable signal density distributions. These distributions are processed to produce bathtub curves to reliably predict BER performance. These simulation approaches apply an impulse response to characterize the serial channel and then apply convolution methods to achieve their high-capacity throughput.

Automotive Ethernet standards apply pulse amplitude modulation (PAM). The 1000BASE-T1 standard targets PAM-3, which means three logic signal levels exist on the channel instead of traditional two-level binary signals (Figure 4). PAM-3 has significant implications for transceiver design as well as the modeling and simulation algorithms. Serial-link simulation software has been recently upgraded to support PAM for IBIS-AMI algorithms. As for transceiver IC design, it is a complex task to accommodate PAM signals in the many equalization algorithms, a task accomplished for PCB system design software in parallel as part of general multilevel PAM signal support.

Due to the application of PAM3, high attenuation and high levels of electromagnetic interference, 1000BASE-T1 designs use forward error correction (FEC). This technique applies Reed Solomon algorithms to boost BER to the required level. FEC is not applied for typical computing or telecom designs but has recently been implemented for PCB system design software to enable automotive Ethernet design.

The final step to complete automotive Ethernet application for mainstream PCB system design is twofold. First, the IEEE standard must be finalized to fully know and implement the protocol compliance checks for serial link performance. Draft-level prototype implementation of such compliance checks is now available. Second, vendors must openly provide IBIS-AMI models for their chipset or IP blocks. This process is slow for computing and telecom device vendors but has become standard practice and seems to be perceived as a market-entry requirement by automotive Ethernet chipset and IP vendors. Rapidly advancing market forces for ADAS and infotainment systems are driving (pun intended) these final steps to be completed sooner than many had envisioned necessary only months ago.

In summary, as the automotive market goes through rapid changes, PCB Design teams must rise to the electrical challenges. Unique signal integrity challenges are faced by design teams due to the systemic nature of an automobile. With safety concerns at a premium, signal quality concerns take a front seat to these challenges. Modern PCB signal integrity tools must advance the features originally developed for computing, telecom and mobile designs to support the automotive industry. Compliance tests for 1000BASE-T1 utilizing three logical signal levels (PAM-3) is just one example. **PCBDESIGN**

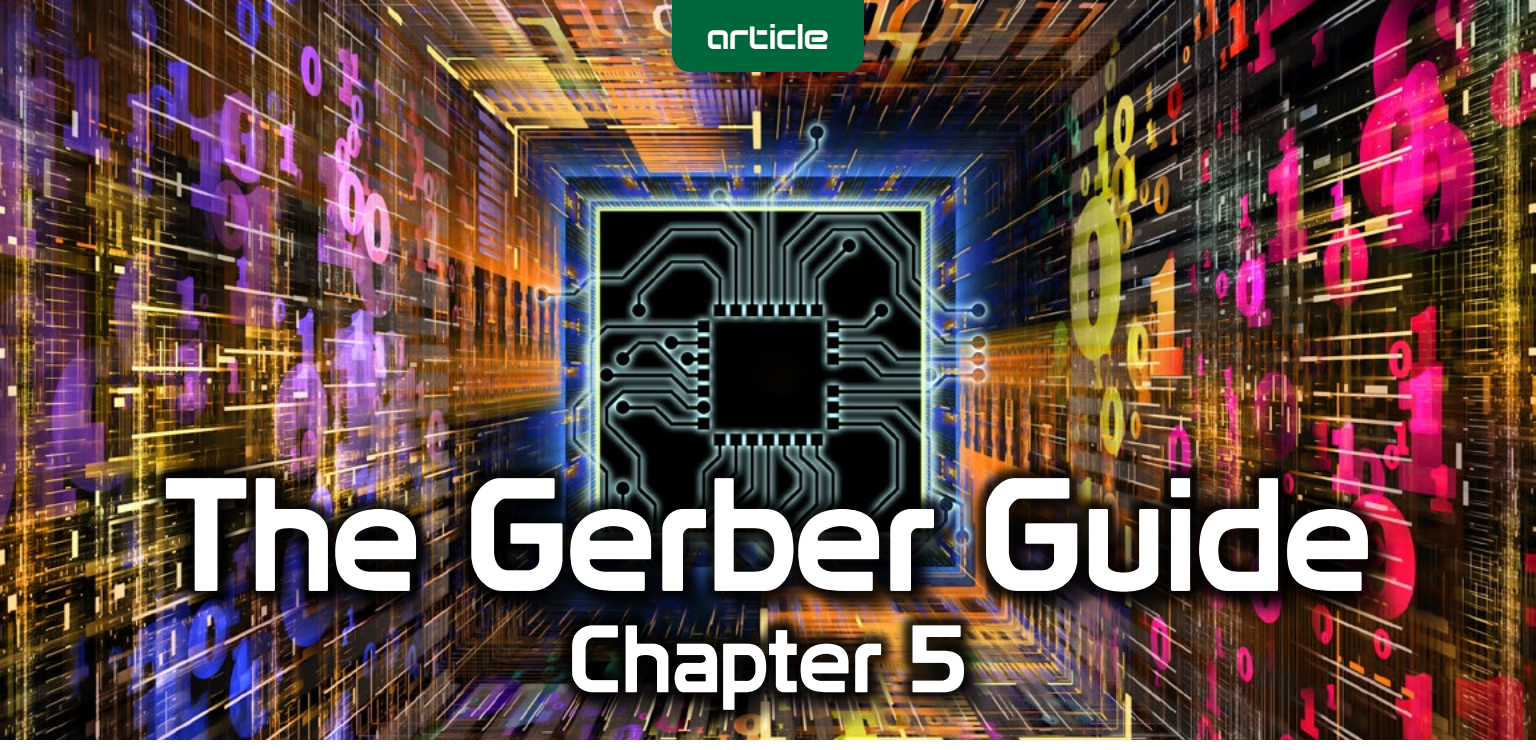
Brad Brim is senior staff product engineer at Cadence Design Systems. He holds a PhD in electrical engineering.

Future Batteries Could Charge in 30 Seconds

Future cell phones and other electronics could have batteries that charge in less than a minute. This new capability will be in part thanks to a space experiment using hard, flexible material as a clean power source.

That potential future is scheduled for launch on the Orbital ATK's S.S. Deke Slayton II Cygnus spacecraft atop a United Launch Alliance Atlas V rocket Dec. 3. A team of students attending Desert Christian School in Lancaster, California, with the support of NASA mentors and the University of California, Los Angeles, developed the experiment.

The experiment is designed to see how graphene-based supercapacitors charge, discharge and deteriorate in a microgravity environment.



The Gerber Guide
Chapter 5

Karel Tavernier
UCAMCO

It is possible to fabricate PCBs from the fabrication data sets currently being used; it's being done innumerable times every day all over the globe. But is it being done in an efficient, reliable, automated and standardized manner? At this moment in time, the honest answer is no, because there is plenty of room for improvement in the way in which PCB fabrication data is currently transferred from design to fabrication.

This is not about the Gerber format, which is used for more than 90% of the world's PCB production. There are very rarely problems with Gerber files themselves; they allow images to be transferred without a hitch. In fact, the Gerber format is part of the solution, given that it is the most reliable option in this field. The problems actually lie in which images are transferred, how the format is used and, more often, in how it is not used.

Each month we look at a different aspect of the design to fabrication data transfer process. In this monthly column, Karel Tavernier explains in detail how to use the newly revised Gerber data format to communicate with your fabrication partners clearly and simply, using an unequivocal yet versatile language that enables you and them to get the very best out of your design data.

Chapter 5: The Layer Structure

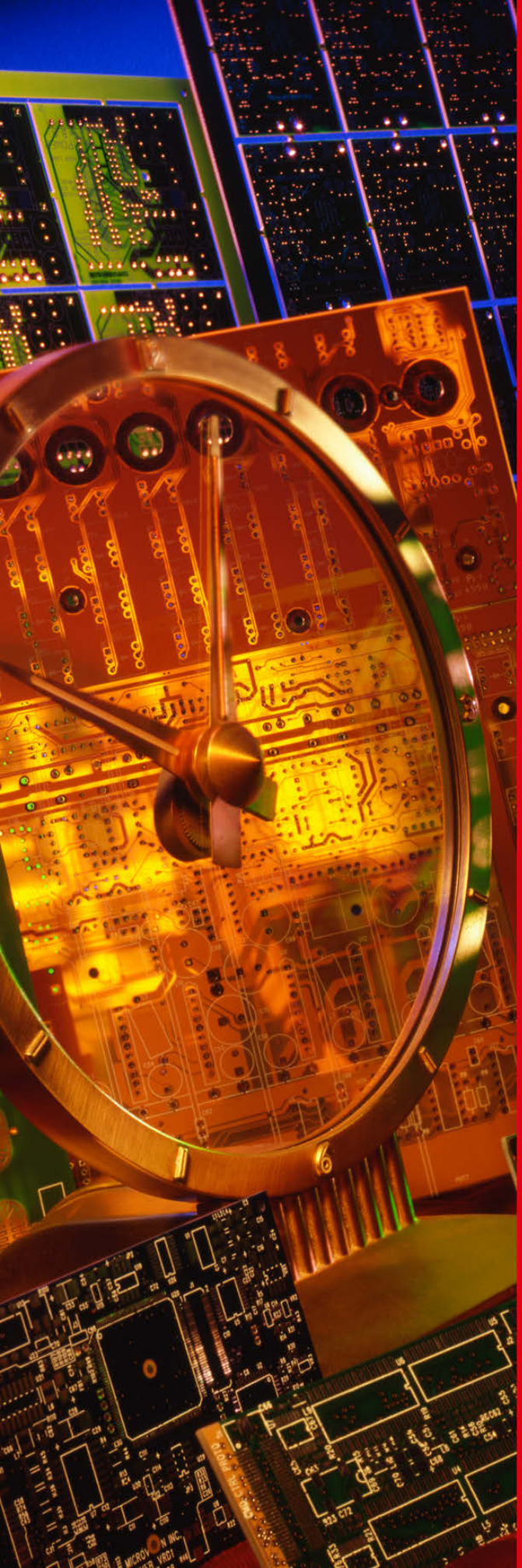
When a PCB fabricator receives a data set, the first thing he does is load it into his CAM system to recreate a model of the PCB. This is the model that will drive manufacturing. To create this model, all image files must be converted and the function of each file in the stack must be clearly defined so it is clear which is the top copper layer, which is the solder mask, etc. The layer structure—the position of each layer—must be defined. After all, a PCB is not a pile of unrelated images, but a strictly ordered set of layers that are laminated together.

The goal is to define this layer structure in an automatic process following a defined standard to eliminate manual work and subjective interpretation. This is precisely what the Gerber specification's .FileFunction attribute does. To quote from the Gerber specification:

> *5.4.1.1 .FileFunction*
> *The .FileFunction file attribute identifies the function of the file in the PCB. The attribute must be set in the file header.*
> *Of all the attributes it is the most important.*

When this attribute is present in the data set, the fabricator's CAM software can use it to assign the file to its correct position in the layer structure, automatically and without any need for manual input. Job done, with no risk of operator error.

To transfer the layer structure according to the standard, you must choose Gerber "X2" output on your layout software, where X2 is shorthand for "Gerber with attributes."



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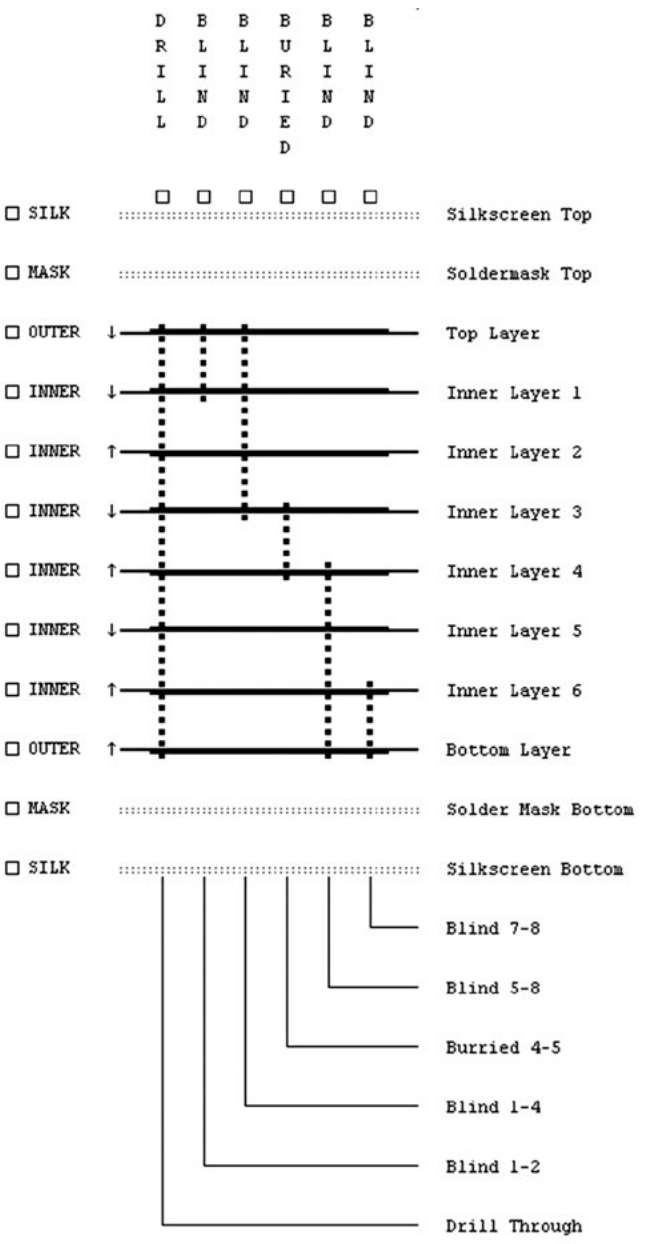


Figure 1: The layer structure.

So what should you do if your PCB layout software is not capable of outputting the current Gerber version with attributes? This is a problem, and indeed the temptation is to suggest that you consider switching to layout software that supports up-to-date Gerber output.

X2 is the Gerber standard to transfer the layer structure. If you cannot output X2, you will need to use an informal method to define the layer structure in a legible form that the CAM operator can use to set the layer structure manually in his CAM system. Naturally, you're hoping that neither of you make mistakes.

The best option is to express the file function in the file name. The Gerber .Filefunction attribute actually allows defining a file naming convention. The Gerber Standard File Naming (GSFN) convention reflects file function in the file name—it encodes the .FileFunction attribute in the file name. This is the closest you will get to a standard without X2 support.

The GFSN standard file name consists of three parts:

1. A free-to-choose prefix identifying the job. This prefix is common to all files for any one job.
2. A postfix identifying file function. The postfix starts with an underscore ('_') followed by the FileFunction value string where the comma (','), which can create confusion in file names, is replaced by '$'.
3. The standard extension .gbr.

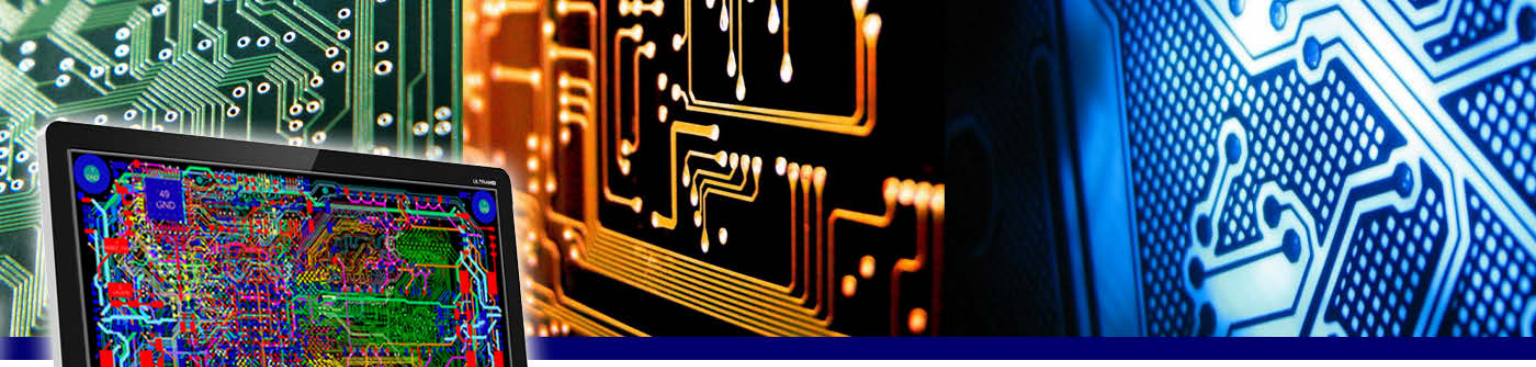
Example:
GJ01911Rev2.1_Legend$Top.gbr
GJ01911Rev2.1_Soldermask$Top.gbr
GJ01911Rev2.1_Copper$L1$Top.gbr
GJ01911Rev2.1_Copper$L2$Inr$Plane.gbr
…
GJ01911Rev2.1_Copper$L10$Inr$Plane.gbr
…

By following the GSFN you clearly identify file function. It is your best option if you cannot use Gerber X2.

Express the layer structure in a standardized way by using Gerber X2. If the standard is not available use clear file names. **PCBDESIGN**

This column has been excerpted from the Guide to PCB Fabrication Data: Design to Fabrication Data Transfer.

Karel Tavernier is managing director of Ucamco.



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TOP TEN

Recent Highlights from PCBDesign007

1 Mentor Graphics Reports Revenues of $291M in Fiscal Q3

Mentor Graphics Corporation has announced financial results for the company's fiscal third quarter ended October 31, 2015. The company reported revenues of $291 million. For the fourth quarter of fiscal 2016, the company expects revenues of about $336 million.

2 SnapEDA: The Female-Owned Startup Revolutionizing CAD Data

SnapEDA founder Natasha Baker may mark the beginning of a new trend in EDA: young female entrepreneurs. (When was the last time we heard about an EDA startup?) As her company prepared for a major launch, Natasha took time to explain the philosophy behind SnapEDA, and how the company is helping designers and engineers manage an ever-increasing volume of CAD data.

3 Digi-Key Partners with Accelerated Designs to Provide Symbols and Footprints for 7.2M Components

Digi-Key Electronics has announced an exclusive, global agreement to distribute software and design data from Accelerated Designs. Accelerated Designs focuses on providing engineers and electronics manufacturers EDA-tool-neutral software and data that improves efficiency of adding and managing new parts when designing circuits and printed circuit boards.

4 Navigating the Global Materials Supply Chain: A Roundtable Discussion

At SMTAI, Andy Shaughnessy sat down for a roundtable discussion with some key players from the materials side of the supply chain. Participants included two executives from Ventec: Mark Goodwin, COO USA and Europe for Ventec International Group; and Jack Pattie, president of Ventec USA. Also participating in the roundtable were Schoeller Electronics CEO Michael Keuthen, and Bob Willis of the National Physics Laboratory.

5 Arlon's John Wright Discusses New High-Performance Materials

During productronica, European Editor Pete Starkey interviewed Engineering/Quality Manager John Wright of Arlon. They discussed Arlon's new 85HP ceramic-filled polyimide, as well as a non-woven aramid material, suitable for space applications, that is a drop-in replacement for a similar material discontinued by a competitor in 2006.

6 Good in, Good out: Bay Area Circuits Discusses Data Strategies

A lot of companies talk about the importance of good data management. Then there are companies like fabricator Bay Area Circuits. I recently sat down with Bay Area Circuits President Stephen Garcia and COO Brian Paper to discuss how automating and upgrading their data systems has significantly cut down overall process time, as well as their drive to educate young PCB designers and actively promote the industry to the emerging electronics industry workforce.

7 Zuken Innovation World 2016 Submission Deadline Draws Near

Time's running out to submit your presentation for Zuken Innovation World 2016, to be held April 18-20, 2016 in San Diego. This year's theme is Zuken University, with a shift toward classroom-style interactive sessions with smaller audiences. A session can range from design tutorials to emerging trends. Please submit your session topic today, before time runs out.

8 Beyond Design: Stackup Planning, Part 4

In this final part of the Stackup Planning series, I will look at 10-plus layer counts. The methodology I have set out in previous columns can be used to construct higher layer-count boards. In general, these boards contain more planes and therefore the issues associated with split power planes can usually be avoided. Also, 10-plus layers require very thin dielectrics in order to reduce the total board thickness.

9 On Scene: ICT Darlington Seminar, 24 November 2015

Darlington, in the northeast of England, has become an established venue for the Institute of Circuit Technology's annual Northern Seminar, a not-to-be-missed opportunity for the UK's PCB technologists to keep abreast with current developments and to network and exchange ideas and experiences with their peers. Coordinated by ICT technical director Bill Wilkie, and generously supported by Merlin PCB Group, the programme consisted of papers on funded projects and project funding, and updates on chemical process technology.

10 Mentor Debuts Multi-Discipline Systems Engineering Tools for the Transportation Market

Mentor Graphics Corporation has launched new tools delivering integrated electrical/electronic/software systems engineering capability for the transportation market. The new CapitalSystems tools allow implementations to be optimized for key parameters such as cost and weight.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out ***The PCB Design Magazine's*** event calendar.

DesignCon 2016
January 19–21, 2016
Santa Clara, California, USA

EIPC Winter Conference
January 21–22, 2016
Dresden, Germany

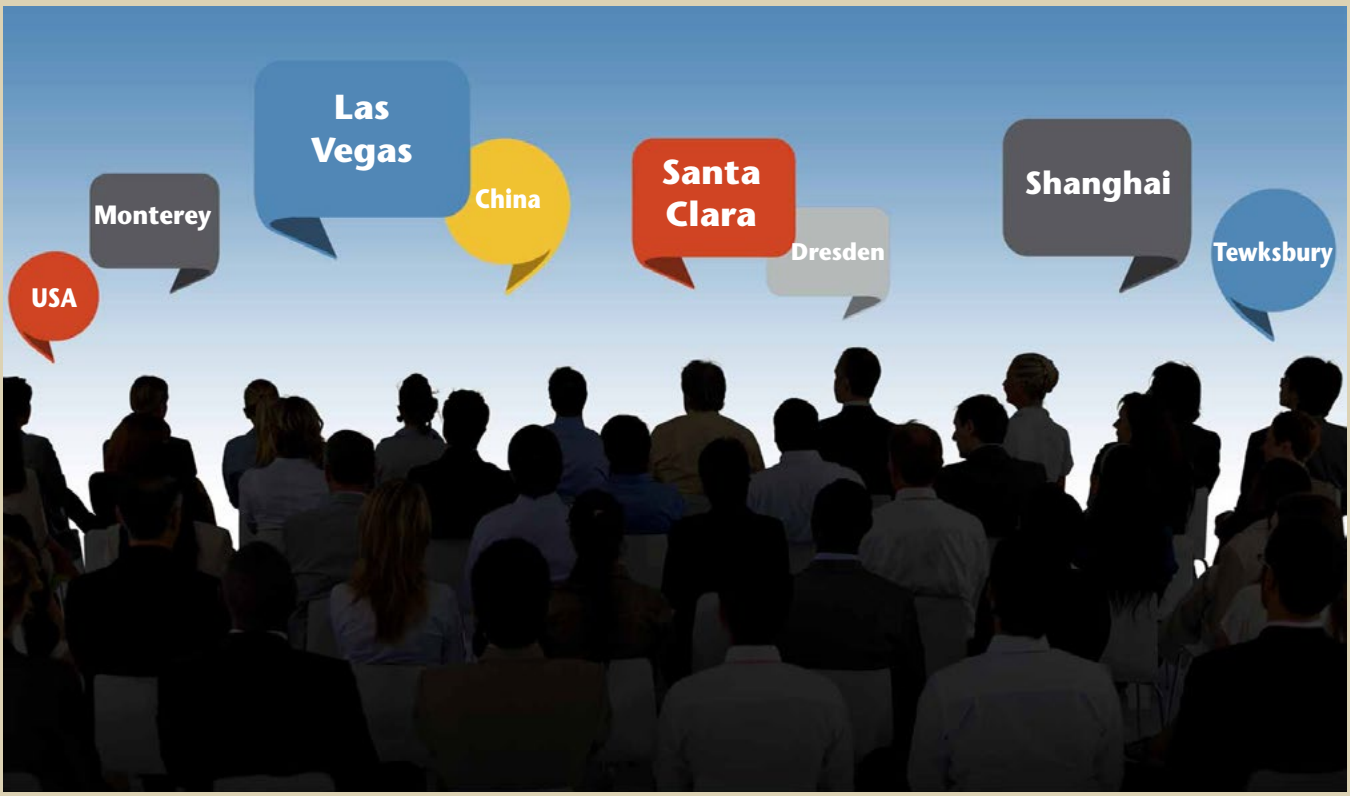
FlexTech Alliance
February 29–March 3, 2016
Monterey, CA USA

ICT-UK Evening Seminar
March 1, 2016
Tewksbury, England

IPC APEX EXPO 2016 and the Design Forum
March 13–17, 2016
Las Vegas, Nevada USA

25th China International PCB & Assembly Show 2016 (CPCA)
March 15–17, 2016
Shanghai, China

For additional events, see our other magazines.



PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

EDITORIAL:

MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

MAGAZINE PRODUCTION CREW:

PRODUCTION MANAGER: **MIKE RADOGNA**
mike@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA, TOBEY MARSICOVETERE**

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EDITORIAL CONTACT

Andy Shaughnessy
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SALES CONTACT

Barb Hockaday
barb@iconnect007.com
+1 916 365-1727 GMT-7

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