PCB Routing Guidelines for Signal Integrity and Power Integrity

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Orange County chapter meeting

November 18, 2015

Agenda

- Insertion Loss 101
- PCB Design Guidelines For SI
- Simulation Examples and Tools
- Power Integrity Examples

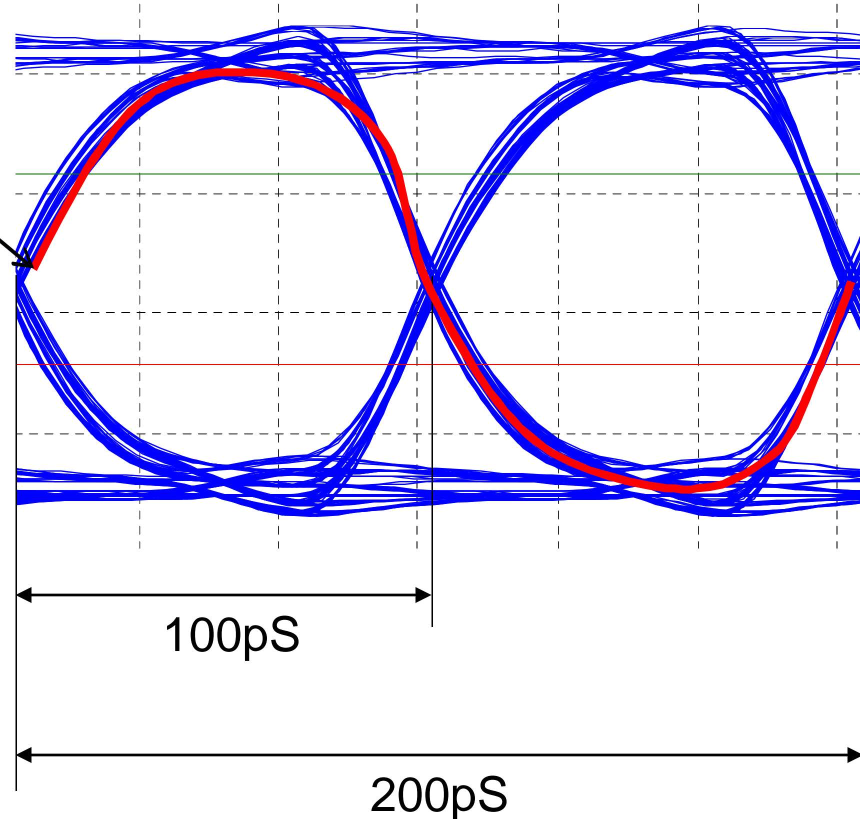
Insertion Loss 101

What is Insertion Loss?

Insertion loss is the loss of signal amplitude resulting from the insertion of a device in a transmission line and is expressed in decibels (dB)

Datarate and Fundamental Frequency

The 10Gbps Signal

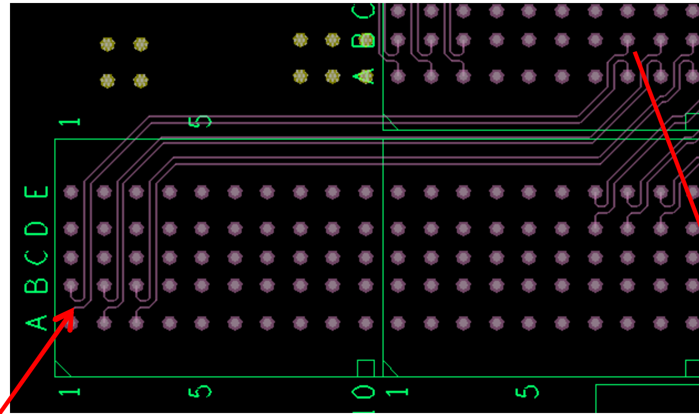


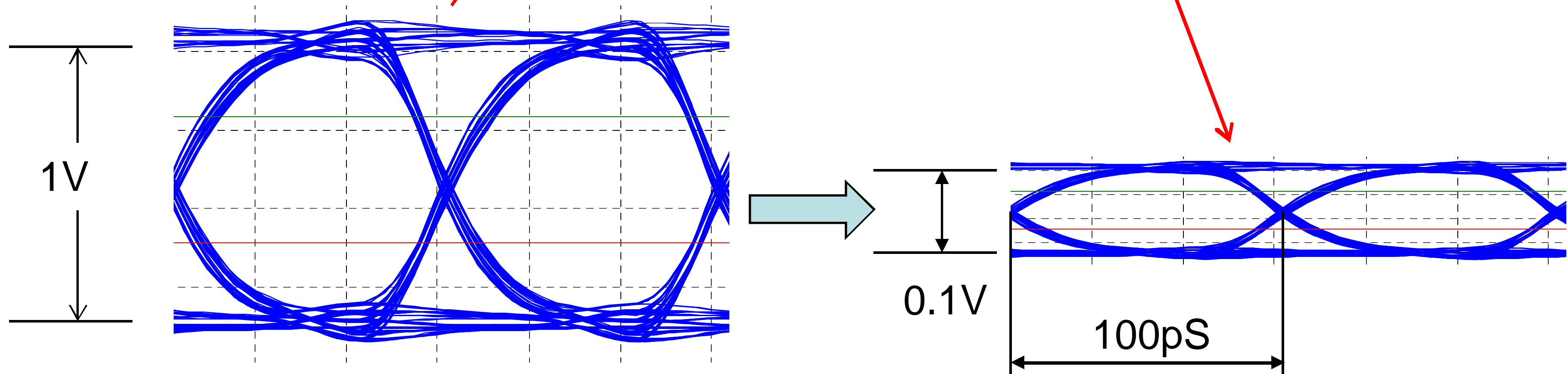
Datarate = 10Gbps = 10e9
Time Between Crossings = 1 / 10e9

Period of Sinusoid = 200pS
Frequency of Sinusoid = 1 / 200pS **= 5e9**

The "**Fundamental Frequency**" = 5e9 = 5GHz
Also called the "Nyquist Frequency"

10Gbps Example

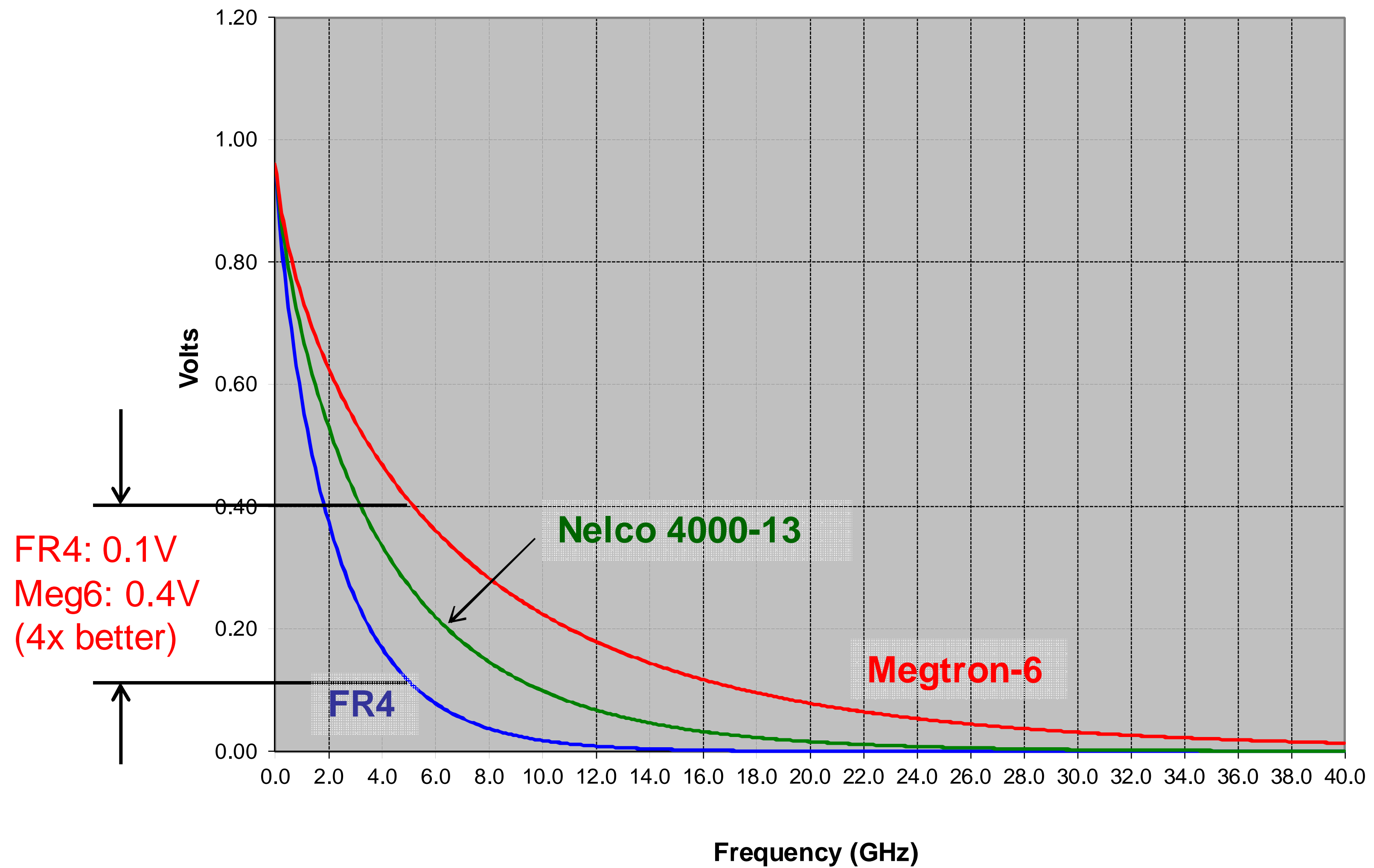




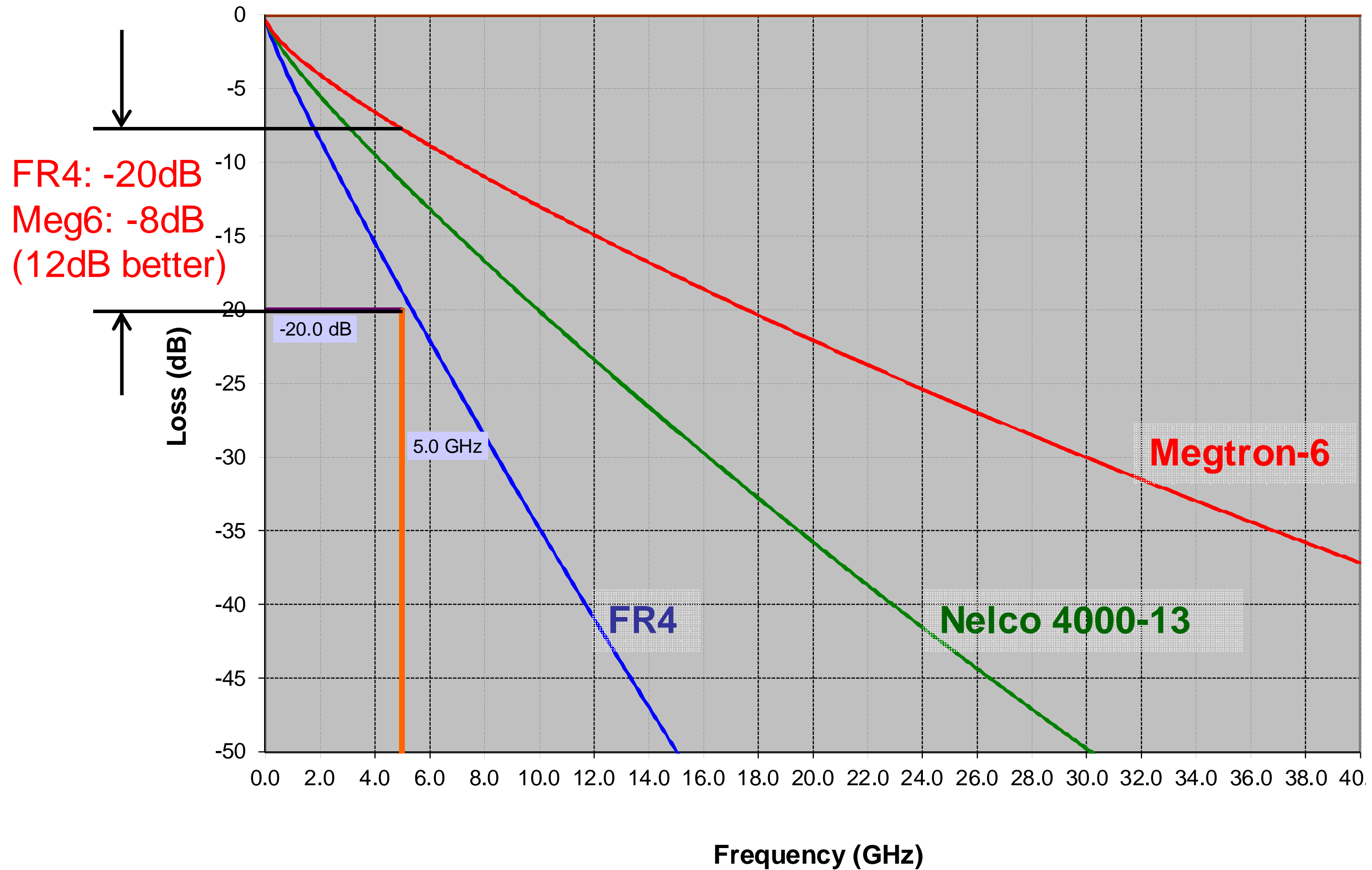
How much insertion loss does this path have?

20 * log (0.1 / 1.0) = -20dB of Insertion Loss (at 5GHz)

Voltage vs Material in Volts



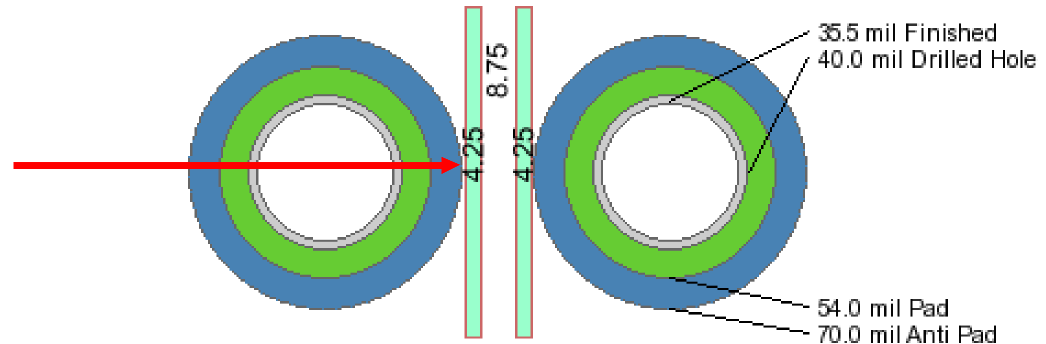
Loss vs Material in dB



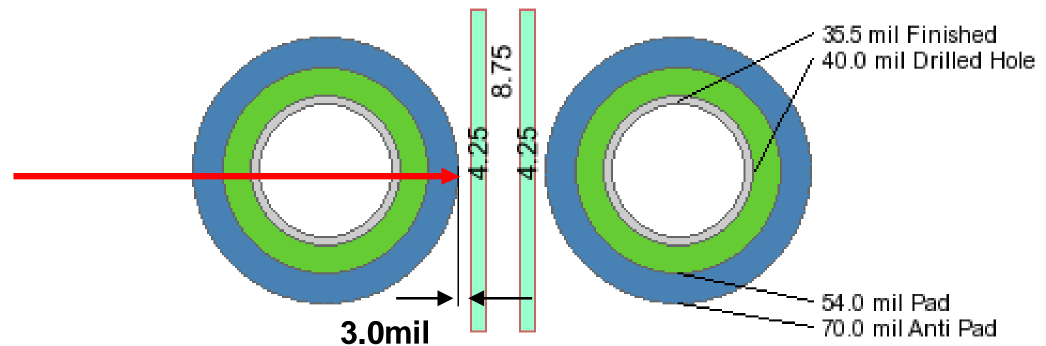
PCB Design Guidelines For SI

Routing Through Antipads

Do Not Rout traces by antipads without any overhang.

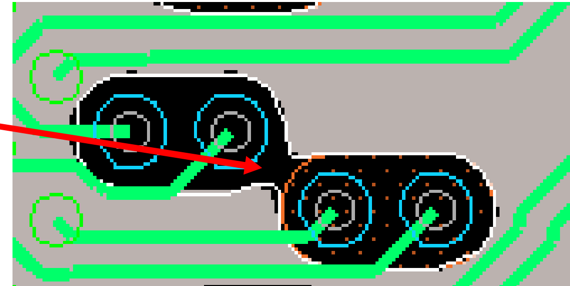


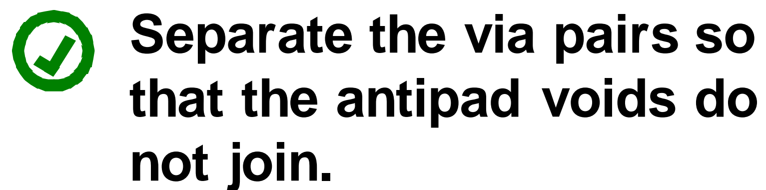
Ensure 3.0mil of Ground plane overhang when routing through Antipads.



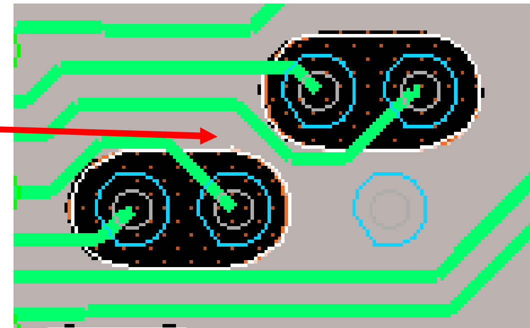
Joining Antipads: 1

Do not join Antipad Voids together.

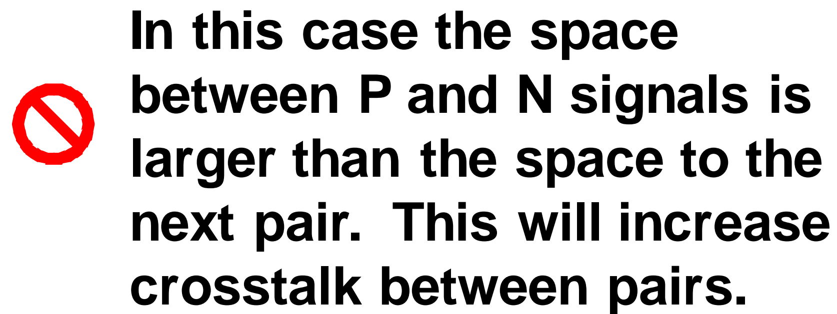




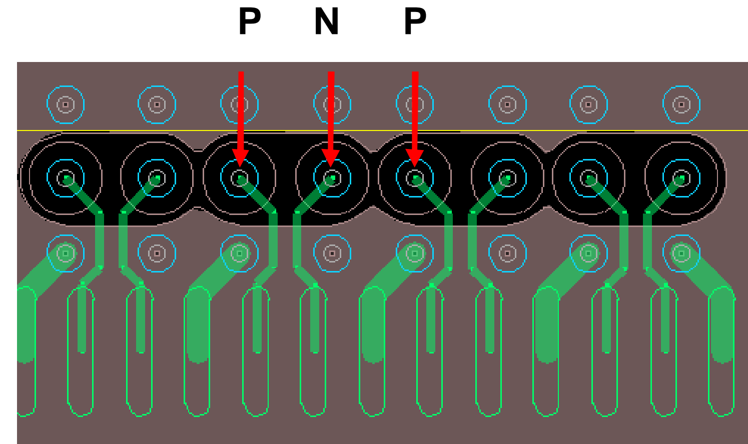
Separate the via pairs so that the antipad voids do not join.

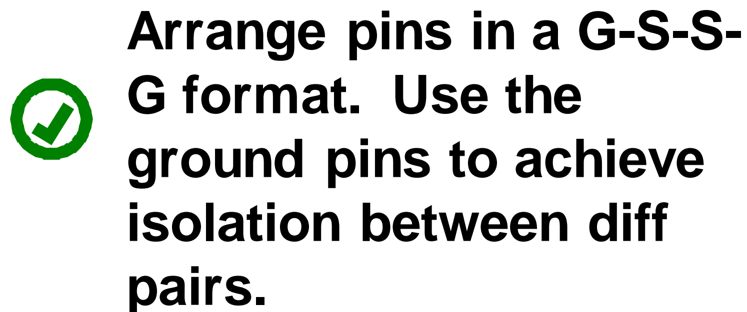


Joining Antipads: 2
IPASS Connector

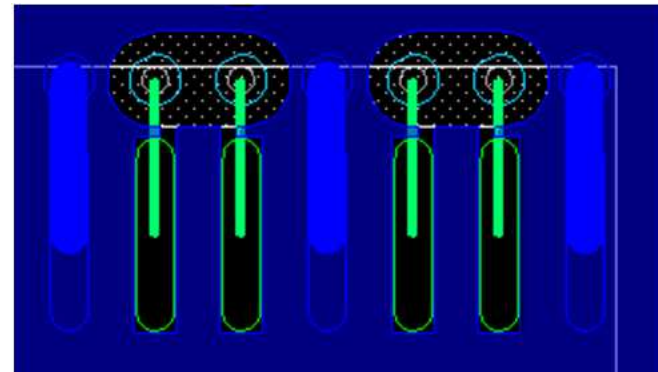


In this case the space between P and N signals is larger than the space to the next pair. This will increase crosstalk between pairs.



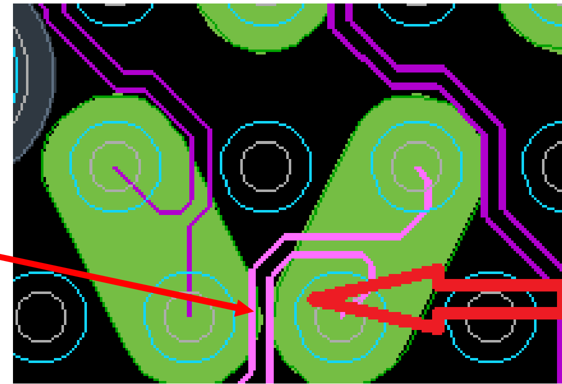


Arrange pins in a G-S-S-G format. Use the ground pins to achieve isolation between diff pairs.

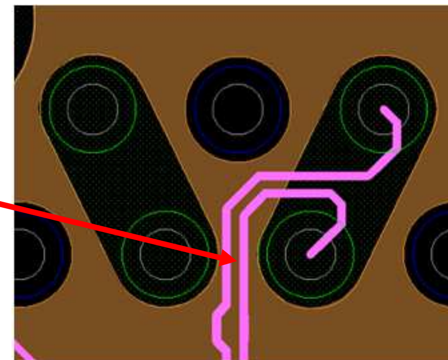


Antipads too Close

Antipads too close causing no ground plane for diff pair.

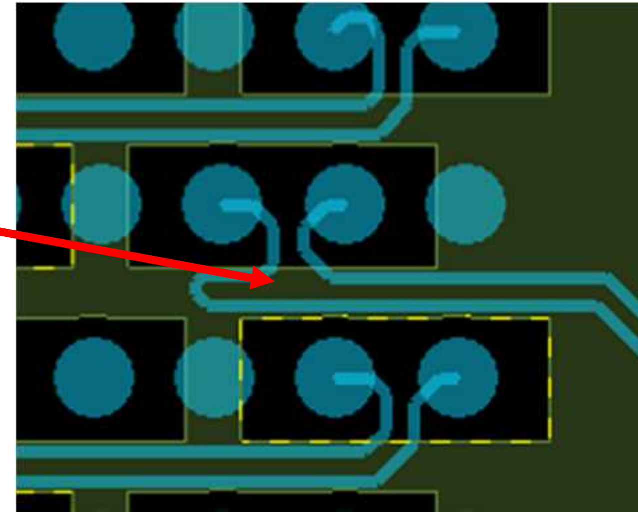


Reduced size of antipad allows for adequate ground plane overhang

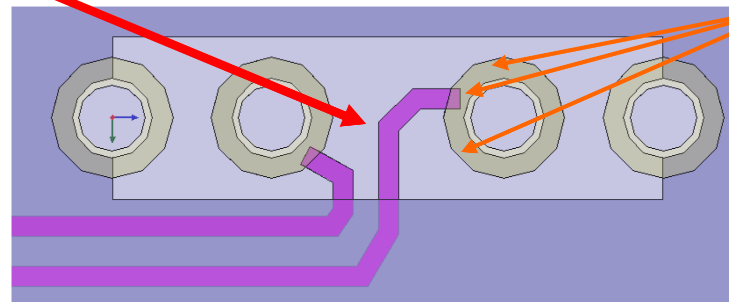


Skew Compensation: 1

This method of increasing length causes crosstalk and impedance issues for any signal over 500MHz

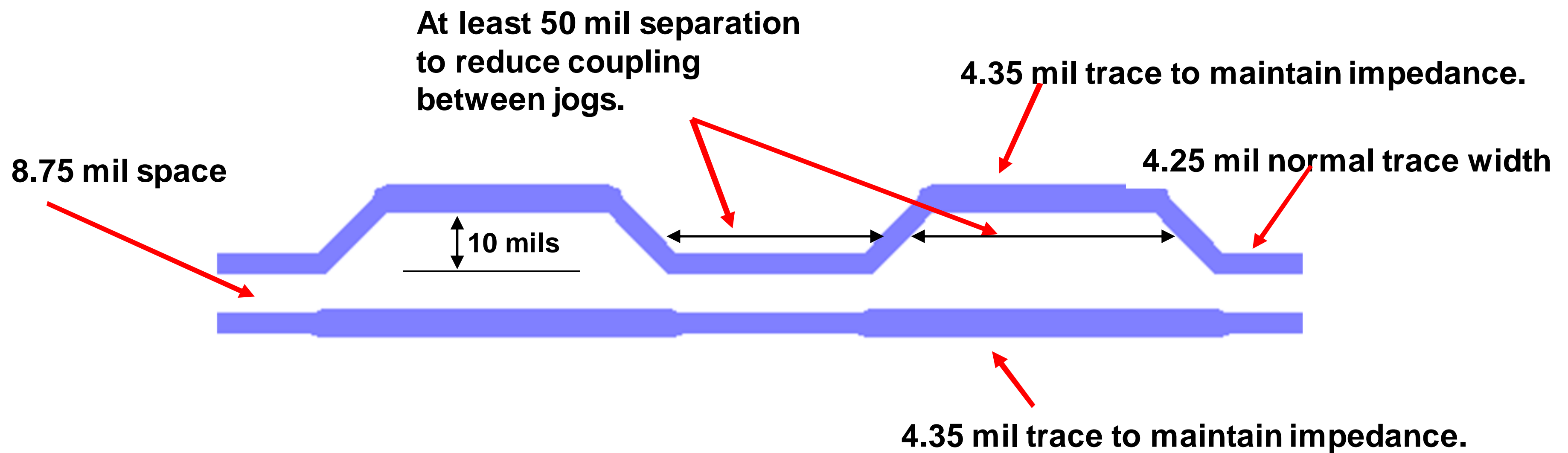


Lengthen Trace within the antipad region as shown.



Trace can connect to pad at these locations. Keep lengthened trace within the antipad opening.

Skew Compensation: 2

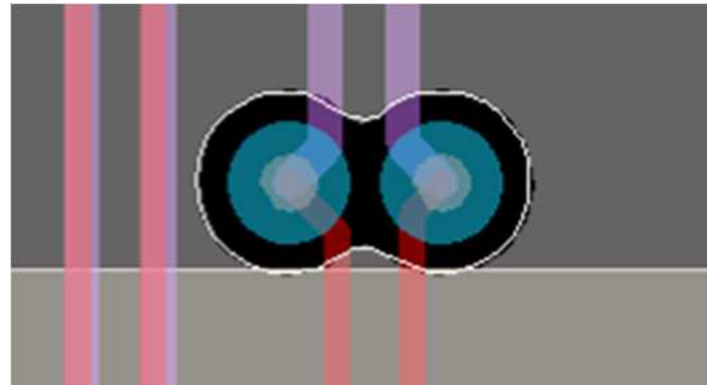


This is the recommended approach

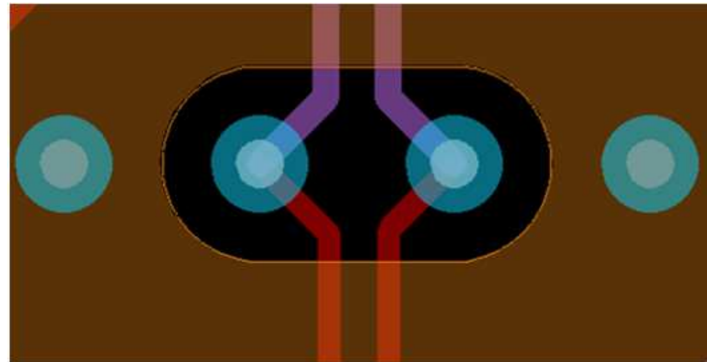
The wider trace widths need to be calculated with a field solver for each application.

Transition Vias Without Grounds

No Ground Vias for the diff pair.

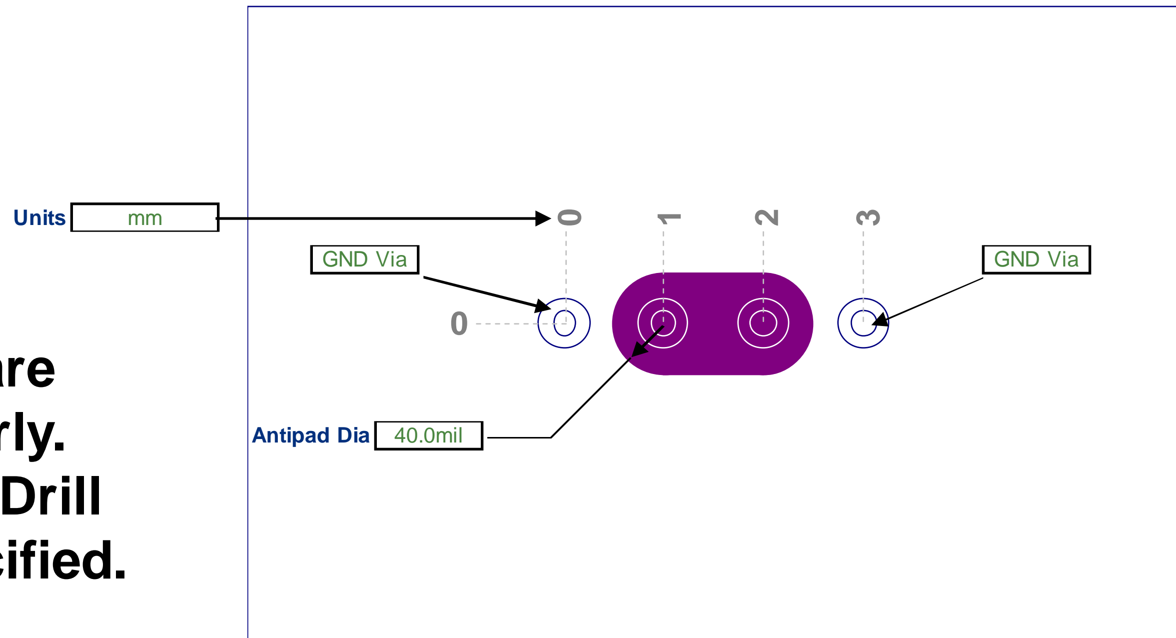


Ground vias added as described in pre-layout simulation results.



Transition Vias: Proper Design

Ground Vias are spaced properly. Antipads and Drill sizes are specified.



Finished Dia	8.0mil	Diff Port Zo	100	Material	RogersTheta
Drill Dia	9.8mil	Layer Escape	6	Dk	3.9
Pad Dia	20.0mil	Line Width	6mil	Df	0.01
Antipad Dia	40.0mil	EtchBack	0.1mil	Layers	8
Oval Dogbone	40.0mil	Line Space	6.70mil	Thickness	91.7 mil

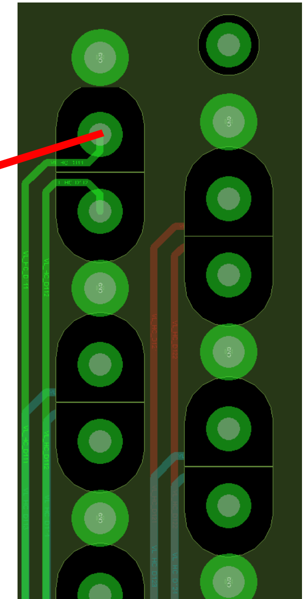
Drill Size Versus Finished Size

Pad Stack Drill Diameter shows the Finished Diameter.

Fab Drawing attempts to correct the problem by stating what drill size to use

Use 17.7mil drill	©	14.0
Use 23.6mil drill	®	20.0

Drill/Slot hole
Hole type: Circle Drill
Plating: Plated
Drill diameter: 14.000
0.000
Tolerance: + 2.000 - 2.000
Offset X: 0.000
Offset Y: 0.000
Non-standard drill:



Signal Integrity Tools import the Drill Size from the Padstack, making simulation results look better than they actually are.

Drill size in PCB Design Padstack should match Drill size desired. It's <u>not OK</u> to allow the PCB Fabricator to pick a drill size.

Specify Drill Size for Transition Vias and AC Caps

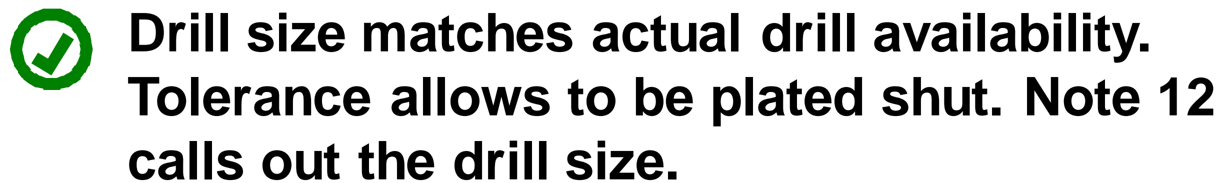
Drill Chart doesn't specify the drill size, but the finished size only

DRILL CHART 1: PRIMARY SIDE to SECONDARY SIDE

7 ALL UNITS ARE IN INCHES

FIGURE	SIZE	TOLERANCE	PLATED	QTY
(A)	.010	+.003/−.01	PLATED	5265

Drill size matches actual drill availability. Tolerance allows to be plated shut. Note 12 calls out the drill size.



DRILL CHART: TOP to BOTTOM

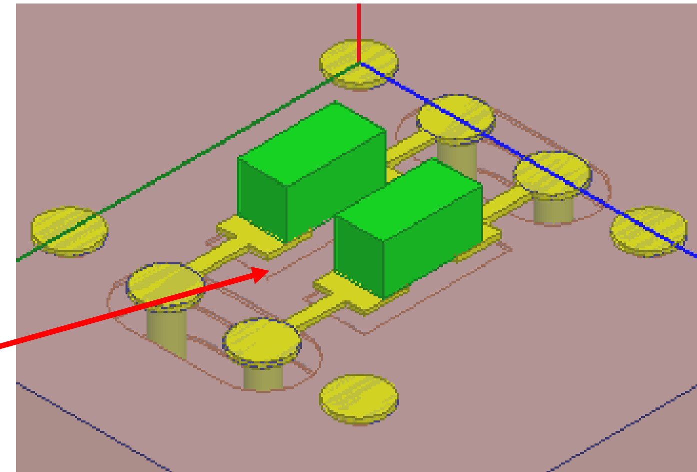
ALL UNITS ARE IN INCHES

FIGURE	SIZE	TOLERANCE	PLATED	QTY
12 ◆	Ø.00984	+Ø.Ø/-Ø.Ø1	PLATED	3215

12 ALL HOLES DIAMETERS INDICATED ARE FINISHED SIZE WITH THE EXCEPTION OF THE Ø.ØØ98" SIZE. THE Ø.ØØ98" SIZE HOLE REFERS TO THE DRILL DIAMETER.

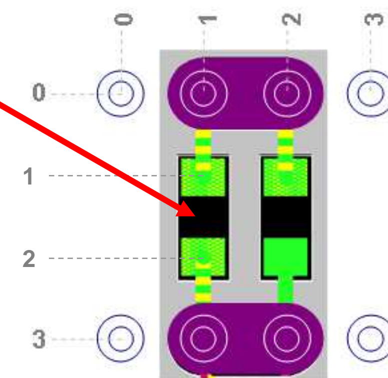
Reliefs Under AC Caps

Add a relief under AC Capacitors on the adjacent ground plane to increase impedance for 0402 Caps on 1mm pitch

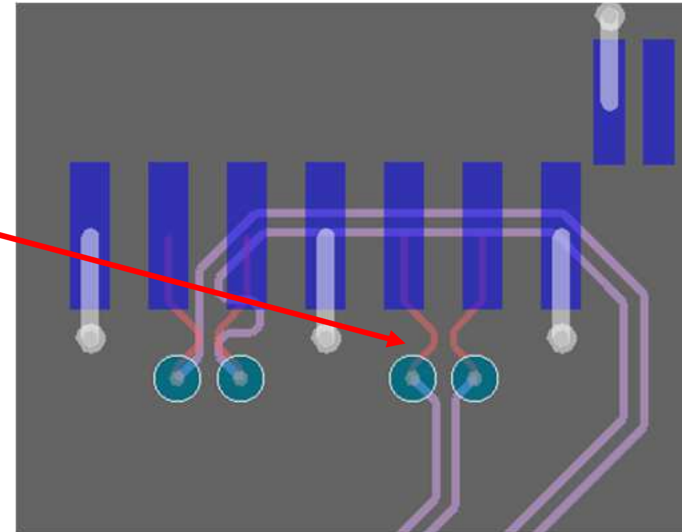


Relief can be individual rectangles or a full rectangle encompassing both capacitors.

Either way it must be simulated and verified. It is stackup and material dependent!



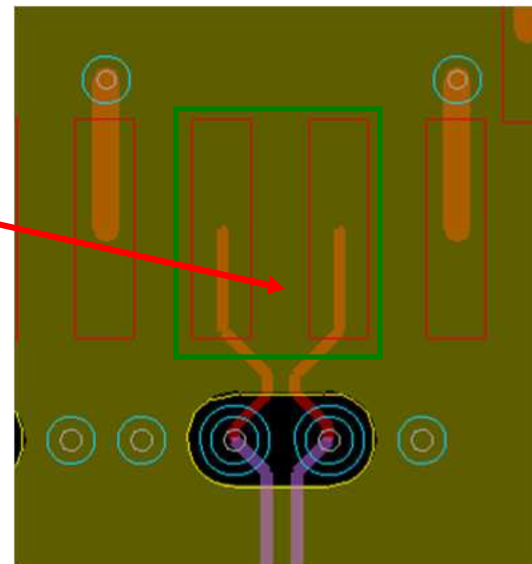
SMT Pad Transitions



No Ground Vias for the diff pair. No clearance under pads.

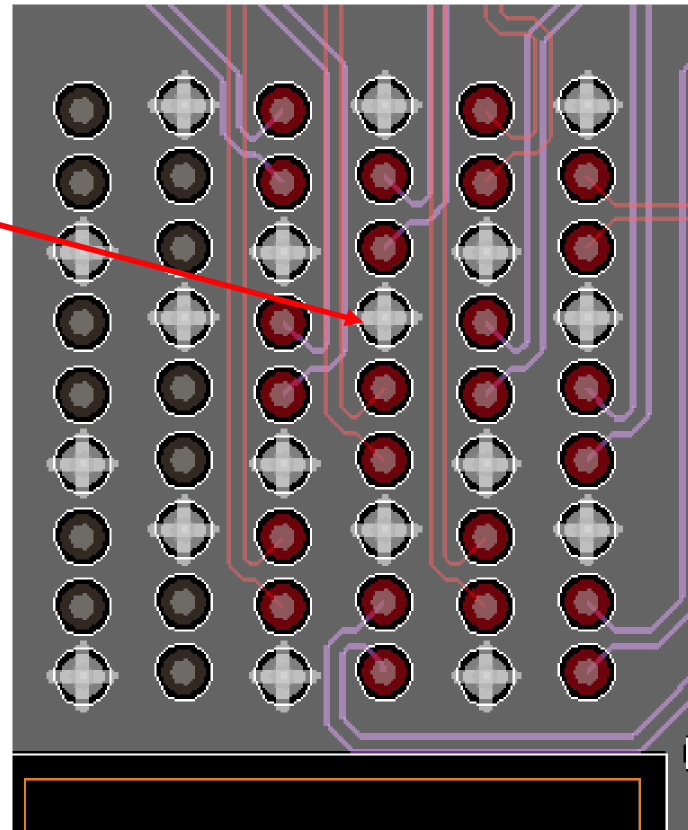
Ground vias added as described in pre-layout simulation results.

Clearance under pads on adjacent plane layer only, increase impedance for a better match to 100ohms



Thermal Reliefs on Press Fit Connectors

Do Not use Thermal Reliefs on Press Fit Connectors.

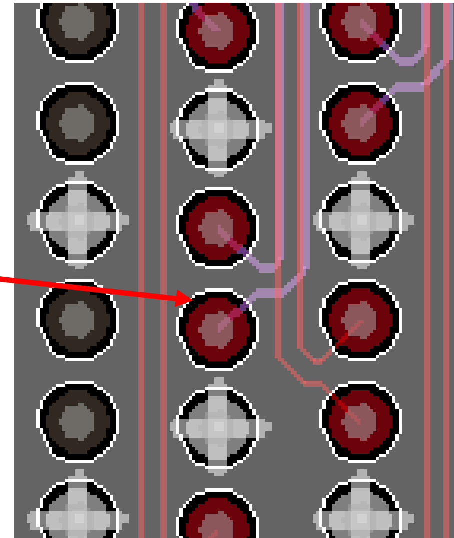


Change Thermal Reliefs to Direct Connections to the plane.

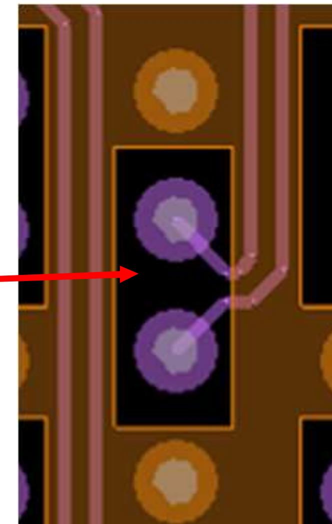
Rectangular or Oval Antipads on High Speed Connectors

Do Not use simple round antipads on high speed connectors

(Example: AirMax)

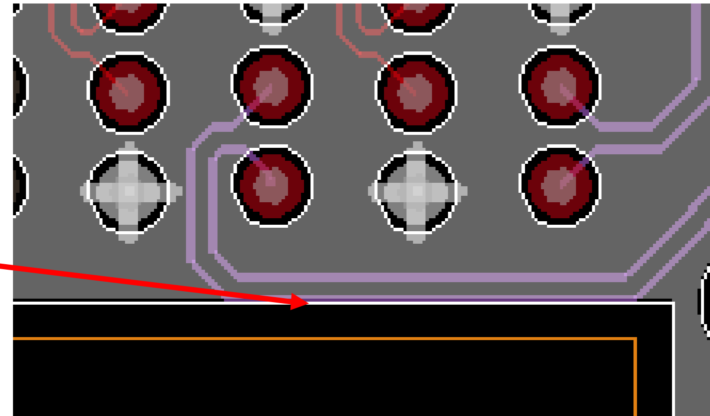


Change to rectangular or oval shape described in pre-layout simulation results.



Routing Over Ground Plane Edges

Do Not Rout Over and Ground Plane Edge

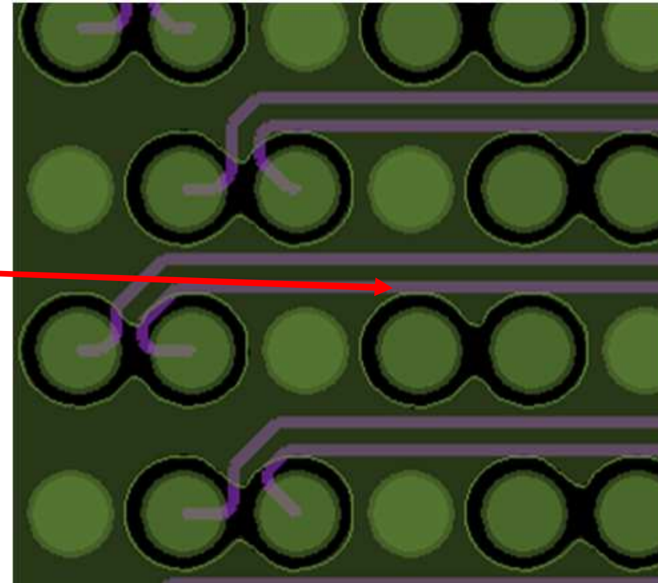


Move the etch away from the ground plane edge or increase the size of the ground plane edge. Diff pair should be >30mil (8H) from edge of plane.

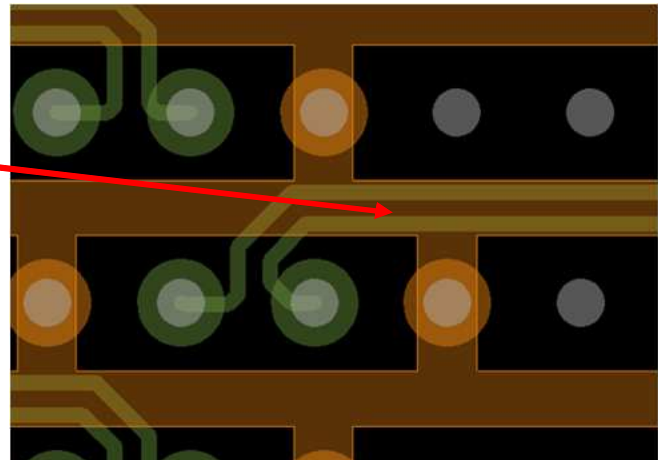
H=Distance from Signal Layer to reference plane layer

Diff Pairs Not Centered in Routing Channels

- Diff pairs running over antipad edges

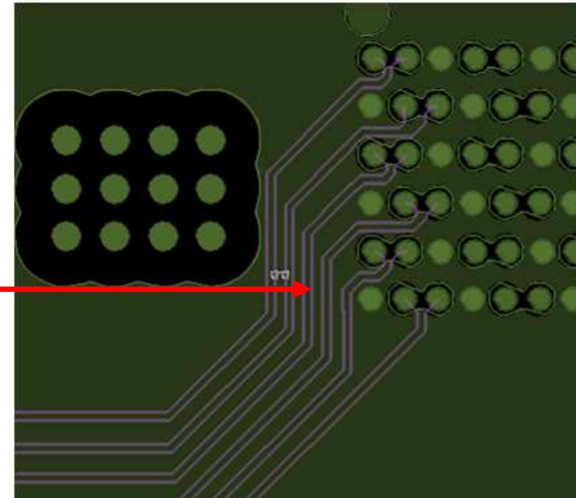


- Diff pair centered in the channel.

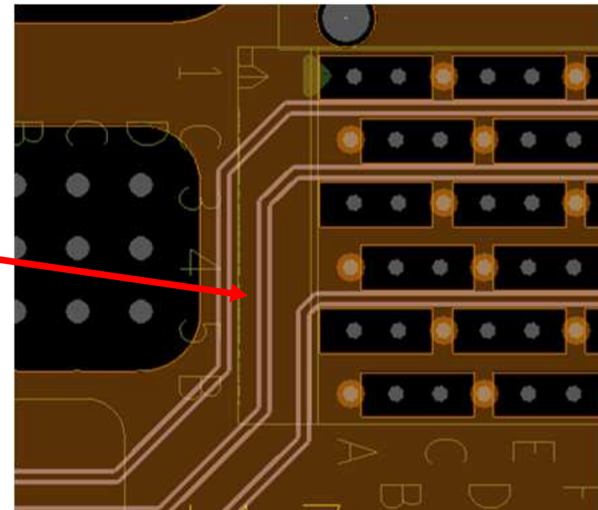


Diff Pairs Spaced Too Close

6-9-6 diff pair spaced 10mils apart. Needs 25-30mils of spacing (4H).

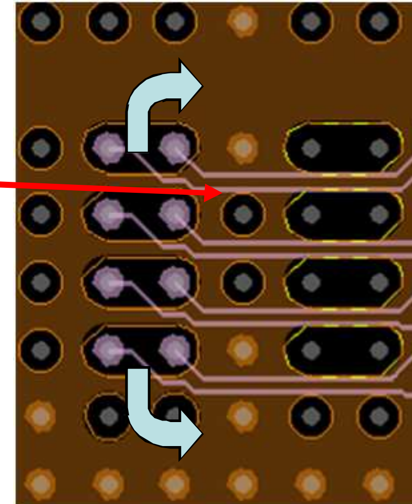


Diff pairs spaced by 30mils

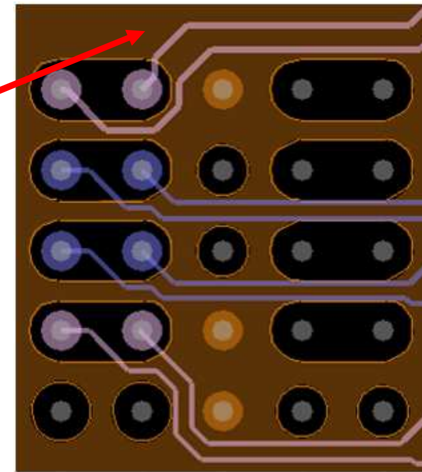


Take Advantage of "Unused" Ground Planes

Move diff pairs up to adjacent channel to avoid the nearby Tx pair and to make use of a better ground reference.



Diff pairs moved away from nearby oval antipads to minimize coupling to other BGA signal pads.



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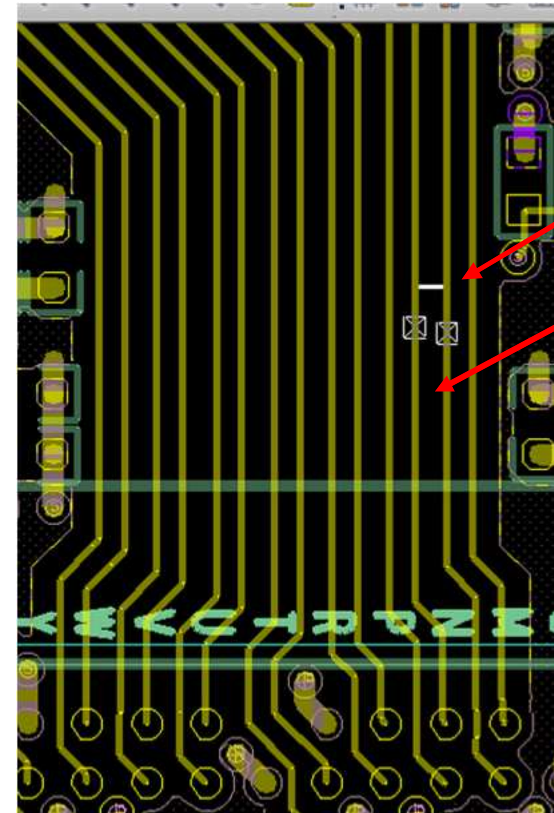
Diff Pair Spacing on Top and Bottom Layers

Microstrip surface pairs are 12mil between P and N. Diff pairs are spaced 16mil apart. This causes lots of crosstalk.

They need to be 50-75mil apart! (10H)

Move diff pairs to inner layers and use closer spacing between P and N (8mil).

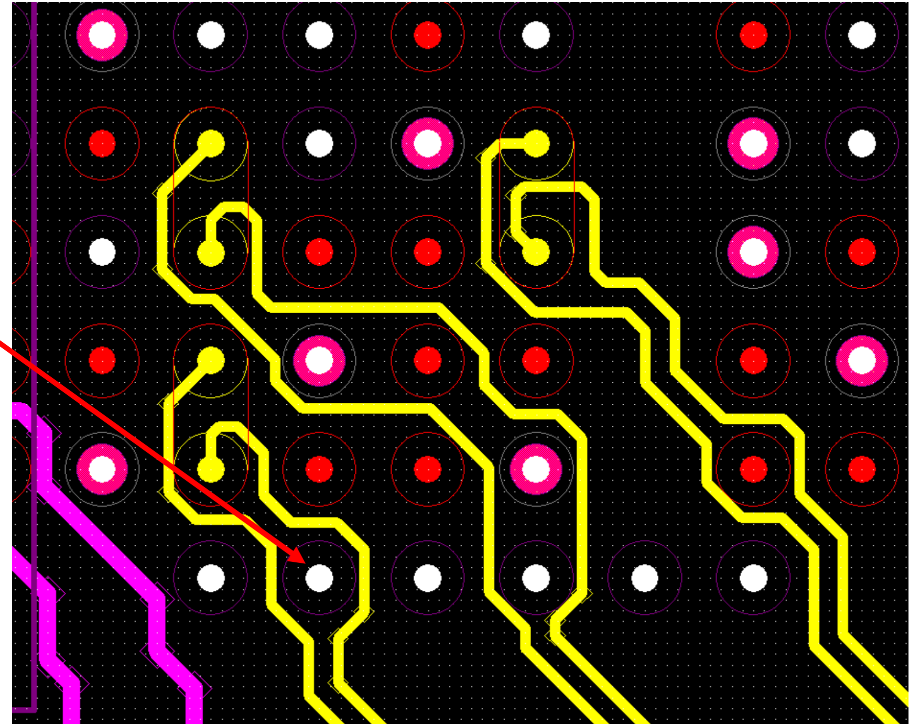
Or use 50-75mil spacing between pairs on the surface.



Splitting Up Diff Pairs: 1

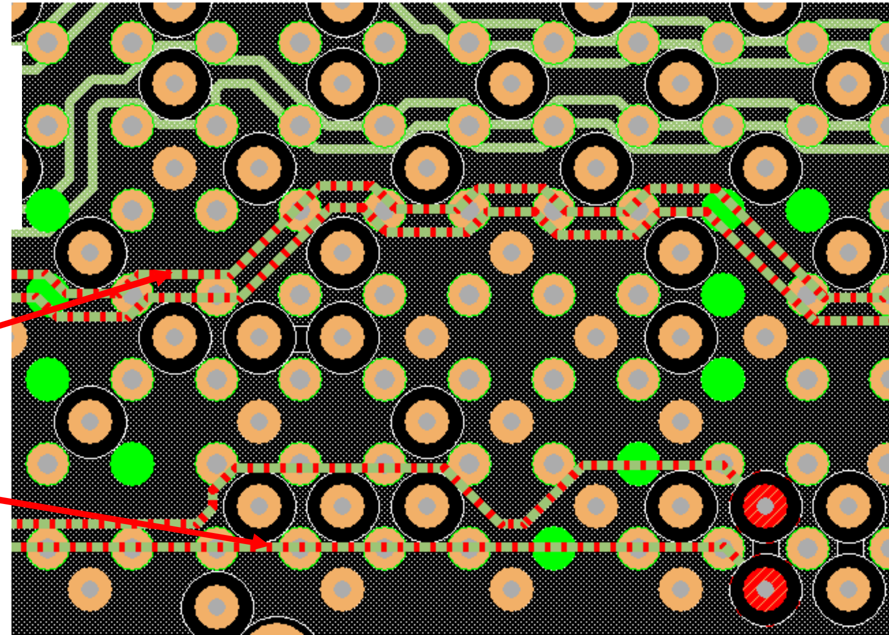
- 🚫 **Avoid separating diff pairs to get around vias.**

- ✅ **Keep the pair coupled together at all times.**



Splitting Up Diff Pairs: 2

Avoid separating diff pairs to get around vias.



3-4-3 : 102 ohms

3-21-3: 112 ohms

Keep the pair coupled together at all times.
Widen the line in areas where the lines pull apart.

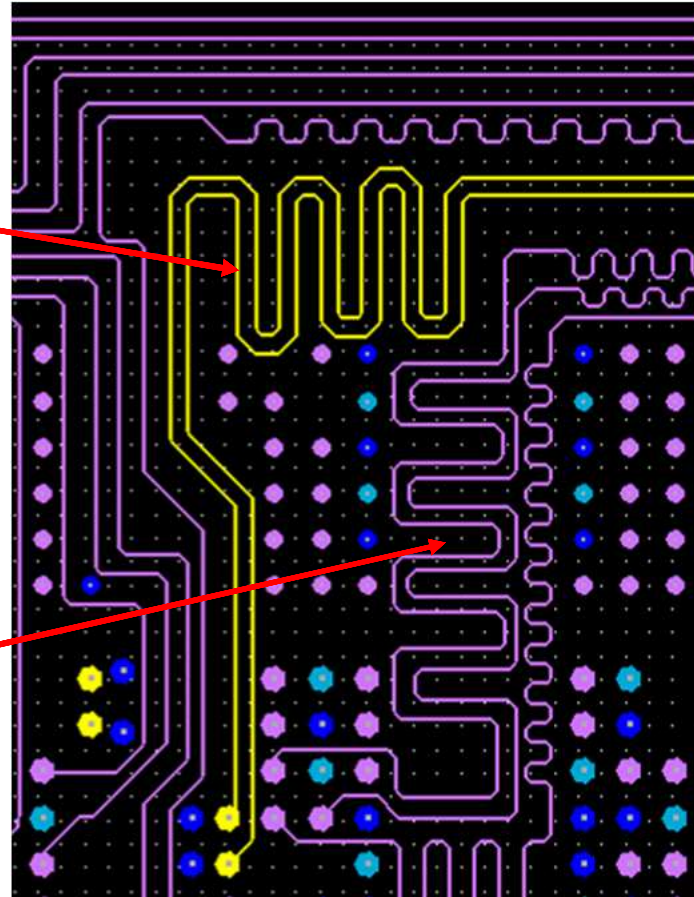
Serpentine Spacing

Serpentines are 13mils apart.

Diff pairs are 8.75mils apart.

This causes about 0.2% of crosstalk on to itself, which is too high.

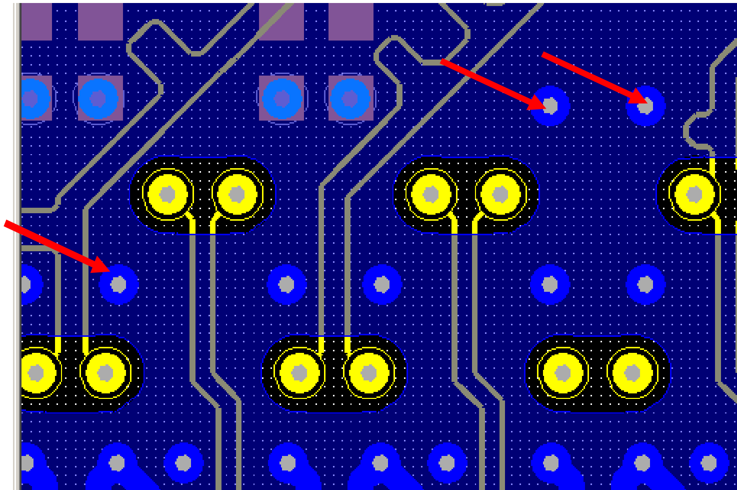
Increase spacing to 17mils or more (4H)



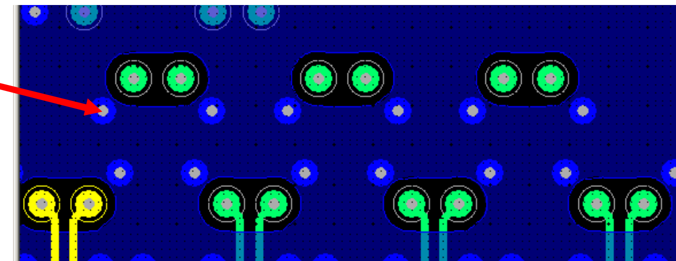
H=Distance from Signal Layer to reference plane layer

Haphazard Ground Via Locations

Ground Vias are positioned randomly.



Ground Vias placed matching pre-layout simulations



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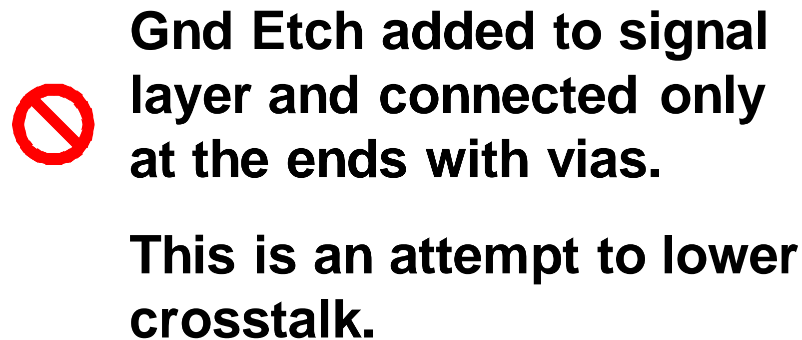
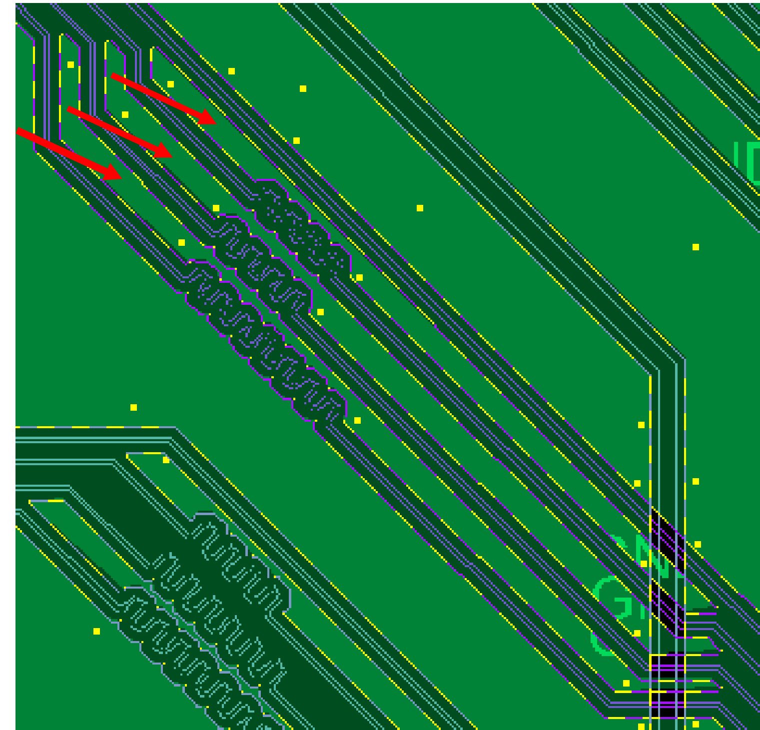
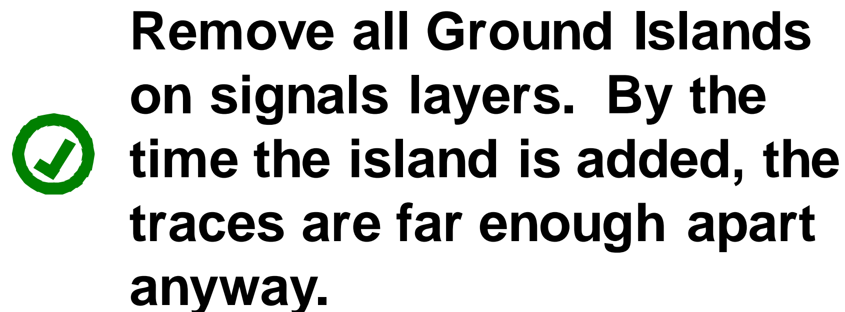
Floating Ground Islands on Signal Layers



Gnd Etch added to signal layer and connected only at the ends with vias.

This is an attempt to lower crosstalk.

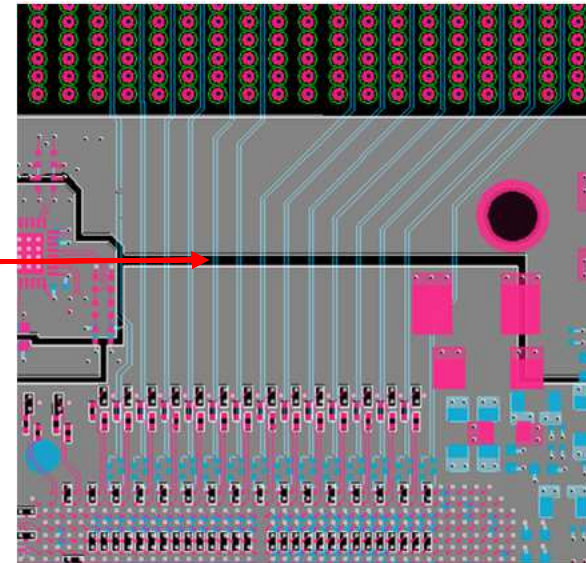




Remove all Ground Islands on signals layers. By the time the island is added, the traces are far enough apart anyway.

Routing Over Splits: 1

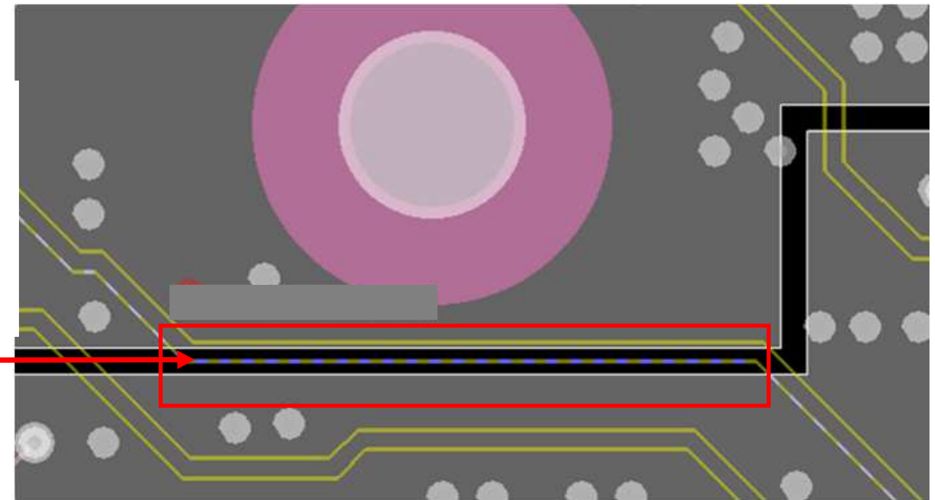
Traces crossing over a split in the ground plane on an adjacent layer



Remove the split in the ground plane or move the traces to a layer that has a continuous plane.

Routing Over Splits: 2

- 🚫 **DQS DDR3 signal runs down the split in the plane shown in red box.**

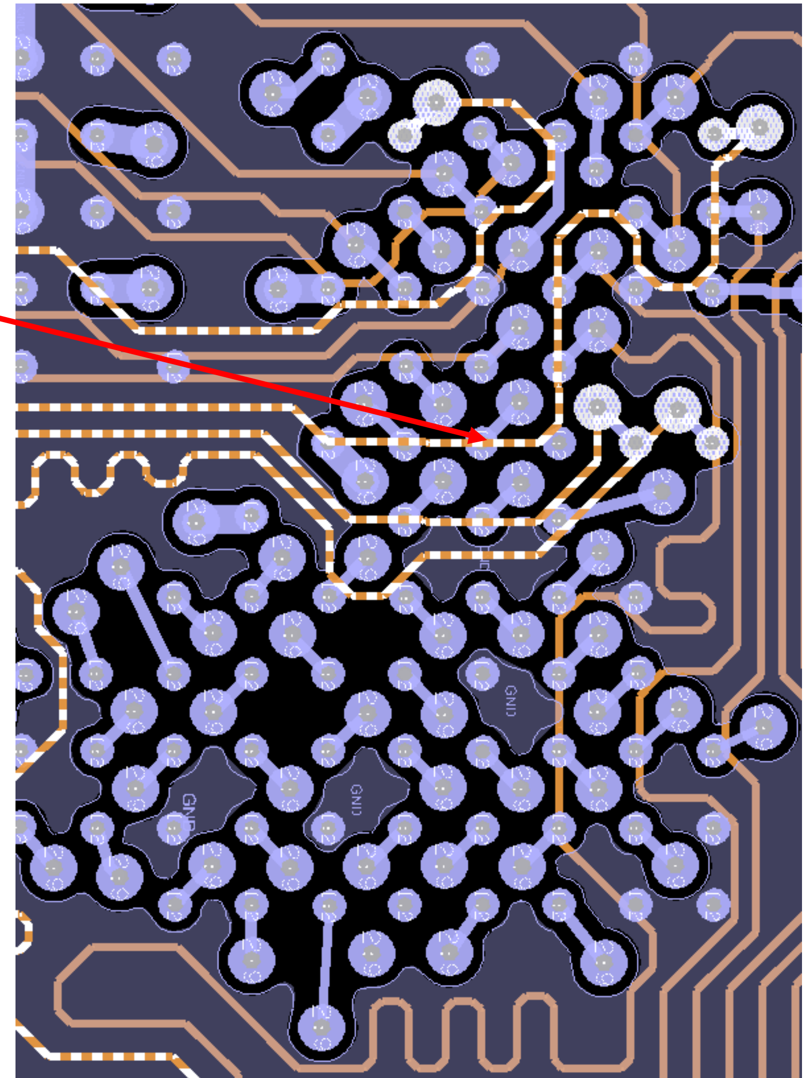


- ✅ **Remove the split in the ground plane or move the traces to a layer that has a continuous plane.**

Blind Vias: Antipads Too Large. Example 1

- DQ signals running over massive voids on Layer 2 due to blind via connections.

- Alternate the use of standard through holes with Blind Vias.

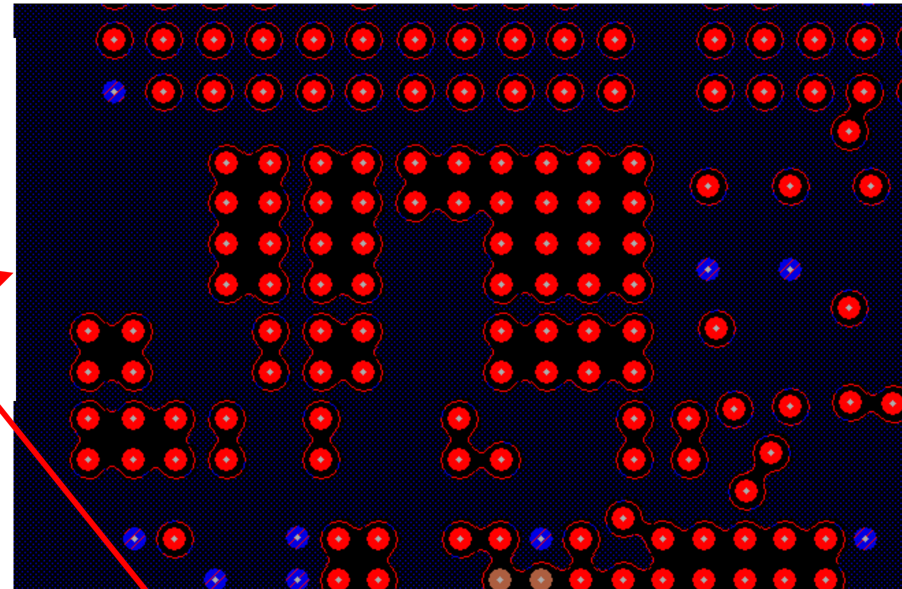


Blind Vias: Antipads Too Large. Example 2
0.8mm ball pitch

Large Joined Voids present on L5, 7,9,12,14,16.

All traces in this area will couple together.

Signals on L6,8,10,11,13, 15 all couple together

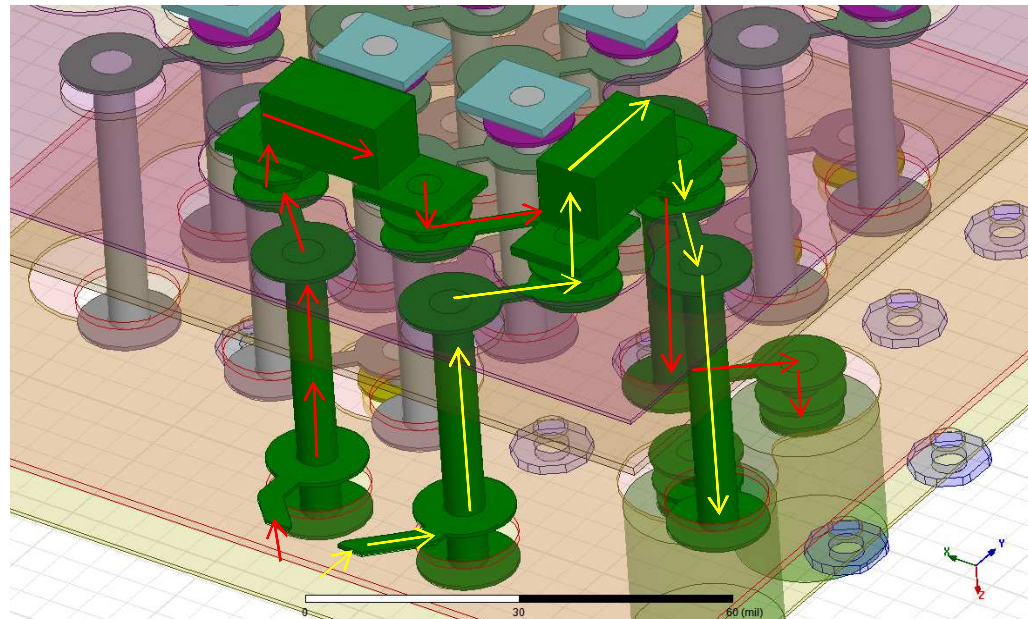


Alternate the use of standard through holes with Blind Vias.

Blind Vias: Out of Control Signal Paths

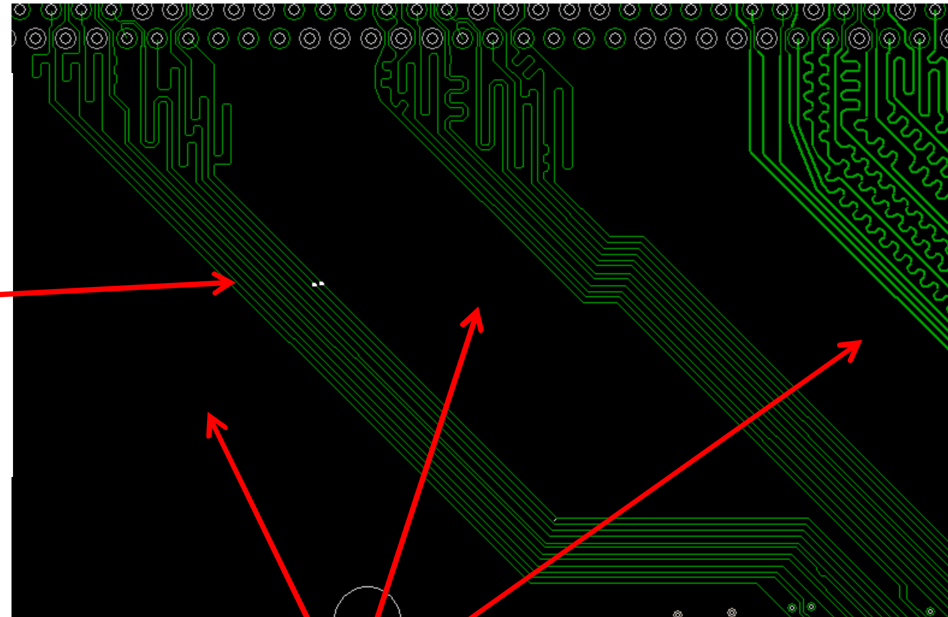
Red and Yellow signal paths are not coupled or consistent.

Ground Vias provide no isolation between signal vias throughout the board because they are Blind vias from L1-L3



Copper Utilization

Traces are routed at minimum spacing with tons of copper available on either side.



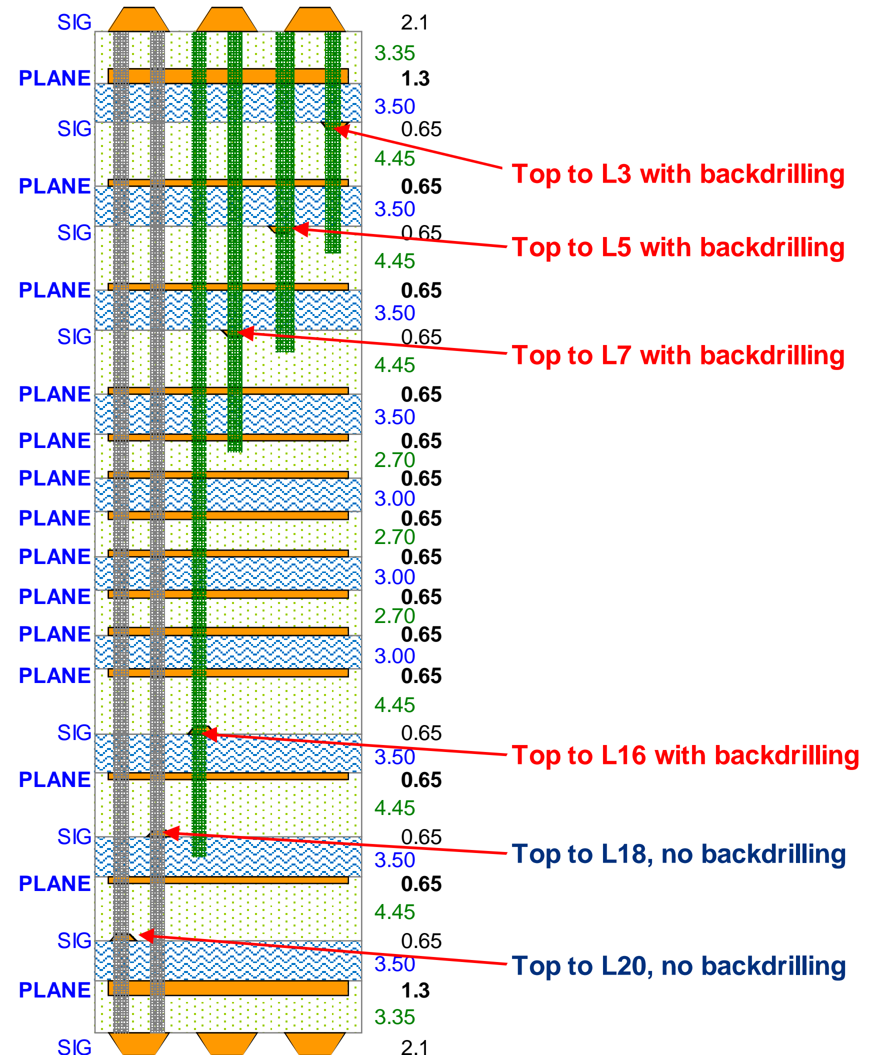
Use these unused areas

Spread Traces out to take advantage of the unused copper and reduce crosstalk in the process

Backdrilling at 6Gbps

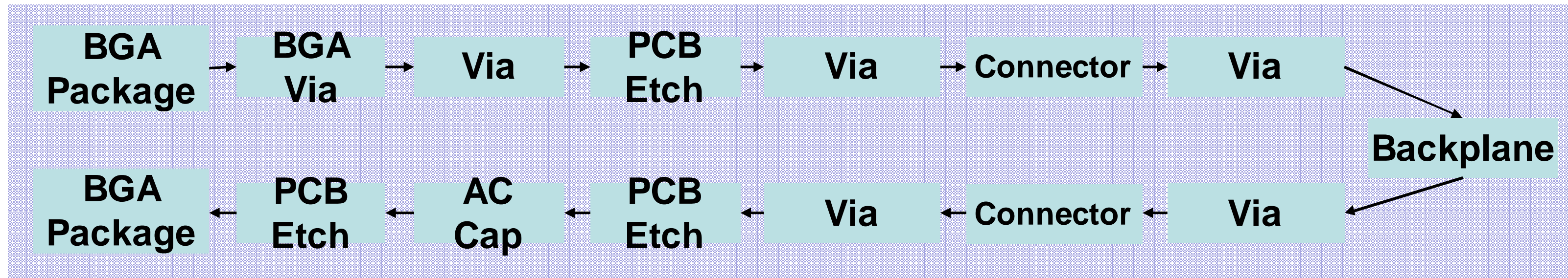
Long stubs under connecting layers cause resonance.

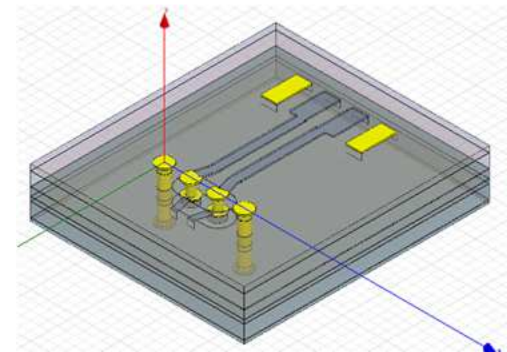
Backdrill to multiple depths keeping stubs less than 30mils (at 6Gbps)



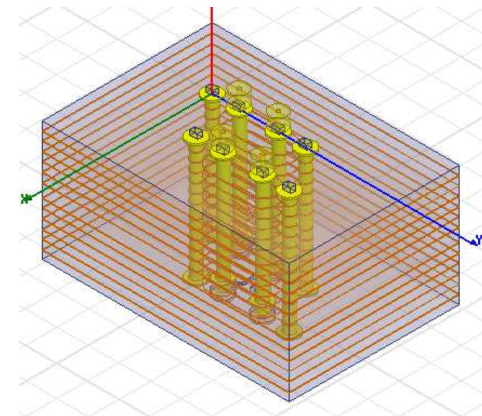
Simulation Examples and Tools

Channel Modeling - Process and Tools



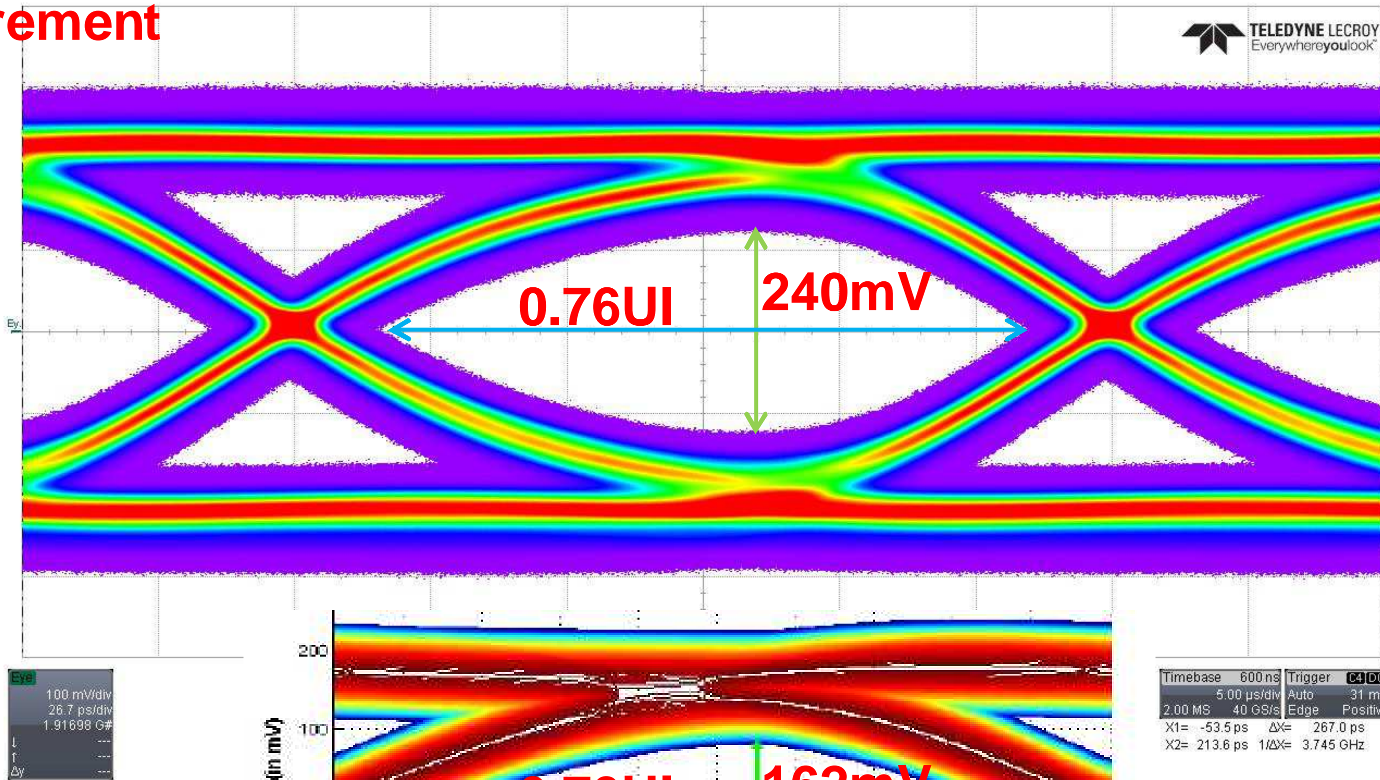


- **Channel Models** created in Hspice Or ADS
  - –S-parameters of connector, footprint, etch
- **Connector Models**
  - –Provided by Connector Vendor in Touchstone format.
- **PCB Footprints / Via Models**
  - –Simulated in Ansoft HFSS
- **PCB Etch Models**
  - –De-Embedded S-parameter Model generated in HFSS

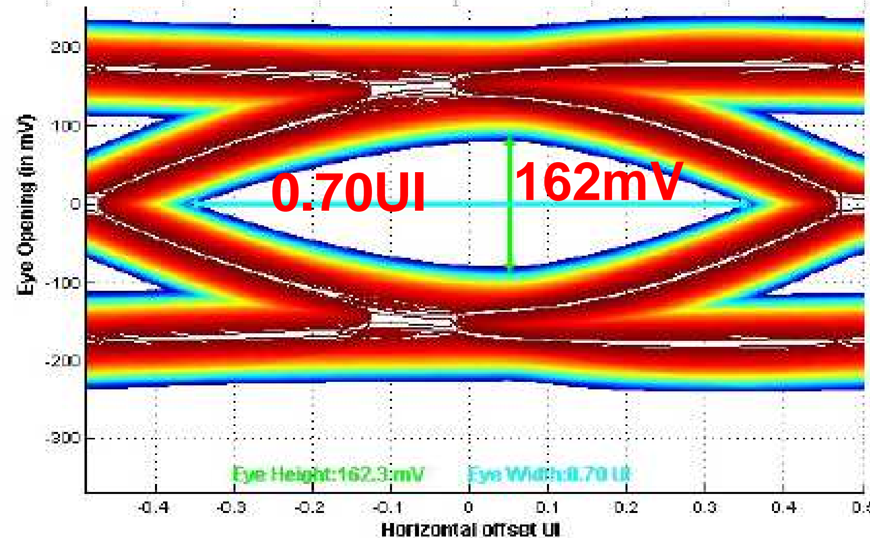


Statistical Eye: 6.25Gbps
Measurement vs. Simulation

Measurement



Simulation
(from LinkEye)



ADS Schematic:
1 Million Bit-By-Bit Simulation

Tx_AMI
Tx_AMI1
ComponentName="stratix_v_gx_tx"
PinName="10"
ModelName="stratix5_gx_tx_100_7"
DataTypeSelector=Fast
UsePkg=yes
CacType=Typ
BitRate=12.5 Gbps
Mode=Maximal Length LFSR
Taps="10001110"
Seed="10101010"
BitSequence="10101010"
NumberTimePtPerUI=
AMIvarName[1]=Ignore_Bits
AMIvarName[2]=Max_Init_Aggressors
AMIvarName[3]=Init_Returns_Impulse
AMIvarName[4]=Use_Init_Output
AMIvarName[5]=GetWave_Exists
AMIvarName[6]=lvod
AMIvarName[7]=tap1
AMIvarName[8]=tap2
AMIvarName[9]=pretap
AMIvarName[10]=invtap2
AMIvarName[11]=invpretap
AMIvarName[12]=protocol
AMIvarName[13]=slew
AMIvarName[14]=Rterm
AMIvarName[15]=Process
AMIvarName[16]=Debug
AMIvarValue[1]=4
AMIvarValue[2]=0
AMIvarValue[3]=True
AMIvarValue[4]=False
AMIvarValue[5]=True
AMIvarValue[6]=7
AMIvarValue[7]=10
AMIvarValue[8]=0
AMIvarValue[9]=8
AMIvarValue[10]=0
AMIvarValue[11]=0
AMIvarValue[12]=0
AMIvarValue[13]=0
AMIvarValue[14]=100
AMIvarValue[15]=0
AMIvarValue[16]="none"

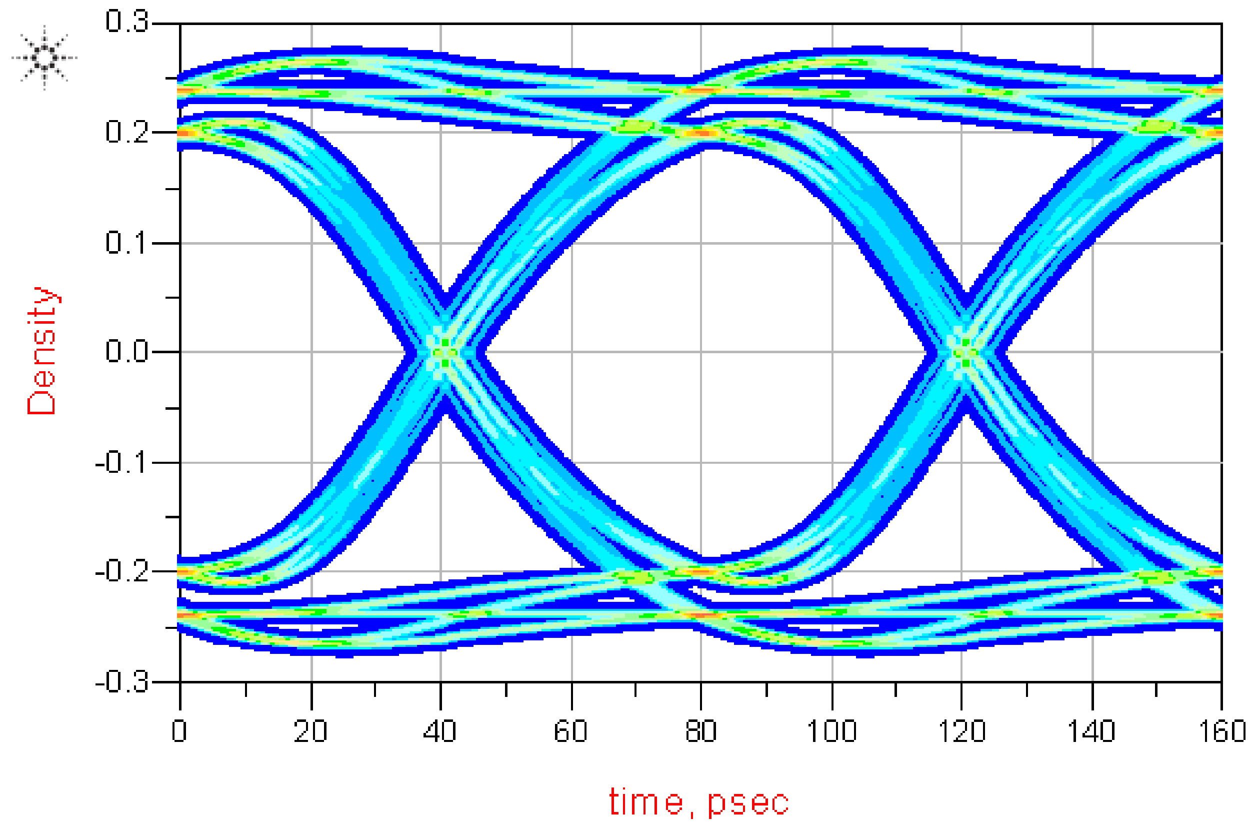
ChannelSim
ChannelSim
ChannelSim1
NumberOfBits=1000000
ToleranceMode=Auto
EnforcePassivity=yes

Eye_Probe
Eye_Probe1
RxAMI
TxAMI

Rx_AMI
Rx_AMI2
ComponentName="ibm_hss15c2c_cu032_nc"
PinName="2p"
ModelName="ibm_hss15c2c_cu032_rx_nc"
SetAllData=yes
DataTypeSelector=Typ
UsePkg=yes
CacType=Typ
AMIvarName[1]=Ignore_Bits
AMIvarName[2]=Max_Init_Aggressors
AMIvarName[3]=Init_Returns_Impulse
AMIvarName[4]=GetWave_Exists
AMIvarName[5]=Use_Init_Output
AMIvarName[6]=Rx_Clock_PDF
AMIvarName[7]=Rx_Receiver_Sensitivity
AMIvarName[8]=baud

thru_channel_s4p_40
X1
AMIvarName[9]=sjrx
AMIvarName[10]=sjrx_freq
AMIvarName[11]=anvga
AMIvarName[12]=gain
AMIvarName[13]=negz
AMIvarName[14]=VTR
AMIvarName[15]=H1limit
AMIvarName[16]=Fc1667
AMIvarName[17]=rxcte
AMIvarName[18]=rxic
AMIvarName[19]=rxh
AMIvarName[20]=Rx_Rj
AMIvarName[21]=agcgain
AMIvarName[22]=agcmax
AMIvarName[23]=agcmin
AMIvarName[24]=agclev
AMIvarName[25]=rotlin
AMIvarName[26]=ndfe
AMIvarName[27]=dfelimit
AMIvarName[28]=freqofs
AMIvarName[29]=dfeadaptoff
AMIvarName[30]=dfeoff
AMIvarName[31]=wavecap
AMIvarName[32]=ADS_VendorID
AMIvarValue[1]=40000
AMIvarValue[2]=0
AMIvarValue[3]=False
AMIvarValue[4]=True
AMIvarValue[5]=False
AMIvarValue[6]=0,0.00696
AMIvarValue[7]=0.013
AMIvarValue[8]=12.5e9
AMIvarValue[9]=0.05
AMIvarValue[10]=1.54e8
AMIvarValue[11]=2.0335e-3
AMIvarValue[12]="mid"
AMIvarValue[13]=0
AMIvarValue[14]=1.05
AMIvarValue[15]=3
AMIvarValue[16]=0
AMIvarValue[17]="ibm/hss15c2c/cu032/ic_rx_ncAVTR1_05negzen0gain_dec255.cte.ami"
AMIvarValue[18]="ibm/hss15c2c/cu032/ncAVTR1_05negzen0gain_dec255peak_dec0_norm.s4p"
AMIvarValue[19]=0
AMIvarValue[20]=420e-15
AMIvarValue[21]=0.0

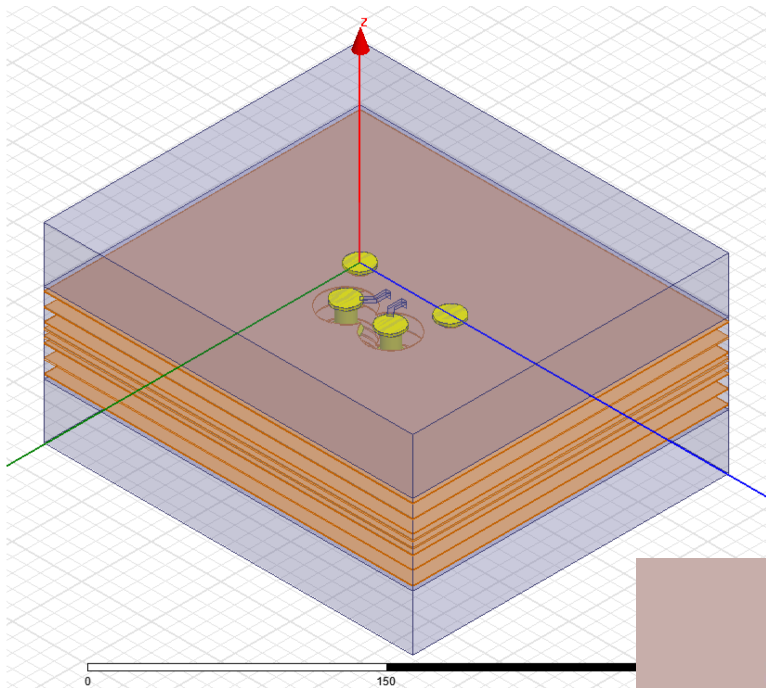
Statistical Eye: 12.5Gbps
1 Million Bit-By-Bit Simulation

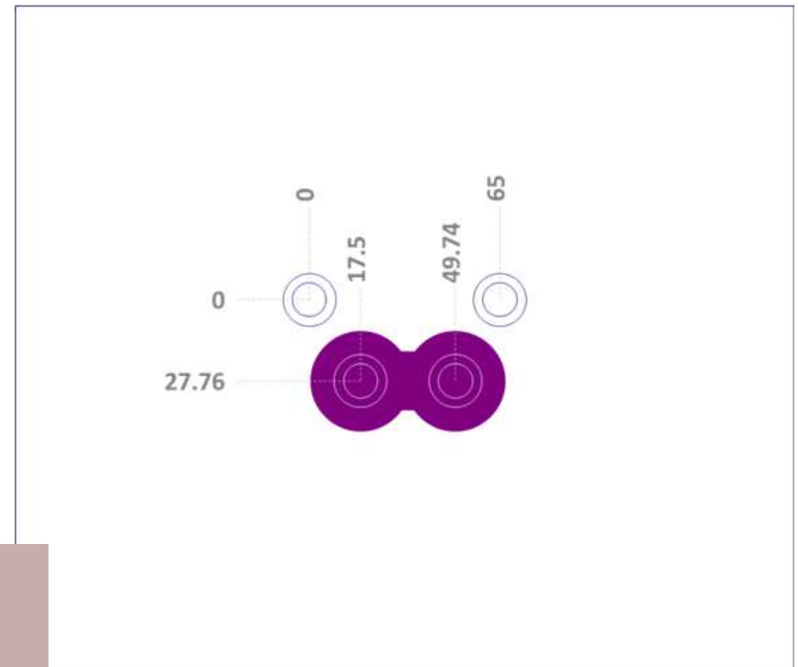


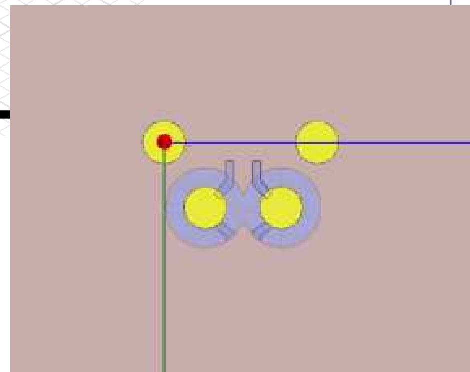
Amplitude: 336mV
Width: 63ps
Width: 0.79UI

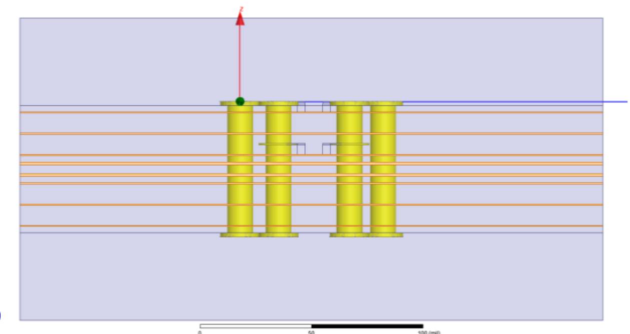
Via Model Example: Return Loss Improvements

Via Model: Transition Via As Designed



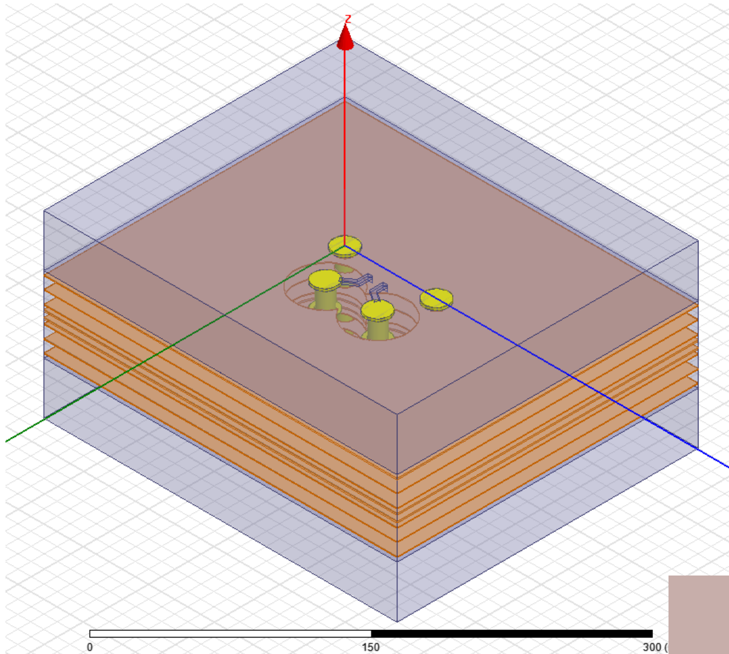


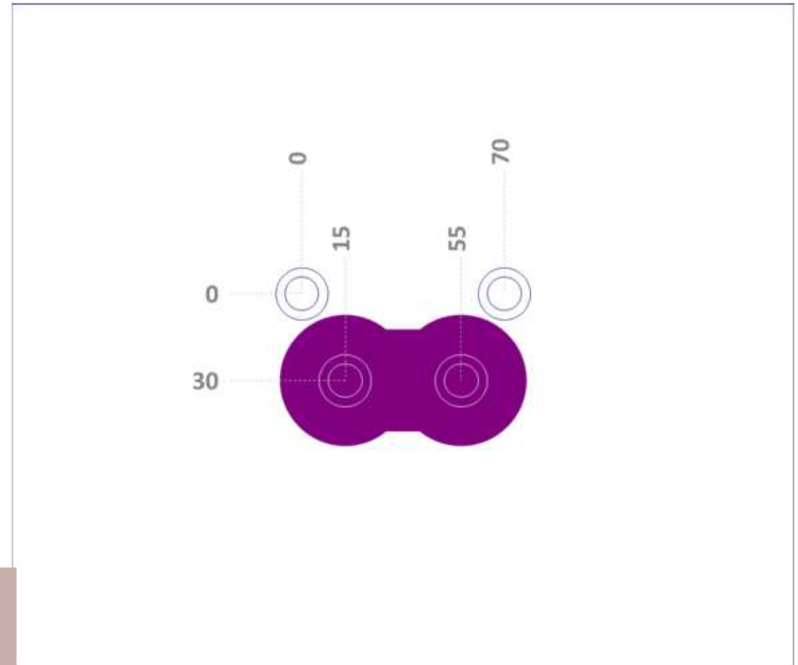


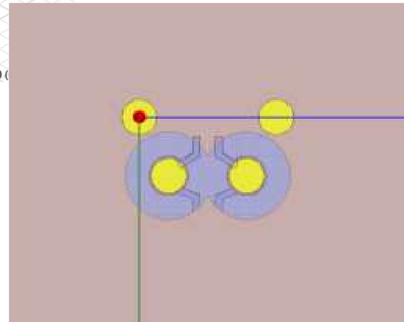


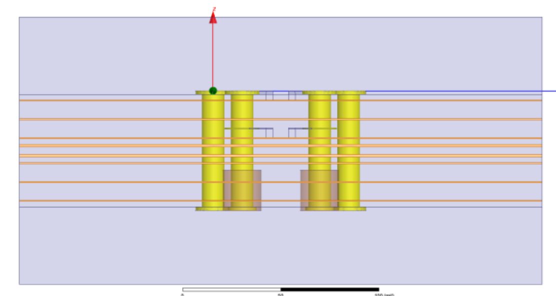
Finished Dia	8.0mil	Diff Port Zo	100	Material	EM888
Drill Dia	11.7mil	Layer Escape	1 and 5	Dk	3.5
Pad Dia	18.0mil	Line Width	3.50mil	Df	0.008
Antipad Dia	34.0mil	EtchBack	0.1mil	Layers	14
Oval Dogbone	20.0mil	Line Space	8.0mil	Thickness	61.5 mil

Via Model: Transition Via Modified



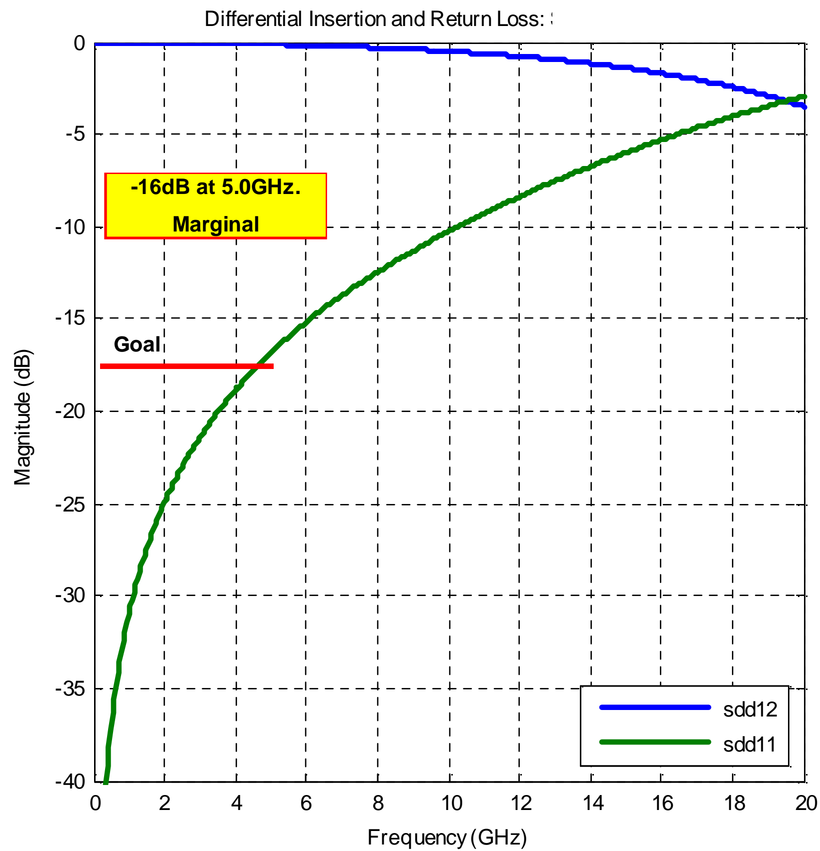


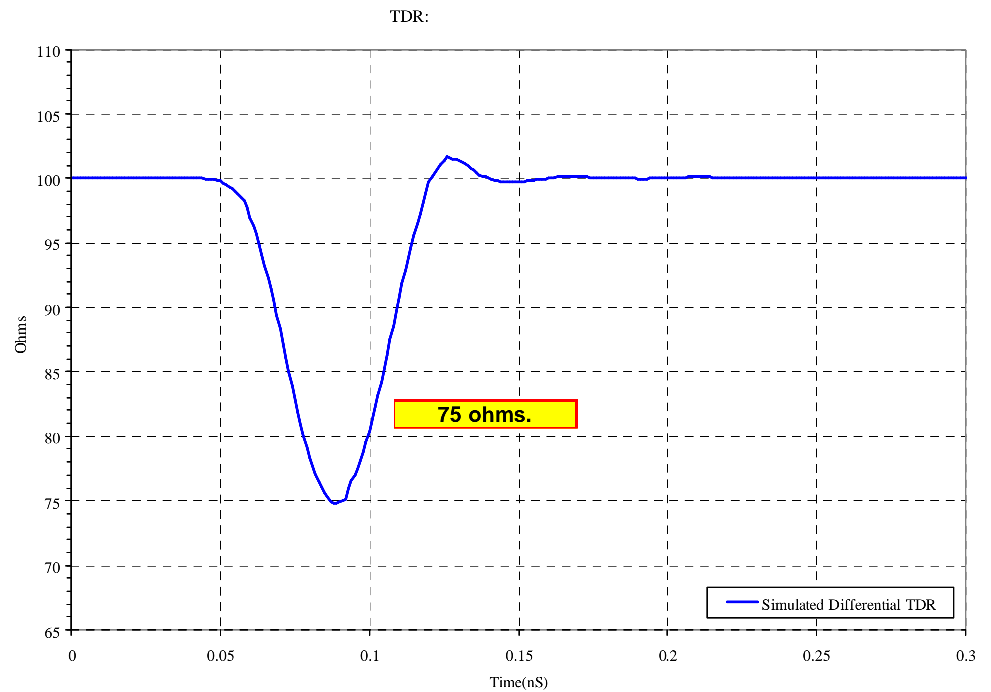




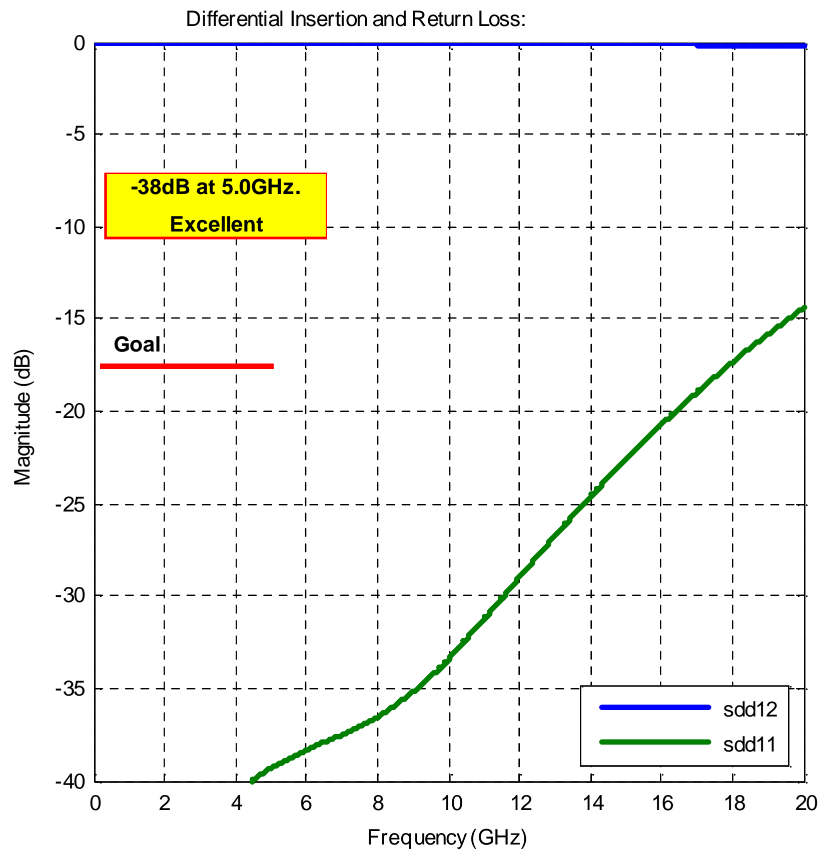
Finished Dia	8.0mil			Diff Port Zo	100	Material	EM888
Drill Dia	11.7mil			Layer Escape	1 and 5	Dk	3.5
Pad Dia	18.0mil	Default Stub	20.0mil	Line Width	3.50mil	Df	0.008
Antipad Dia	45.0mil	Backdrill Dia	20.0mil	EtchBack	0.1mil	Layers	14
Oval Dogbone	35.0mil	Backdrill Hole?	Yes	Line Space	8.0mil	Thickness	61.5 mil

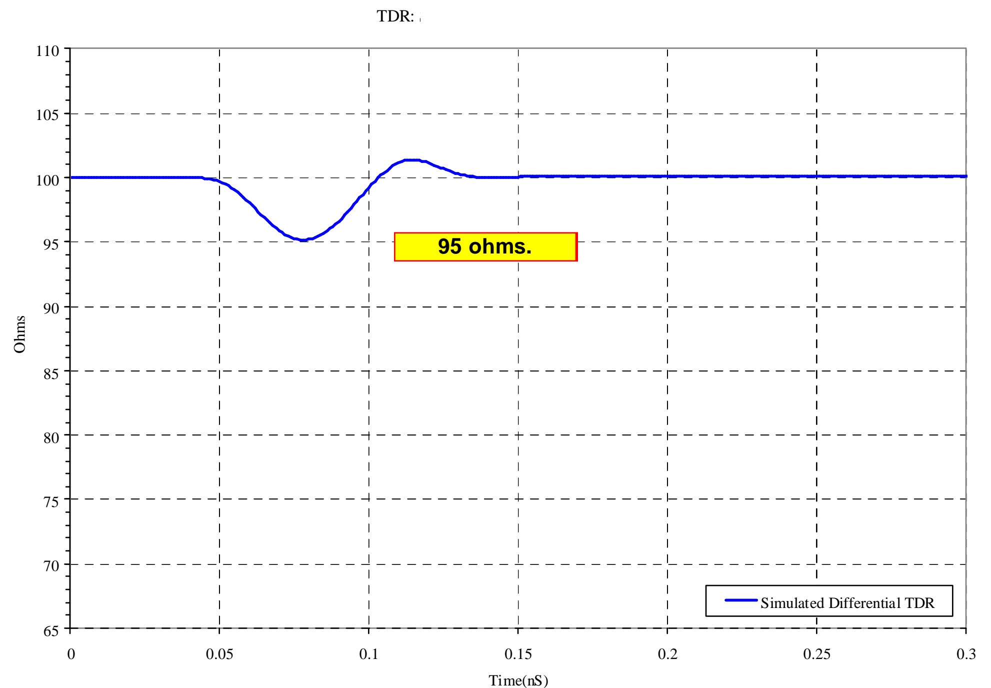
IL, RL and TDR: Transition Via As Designed



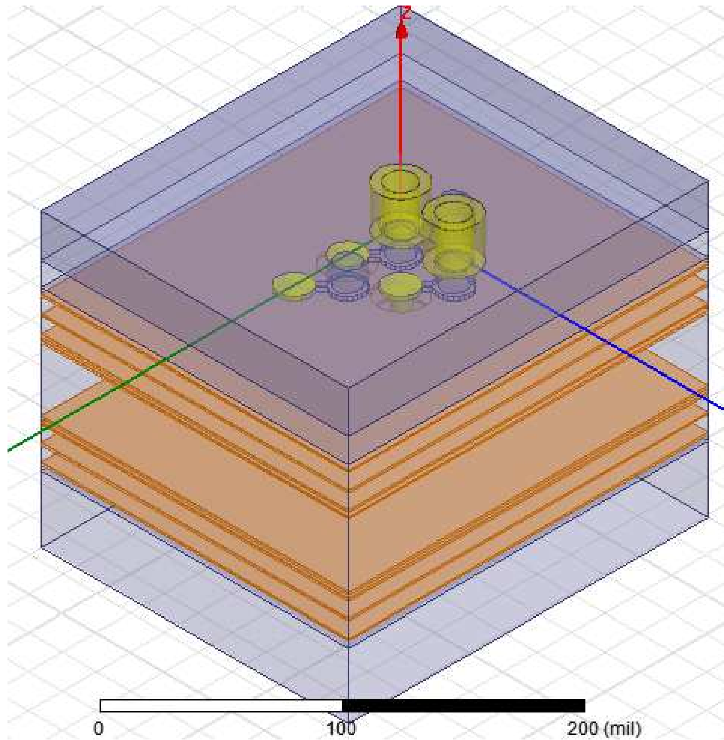


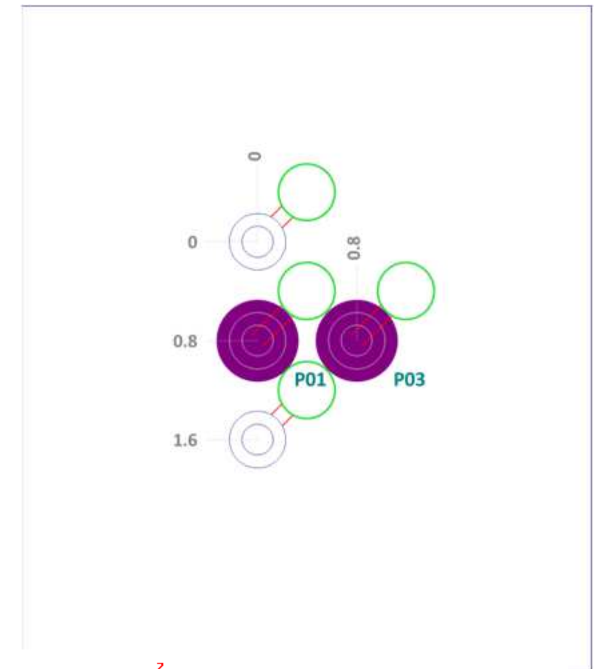
IL, RL and TDR: Transition Via Modified

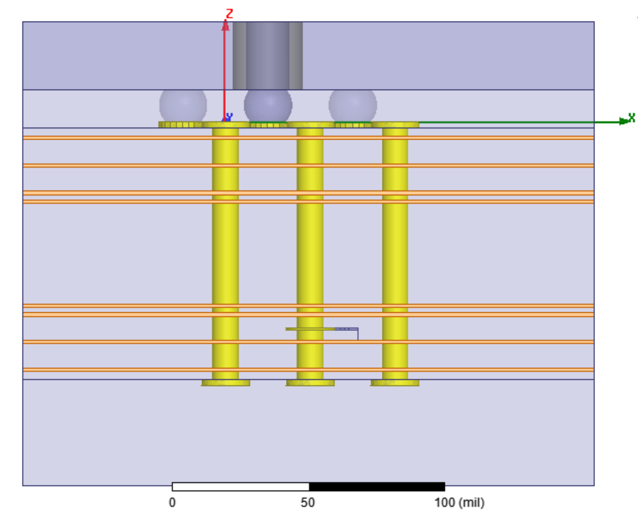




Via Model: 0.8mm BGA



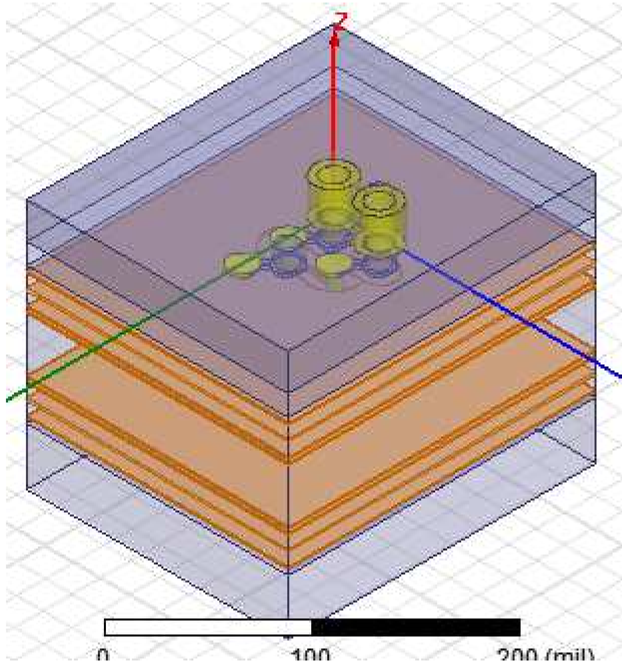


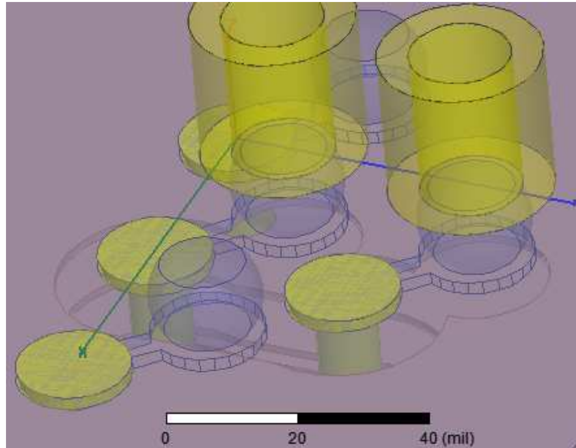


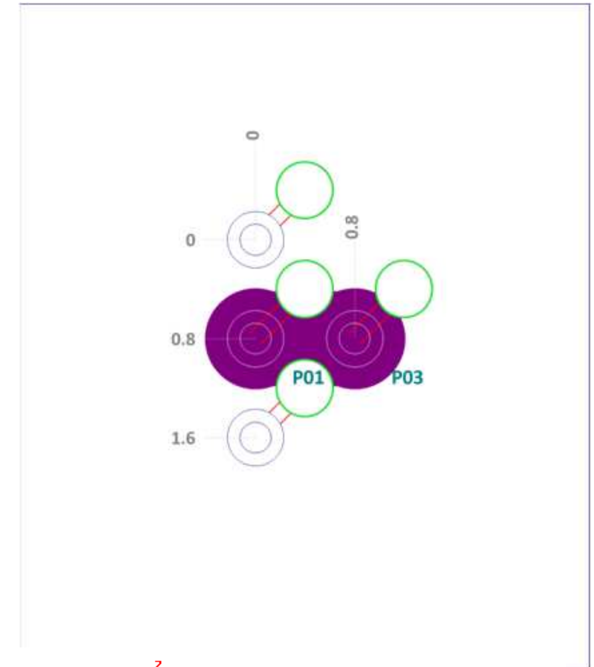
		Diff Port Zo	100	Material	FR408HR		
Finished Dia	6.0mil	Layer Escape	10	Dk	3.86		
Drill Dia	9.8mil	Line Width	3.45mil	Df	0.0147		
Pad Dia	18.0mil	EtchBack	0.1mil	Layers	14	Max Freq.	20 GHz
Antipad Dia	26.0mil	Line Space	4.6mil	Thickness	98.0 mil	Adapt Freq.	10 GHz

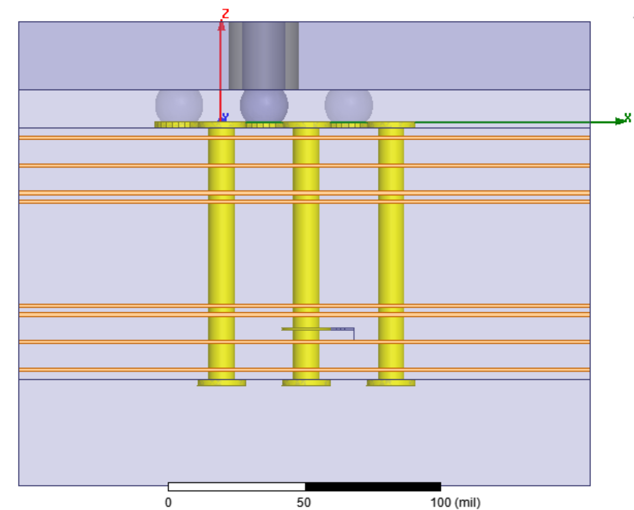
Via Model: 0.8mm BGA-R1

With 32/30 Antipad and 22mil clearance under BGA Pads





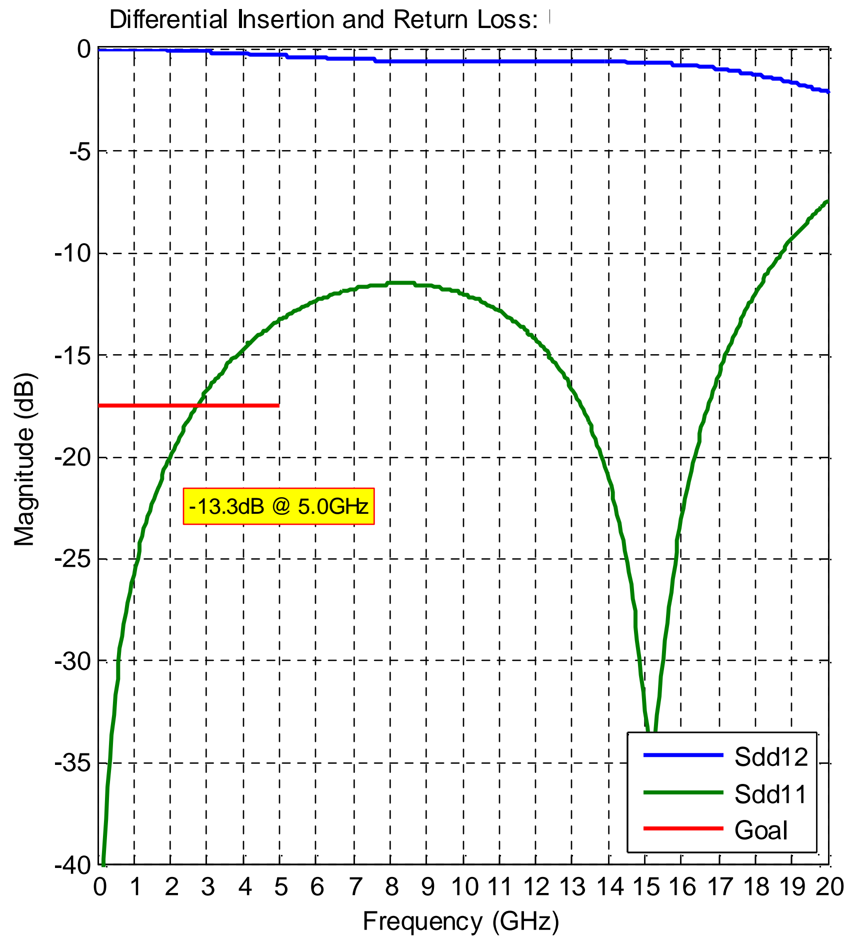


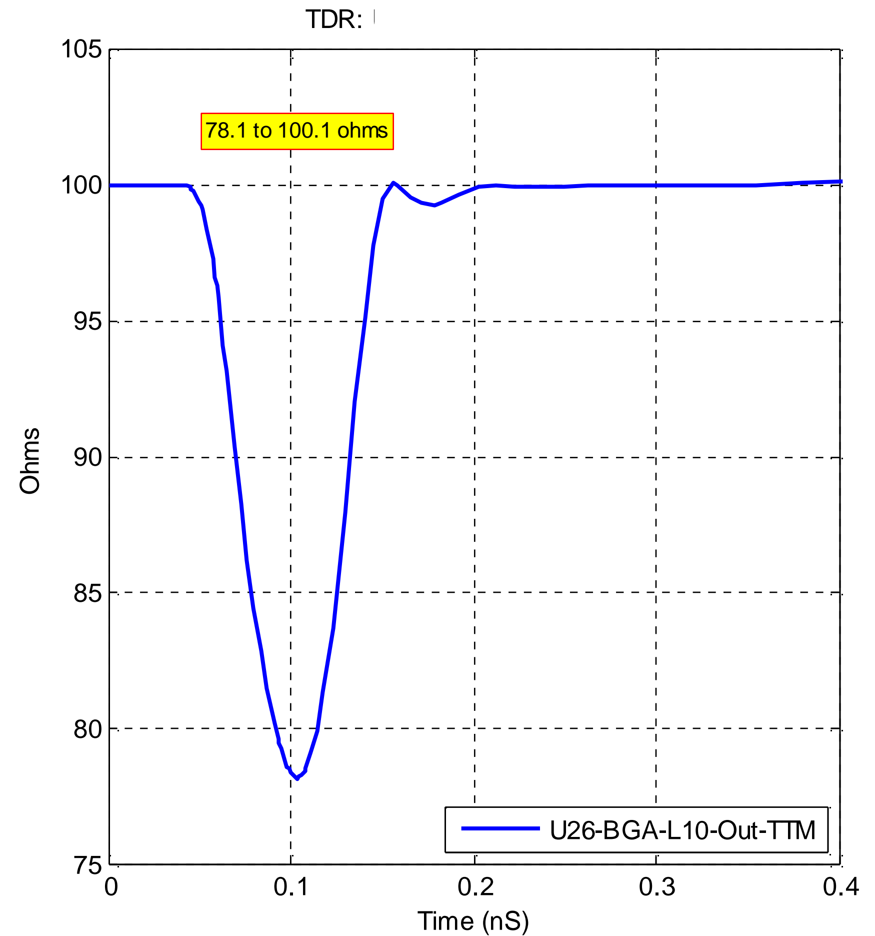


Finished Dia	6.0mil	Diff Port Zo	100	Material	FR408HR		
Drill Dia	9.8mil	Layer Escape	10	Dk	3.86		
Pad Dia	18.0mil	Line Width	3.45mil	Df	0.0147		
Antipad Dia	32.0mil	EtchBack	0.1mil	Layers	14	Max Freq.	20 GHz
Oval Dogbone	30.0mil	Line Space	31.5mil	Thickness	98.0 mil	Adapt Freq.	10 GHz

IL, RL and TDR: 0.8mm BGA

This is not acceptable performance at 10Gbps

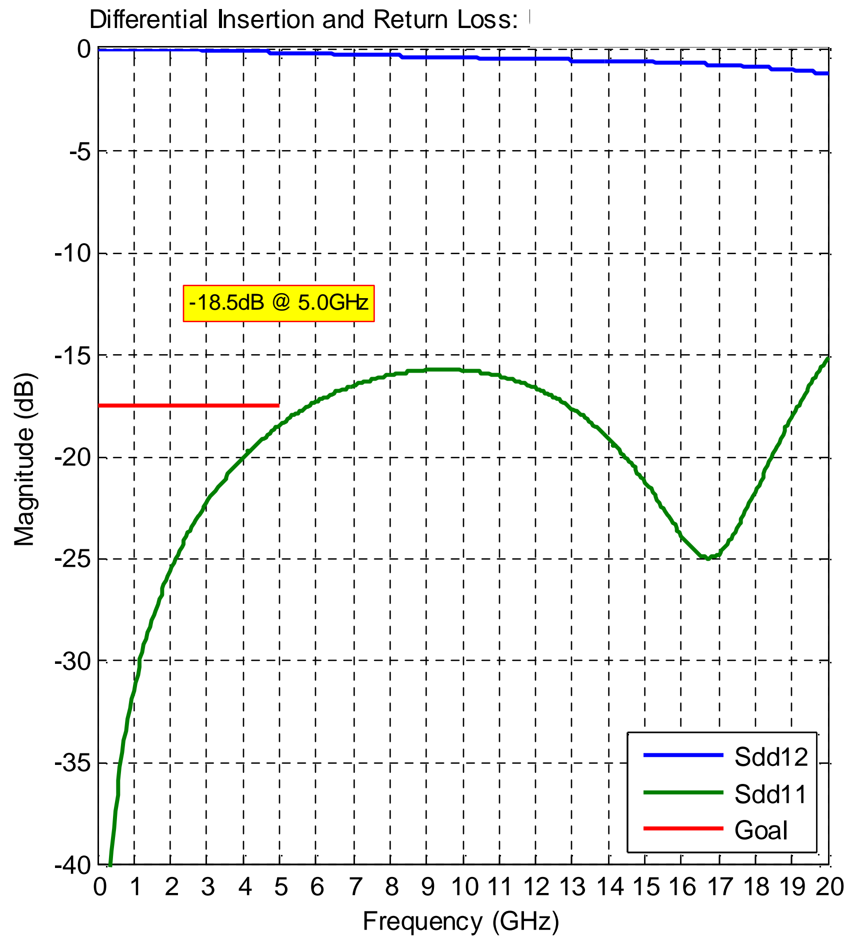


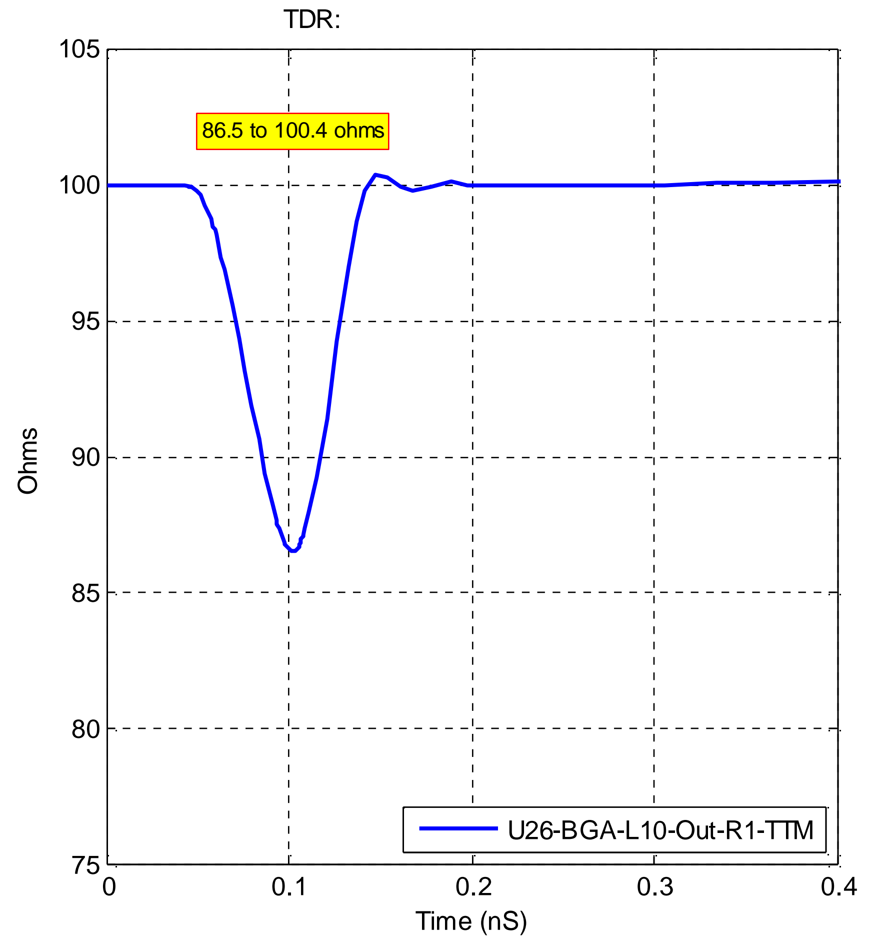


IL, RL and TDR: 0.8mm BGA-R1

With 32/30 Antipad and 22mil clearance under BGA Pads

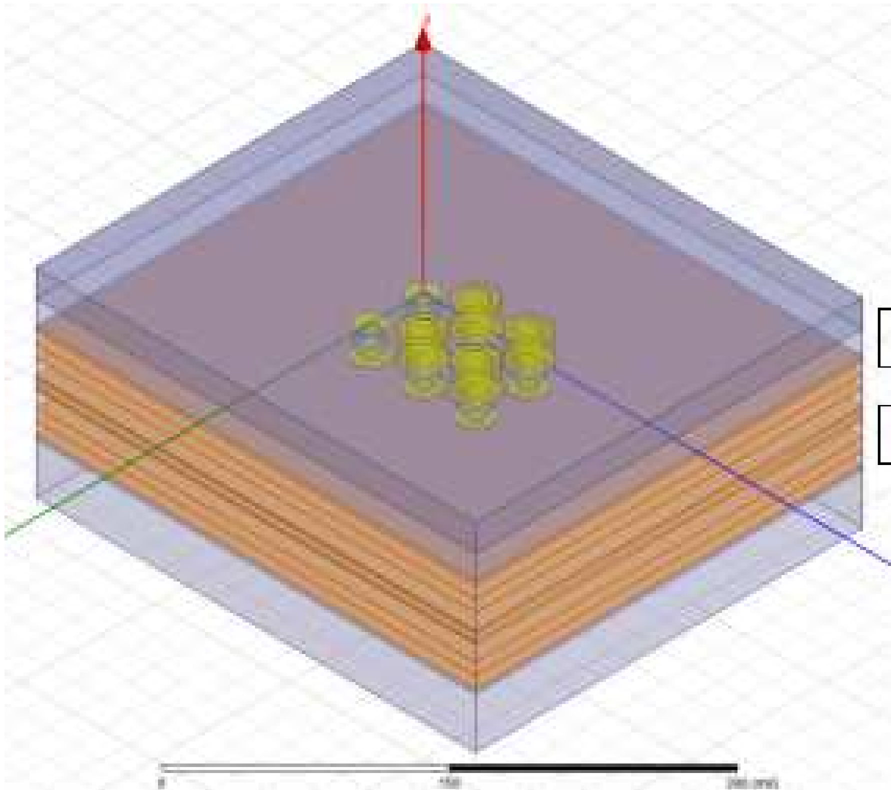
This is acceptable.



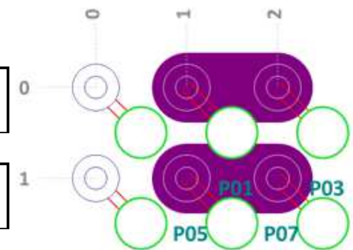


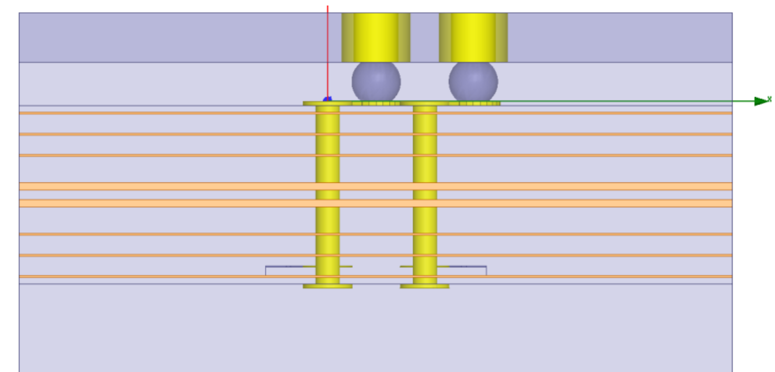
Via Model Example: Alternating Layers

Via Model: BGA-L14



Layer 14	Rx (Victim)
Layer 14	Rx1

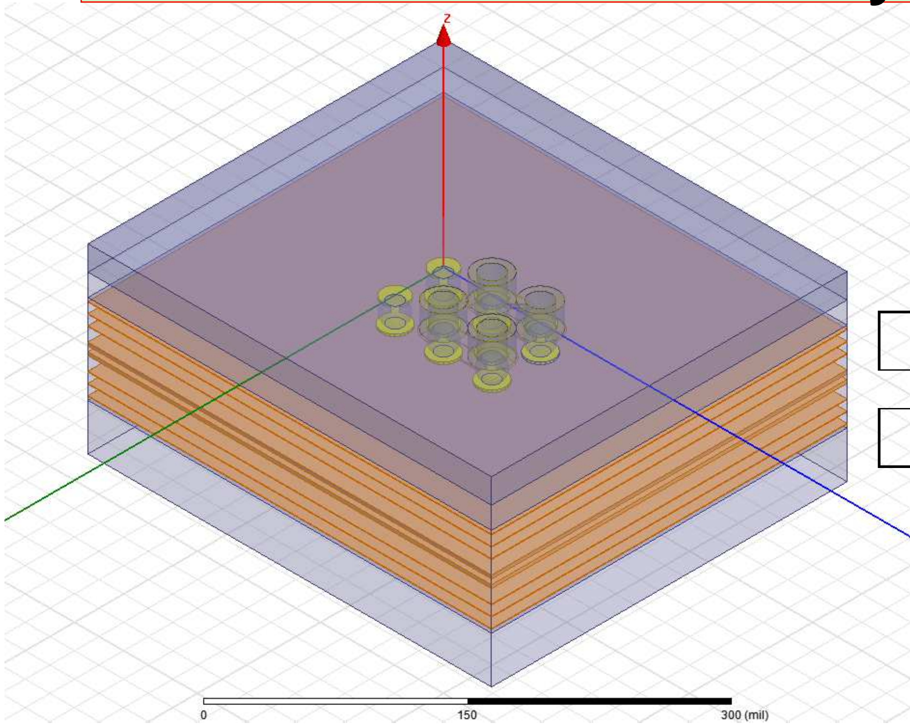




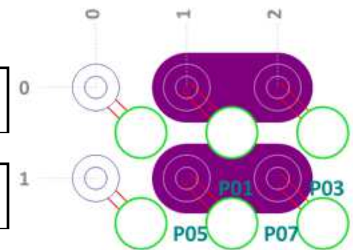
Finished Dia	6.0mil	Diff Port Zo	95	Material	N4000-13-SI		
Drill Dia	9.8mil	Layer Escape	14	Dk	3.35		
Pad Dia	20.0mil	Line Width	3.90mil	Df	0.011		
Antipad Dia	30.0mil	EtchBack	0.1mil	Layers	16	Max Freq.	40 GHz
Oval Dogbone	30.0mil	Line Space	6.0mil	Thickness	76.0 mil	Adapt Freq.	20 GHz

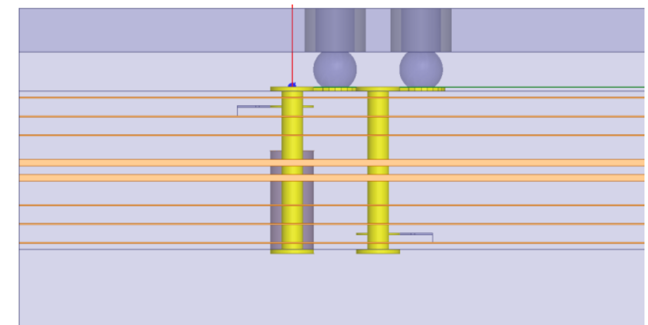
chris.heard100@gmail.com. 603-494-9277

Via Model: BGA-L14-R1
Alternate layer assignments



Layer 3	Rx (Victim)
Layer 14	Rx1

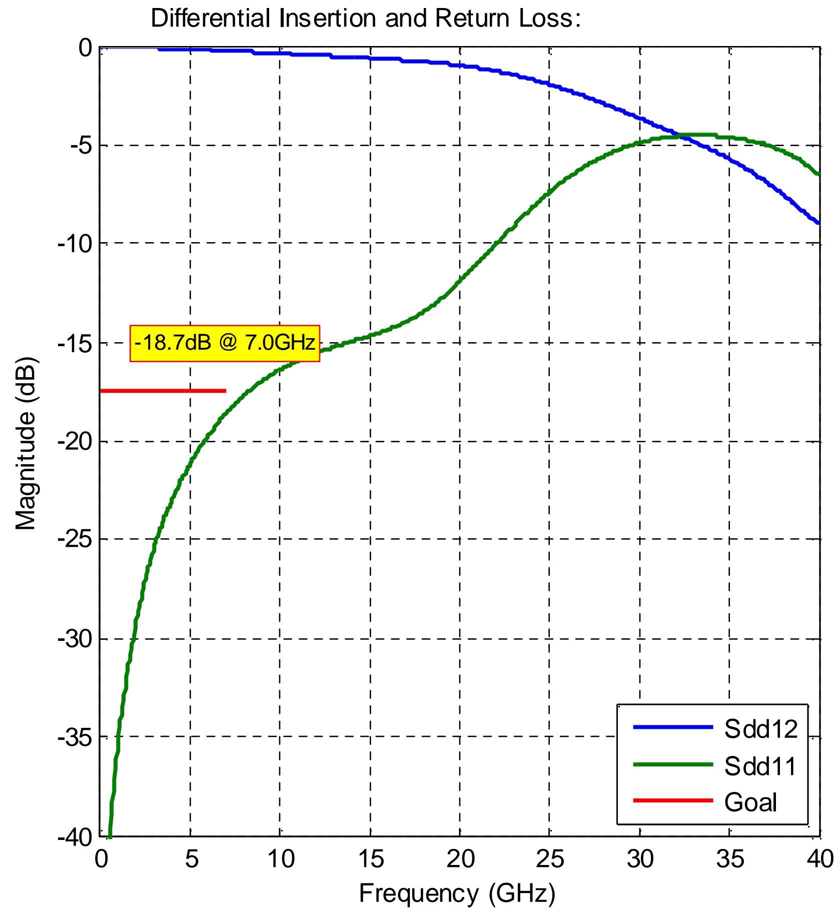


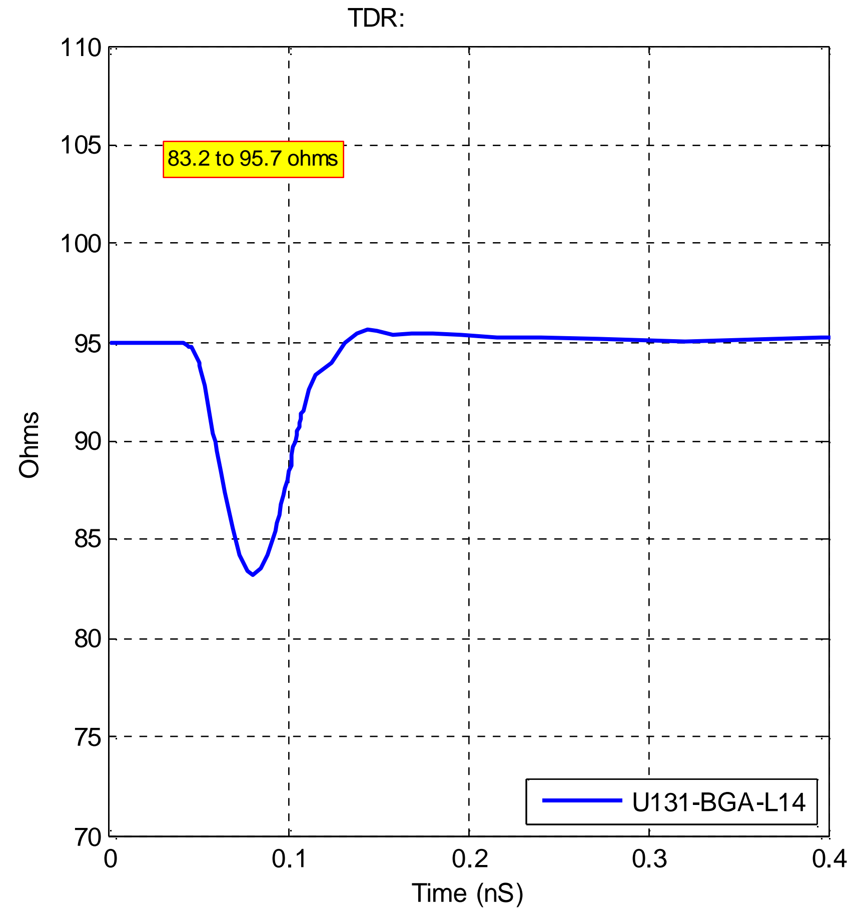


Finished Dia	6.0mil			Diff Port Zo	95	Material	N4000-13-SI		
Drill Dia	9.8mil			Layer Escape	3 and 14	Dk	3.35		
Pad Dia	20.0mil	Default Stub	20.0mil	Line Width	3.90mil	Df	0.011		
Antipad Dia	30.0mil	Backdrill Dia	20.0mil	EtchBack	0.1mil	Layers	16	Max Freq.	40 GHz
Oval Dogbone	30.0mil	Backdrill Hole?	Yes	Line Space	6.0mil	Thickness	76.0 mil	Adapt Freq.	20 GHz

IL, RL and TDR: BGA L14

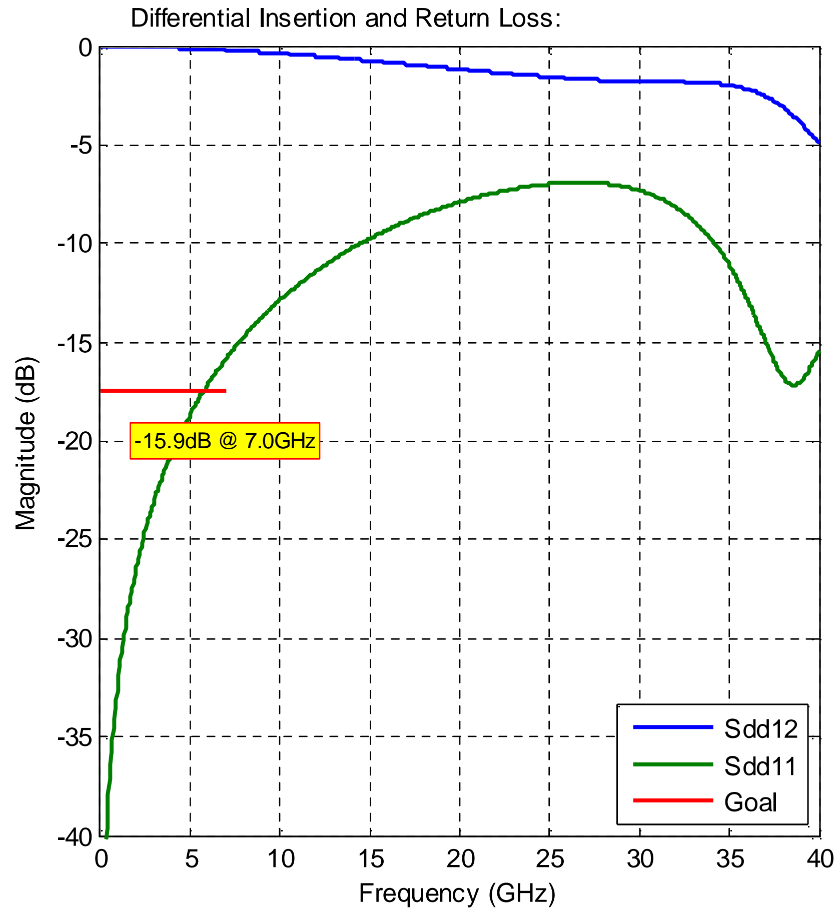
Bottom Layer Has Great Return Loss

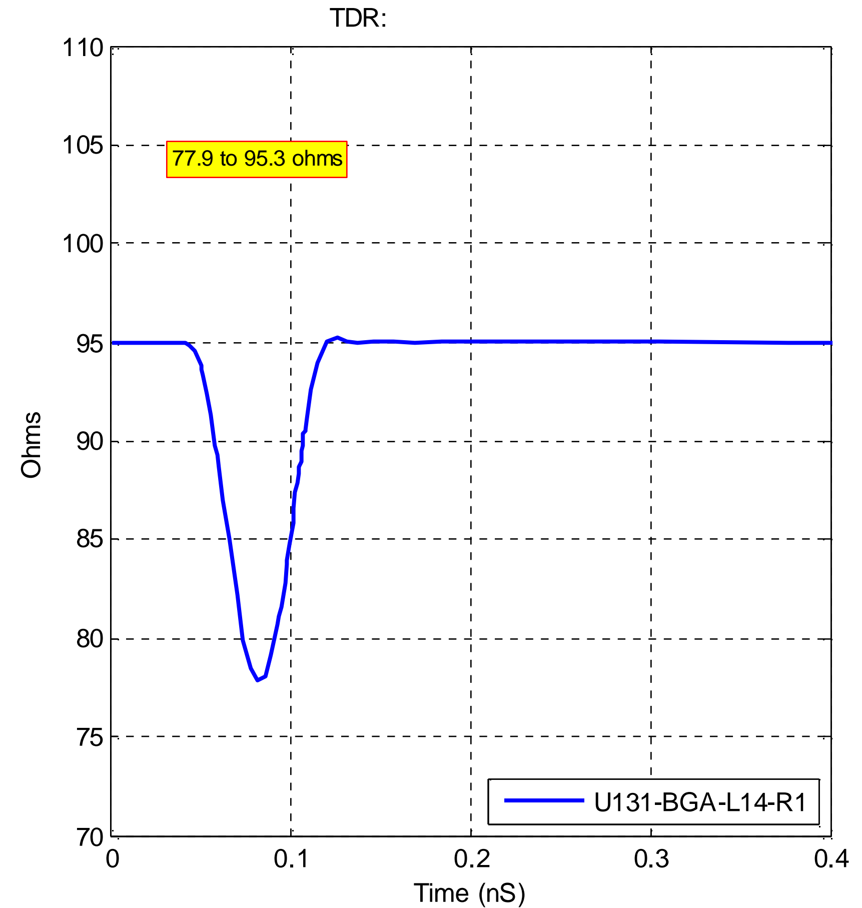




IL, RL and TDR: BGA L14 R1

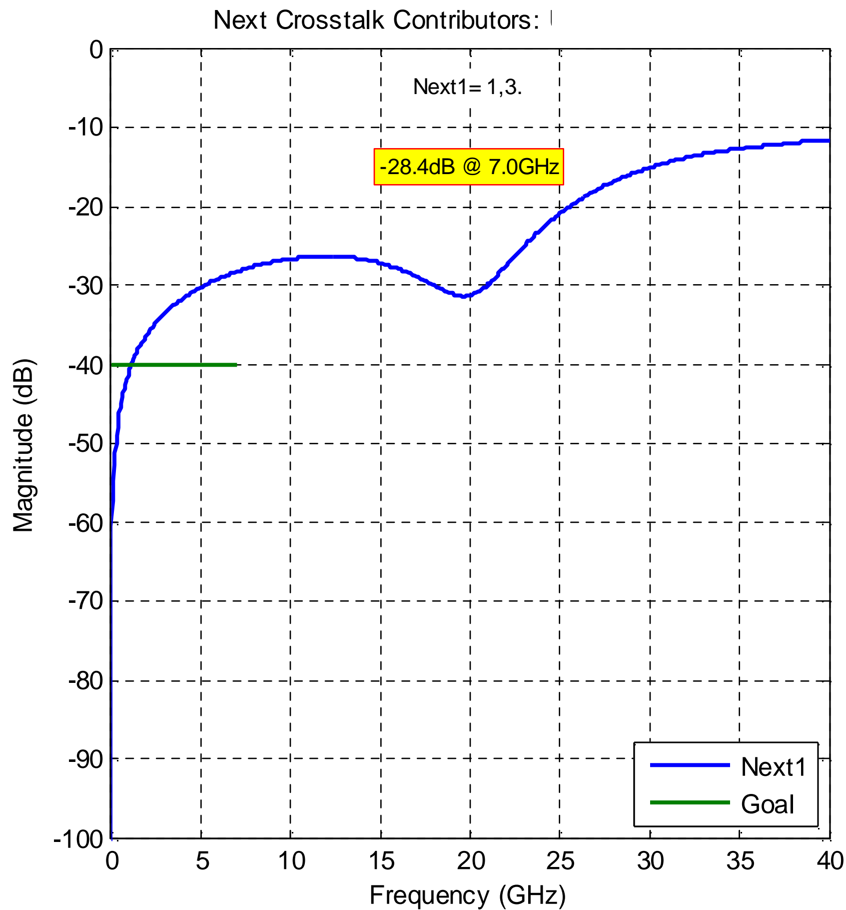
Layer 3 with Backdrilled Stub a Lower Impedance

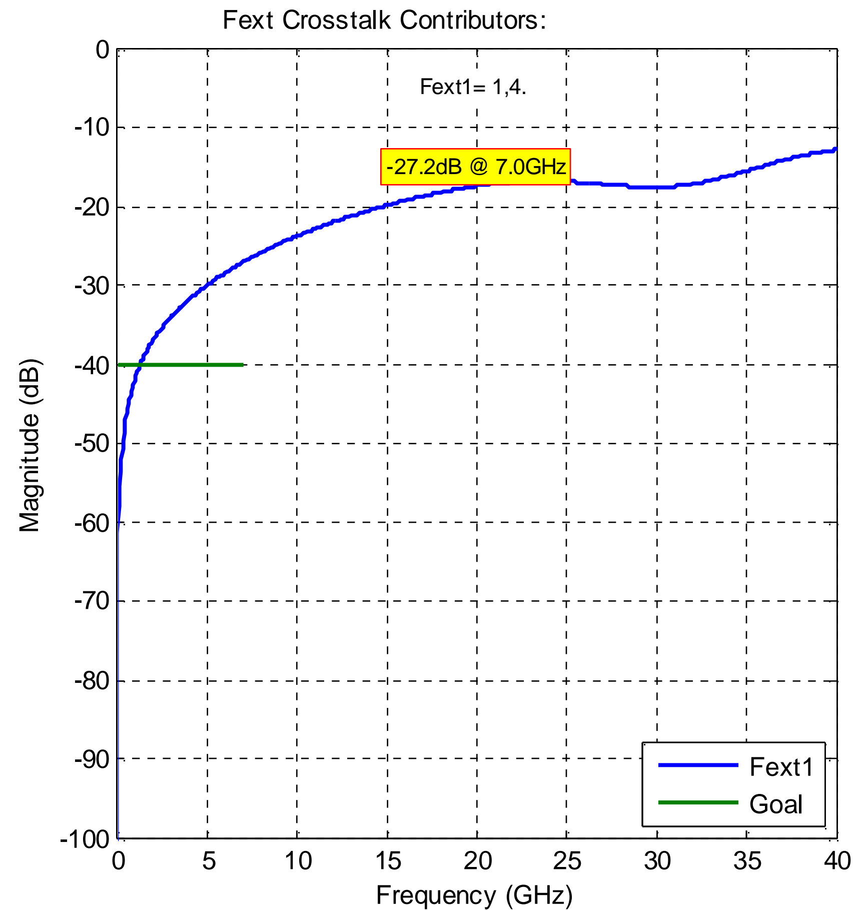




Next and Fext: BGA L14

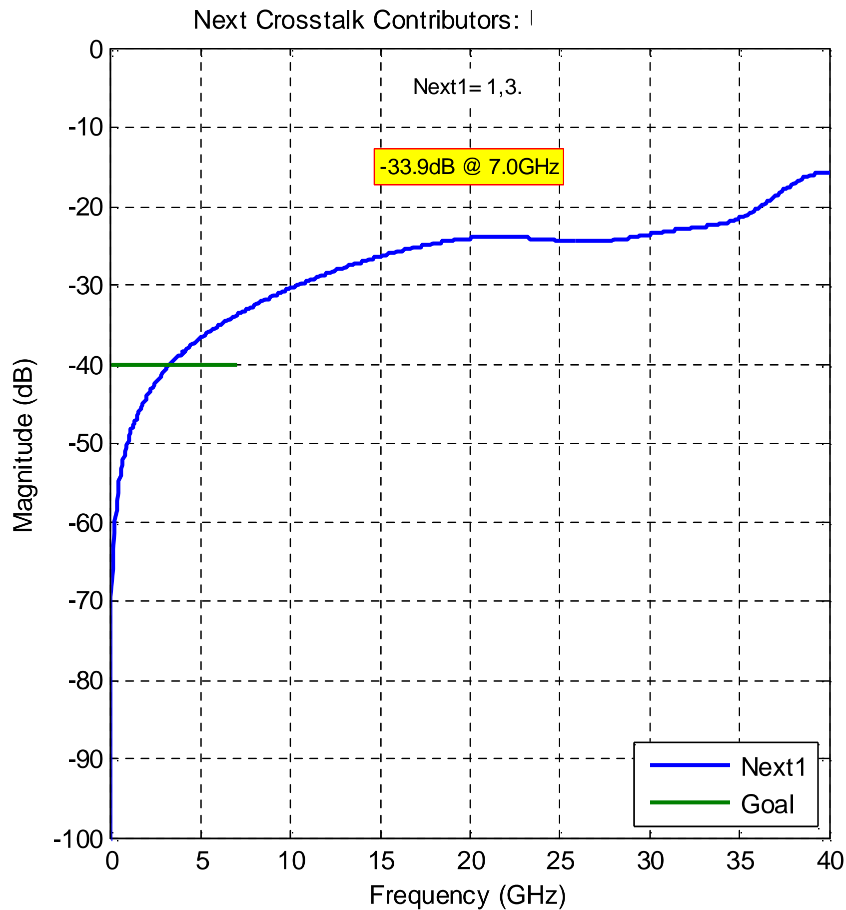
Crosstalk between the Vias is high.

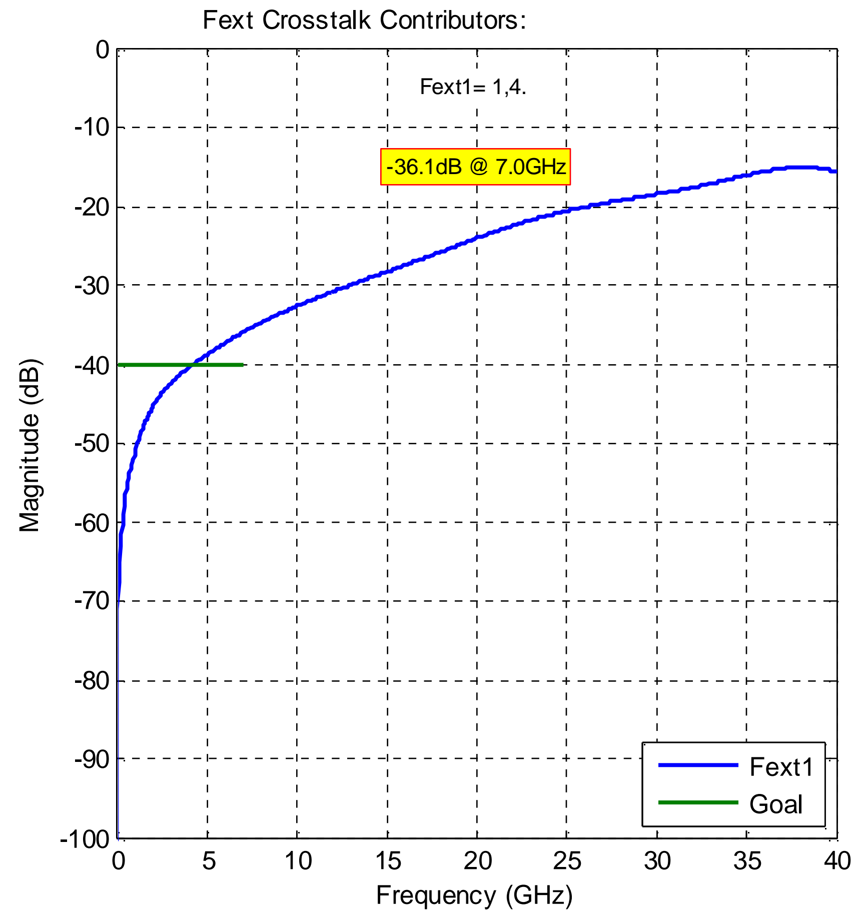




Next and Fext: BGA L14 R1

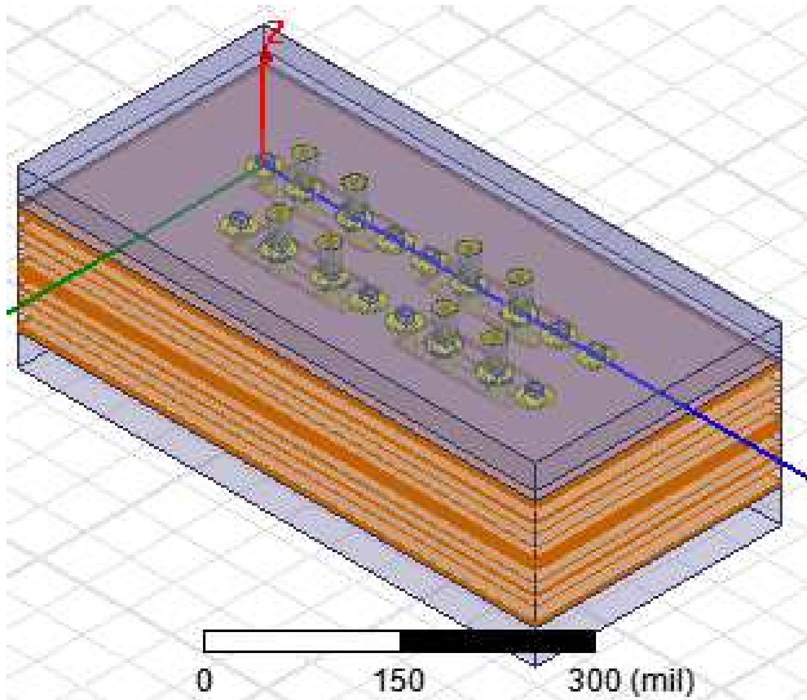
9dB (2.8x) Reduction in FEXT

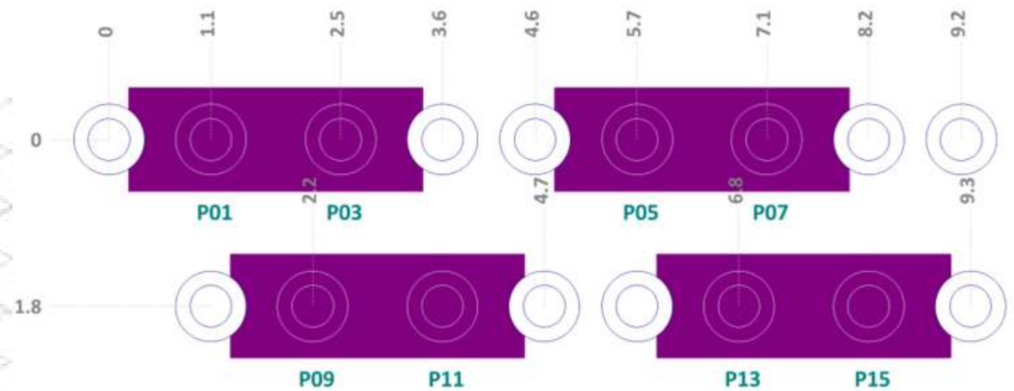


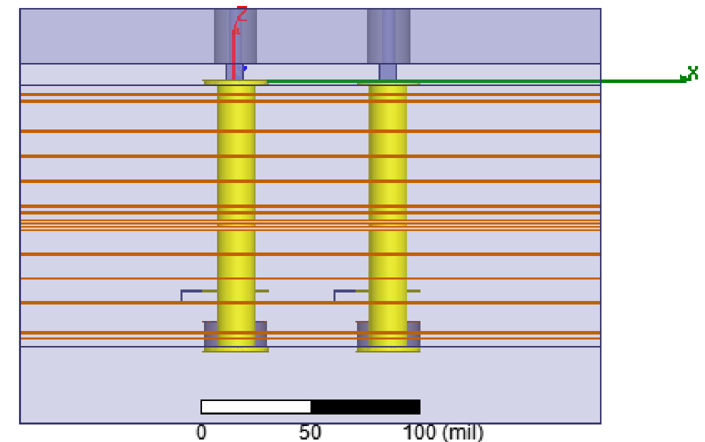


Via Model Example:
Very Low Crosstalk

Via Model: Amphenol XCedeHDPlus

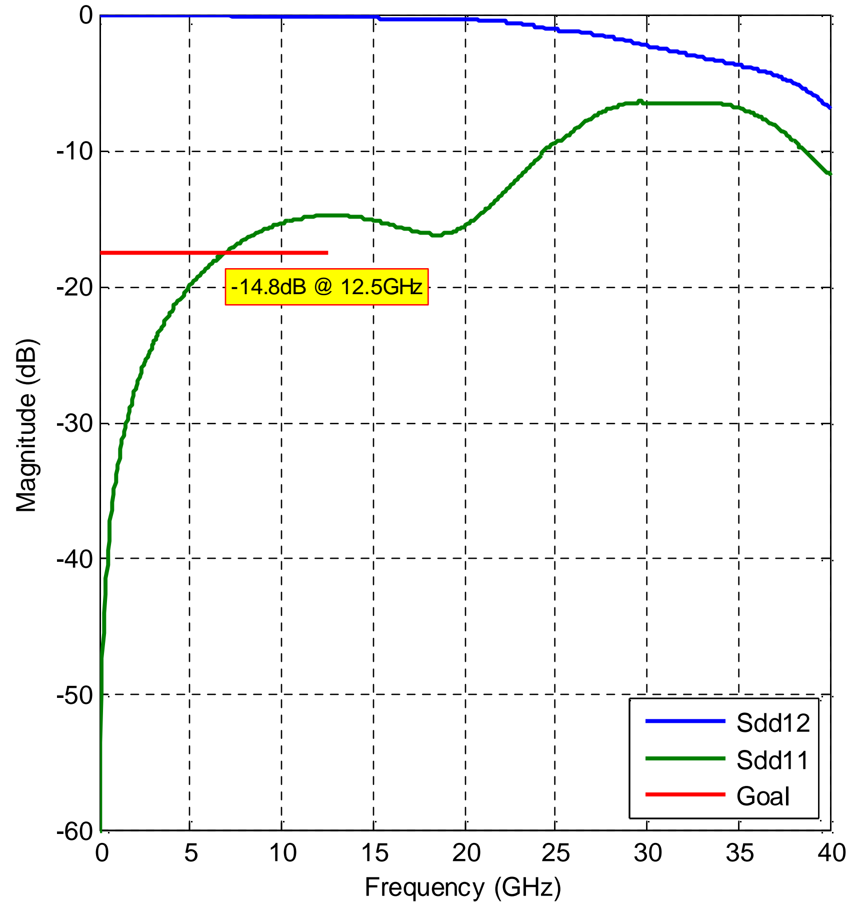


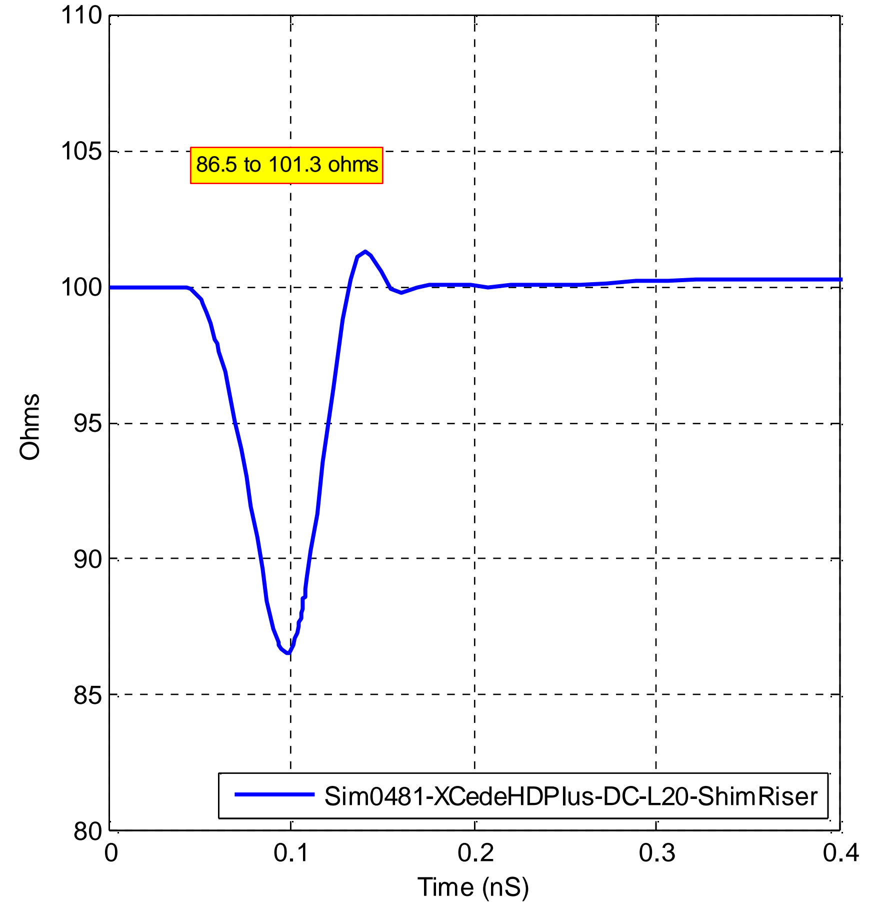




Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
Finished Dia	14.2mil			Diff Port Zo	100	Material	MyMeg6		
Drill Dia	17.7mil			Layer Escape	20	Dk	3.2		
Pad Dia	30.0mil	Default Stub	14.2mil	Line Width	5.25mil	Df	0.0067		
AntiPad Height	44.0mil	Backdrill Dia	29.2mil	EtchBack	0.1mil	Layers	26	Max Freq.	40 GHz
AntiPad Width	70.0mil	Backdrill Hole?	Yes	Line Space	9.8mil	Thickness	126.1 mil	Adapt Freq.	20 GHz

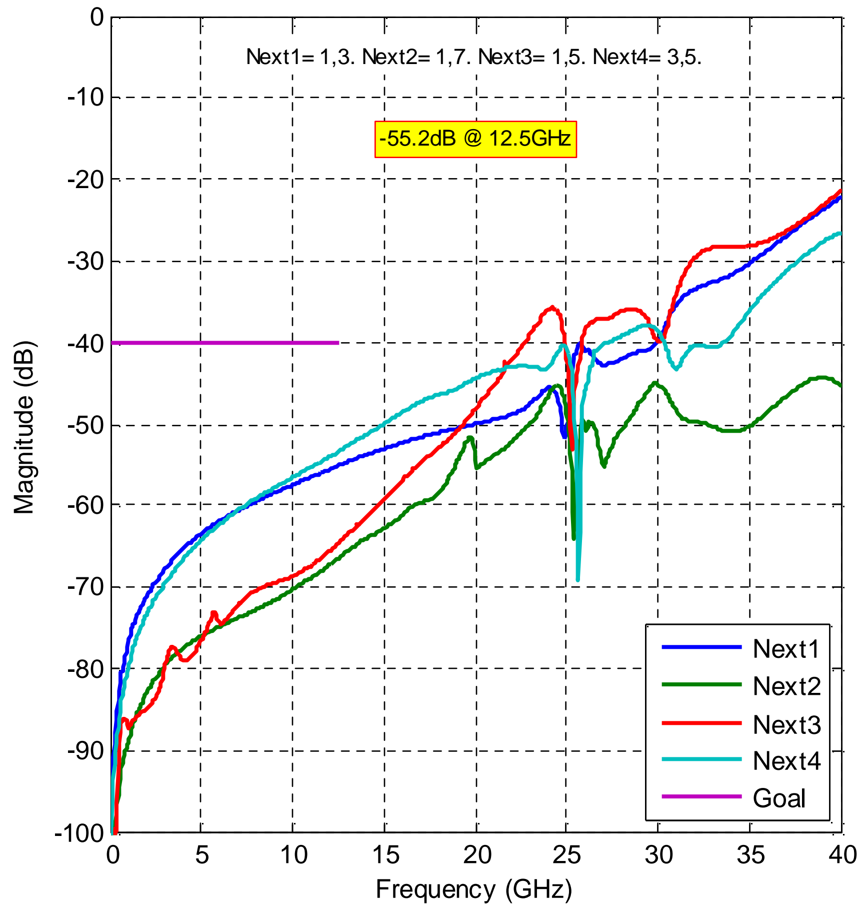
IL, RL and TDR: Amphenol XCedeHDPlus

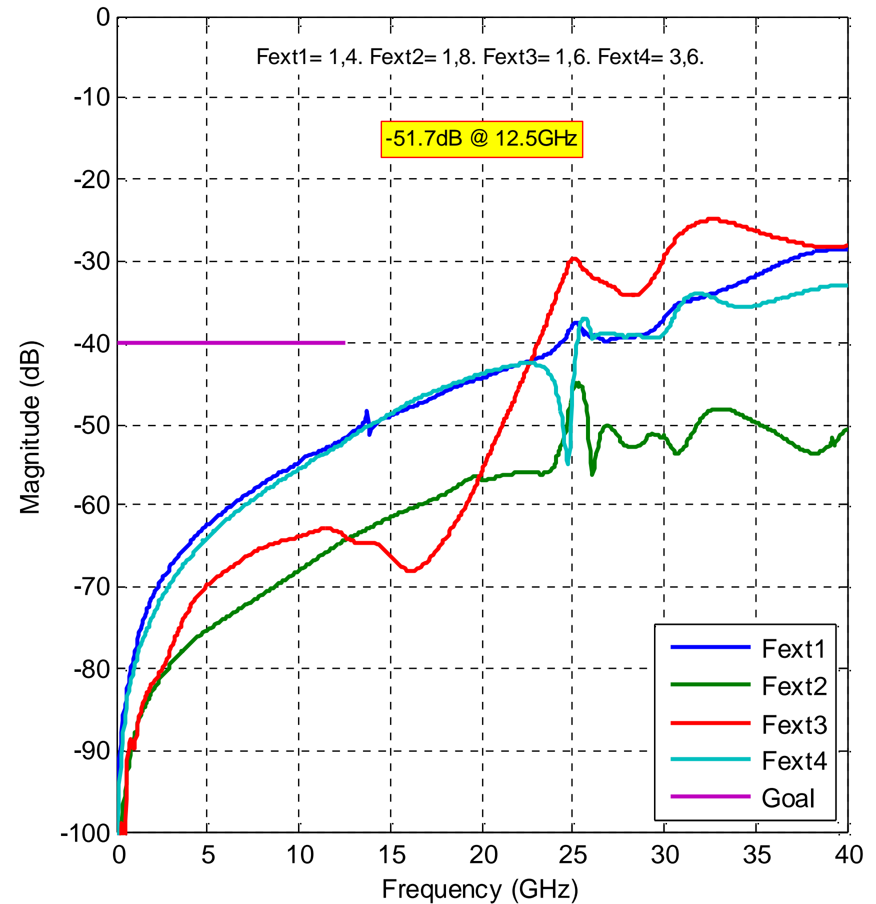




Next and Fext: Amphenol XCedeHDPlus

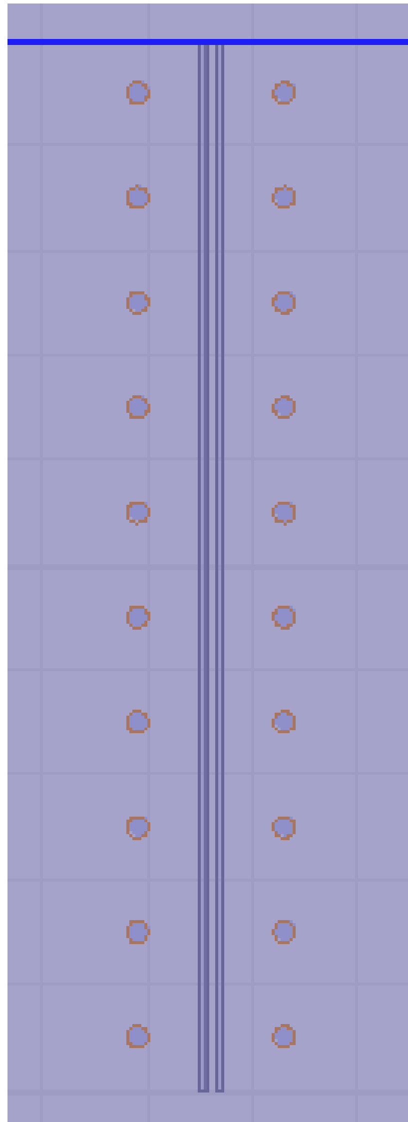
6.2x Lower than BGA Alternating Layer Example

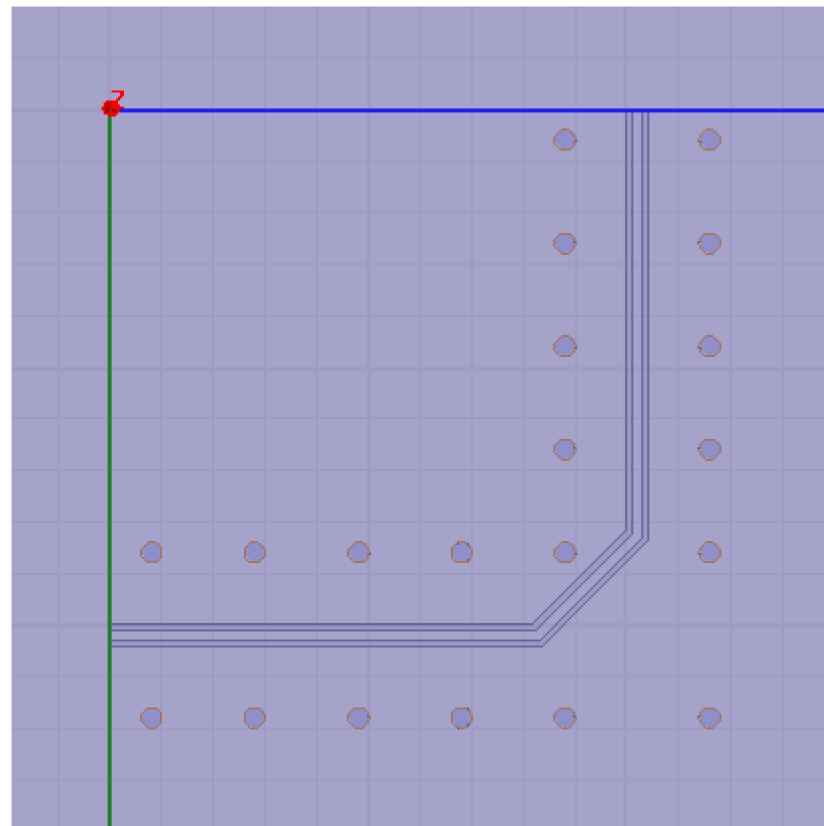




Etch Model Example: Mitre vs. Curved vs. Right Angle

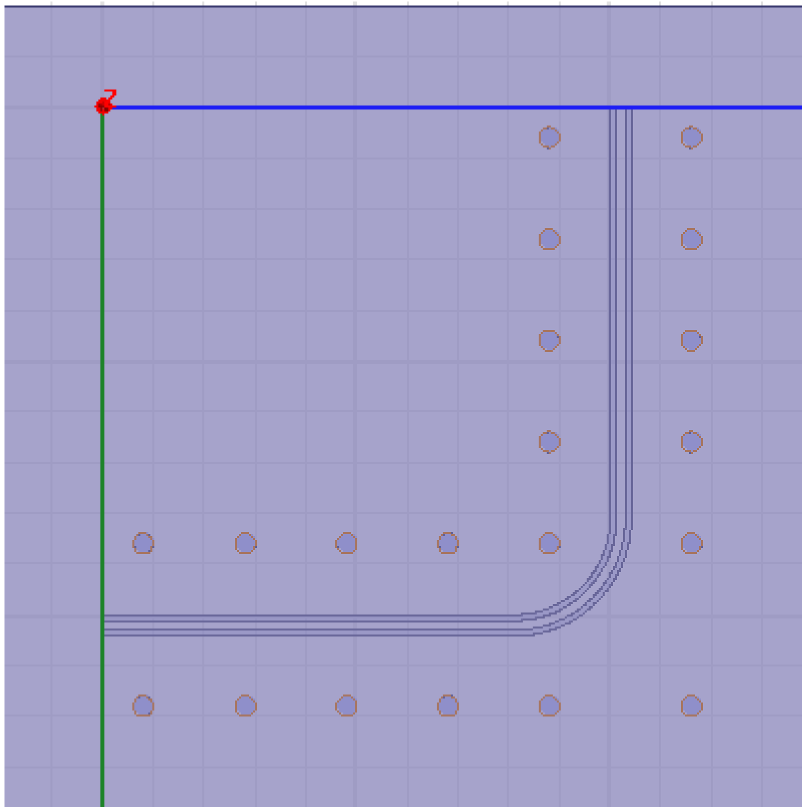
Straight Etch and Mitred Bend

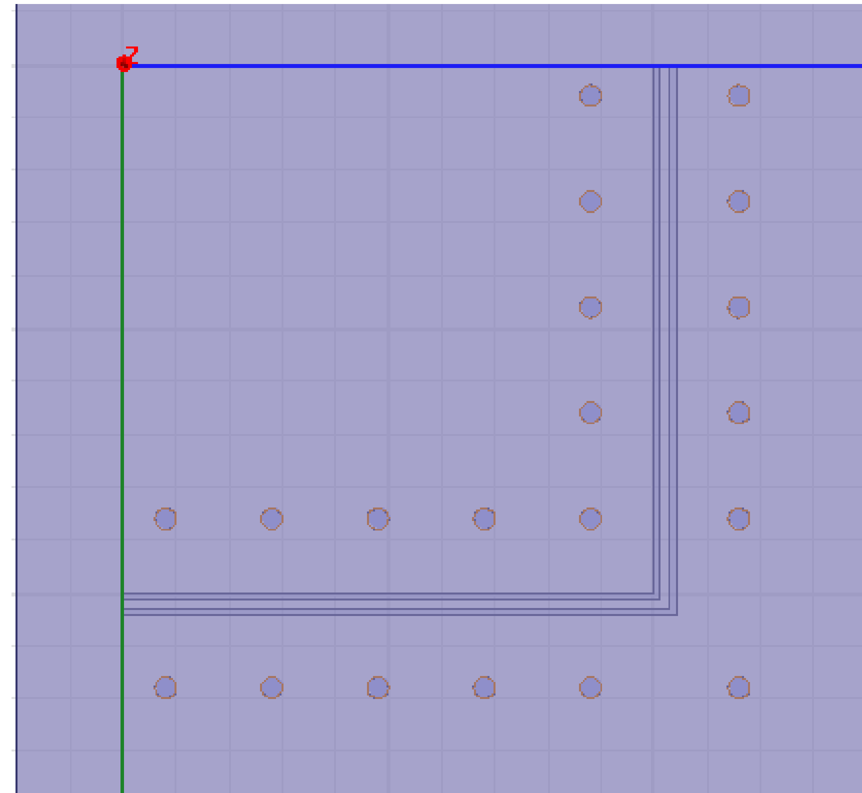




1.0” long, 6mil line, 9 mil space

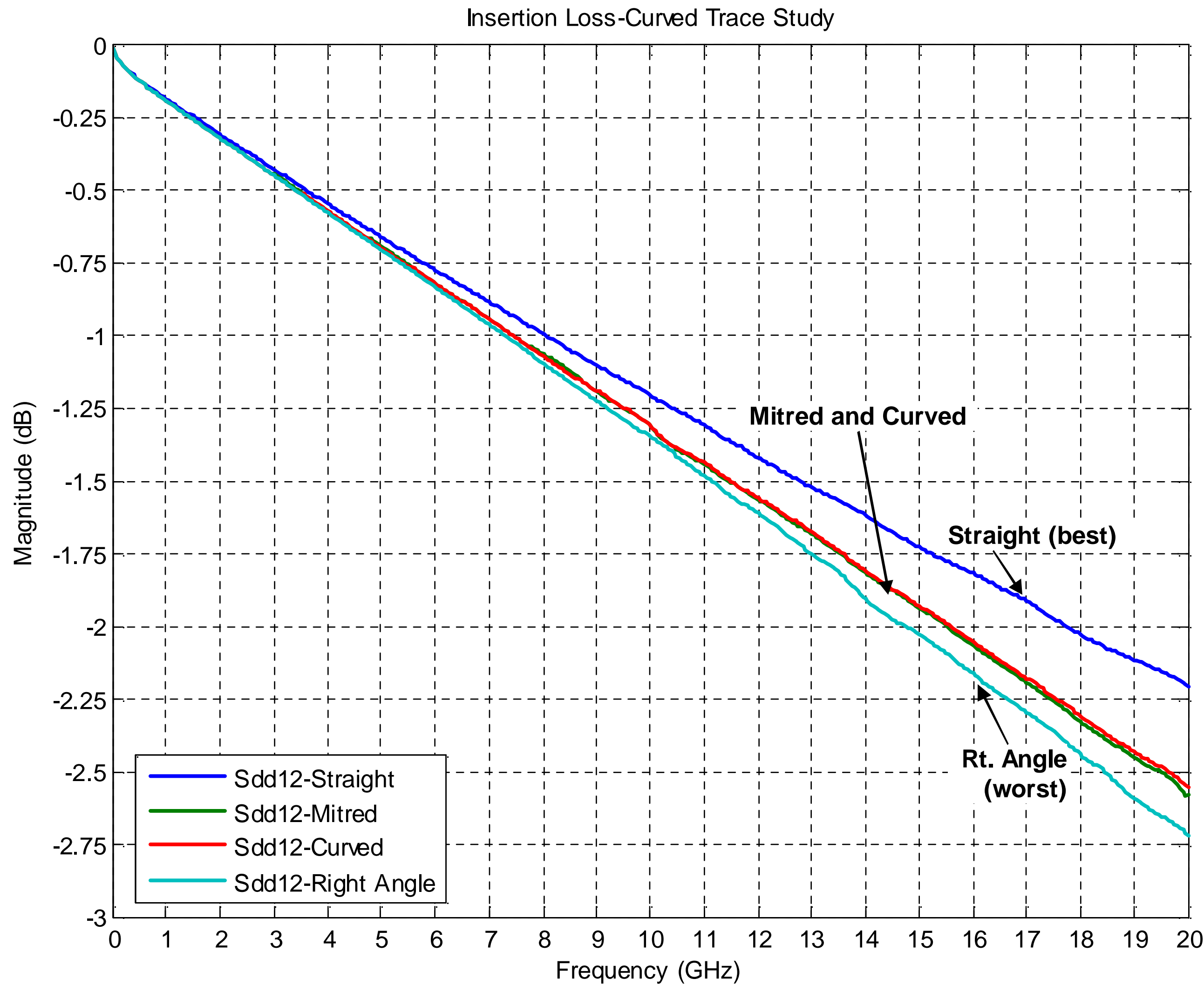
Curved Bend and Right Angle Bend





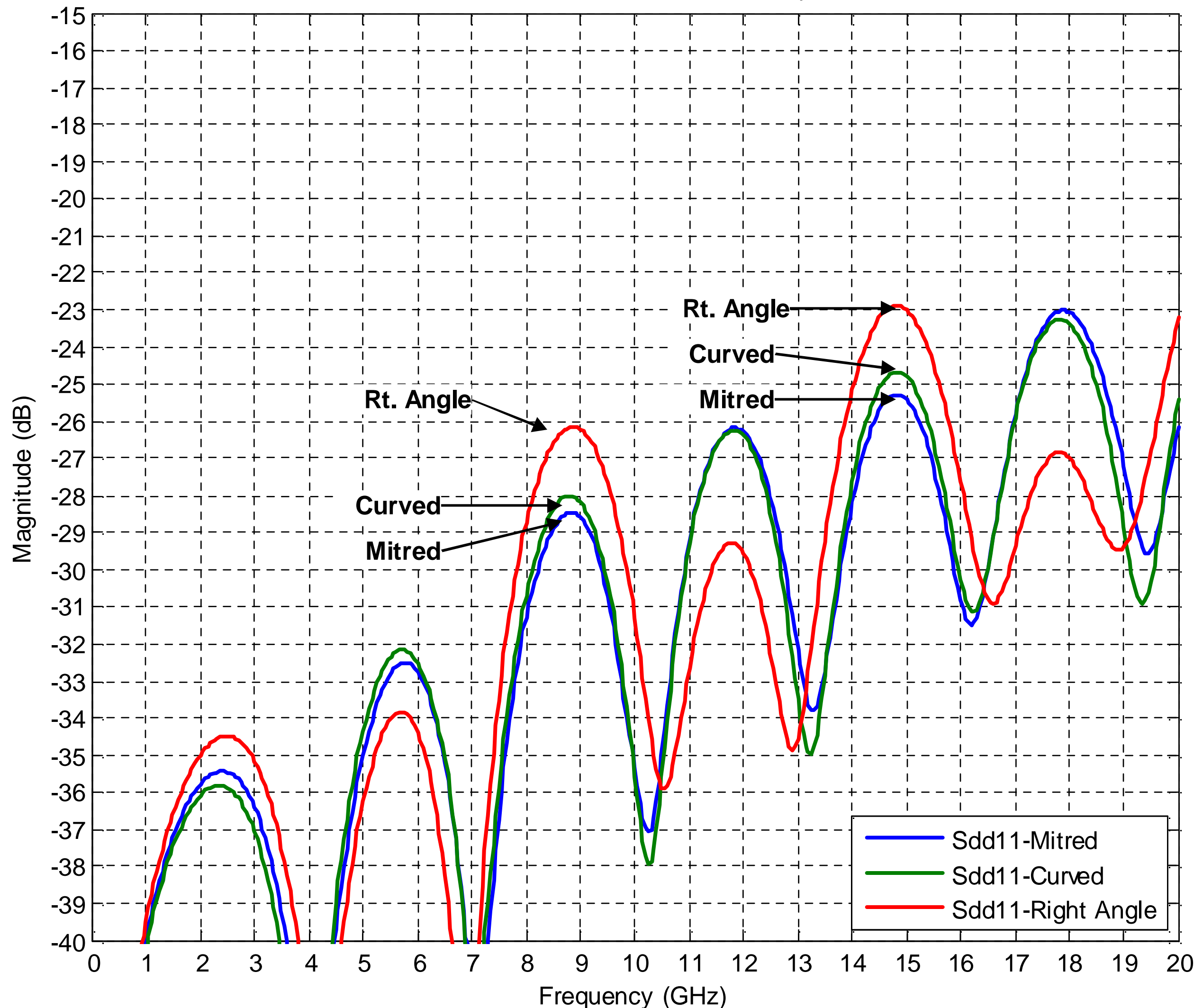
1.0” long, 6mil line, 9 mil space

Insertion Loss Comparison



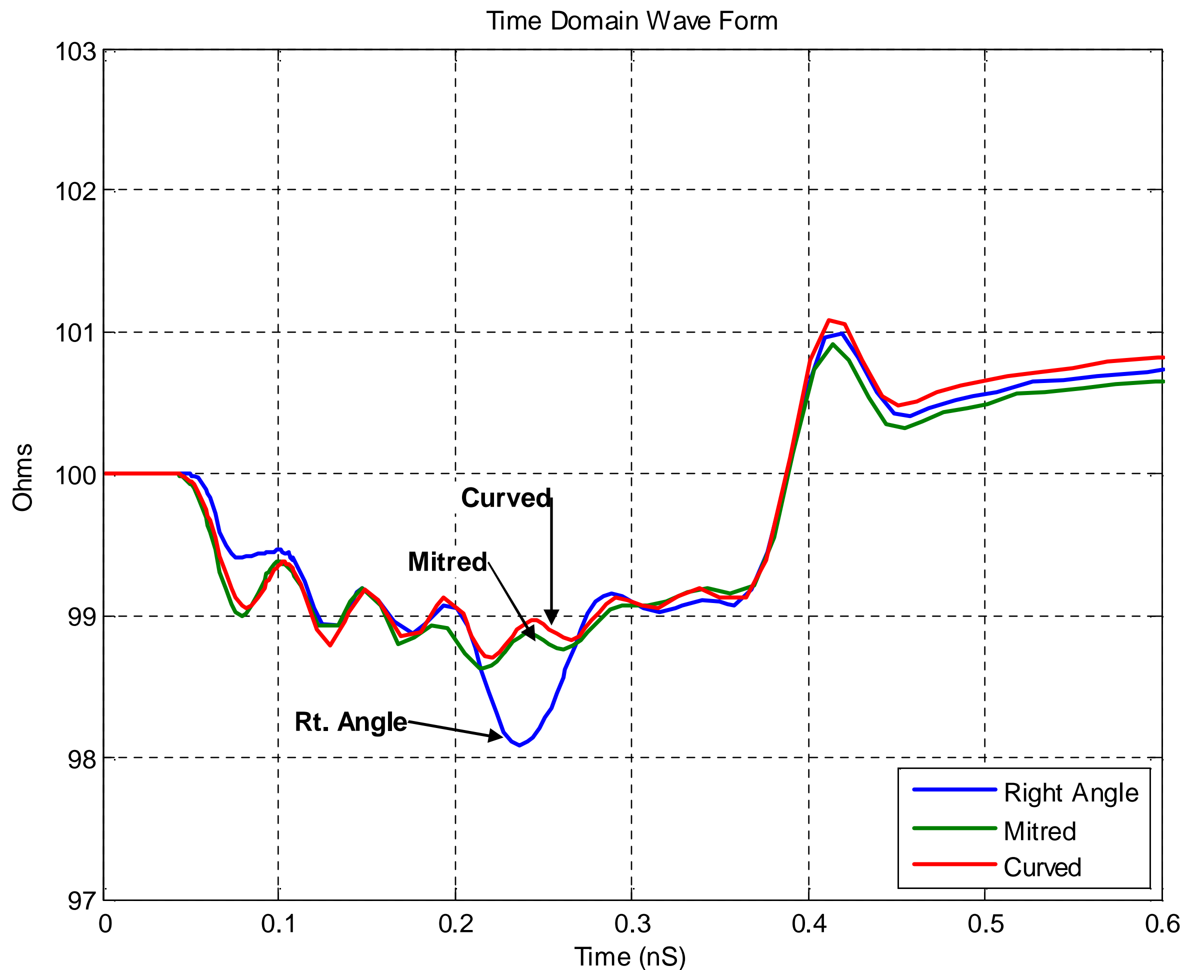
- **Higher** is better in this chart.
- After about 8GHz, the right angle bend is worse than the others.
- Mitred and Curved are about the same all the way out to 20GHz.
- Straight is best at all frequencies

Return Loss Comparison



- **Lower** is better in this chart.
- After about 7GHz, the Right Angle bend is worse.
- Mitred and Curved are about the same all the way out to 15GHz
- Anything under -25dB is considered great!

TDR Comparison

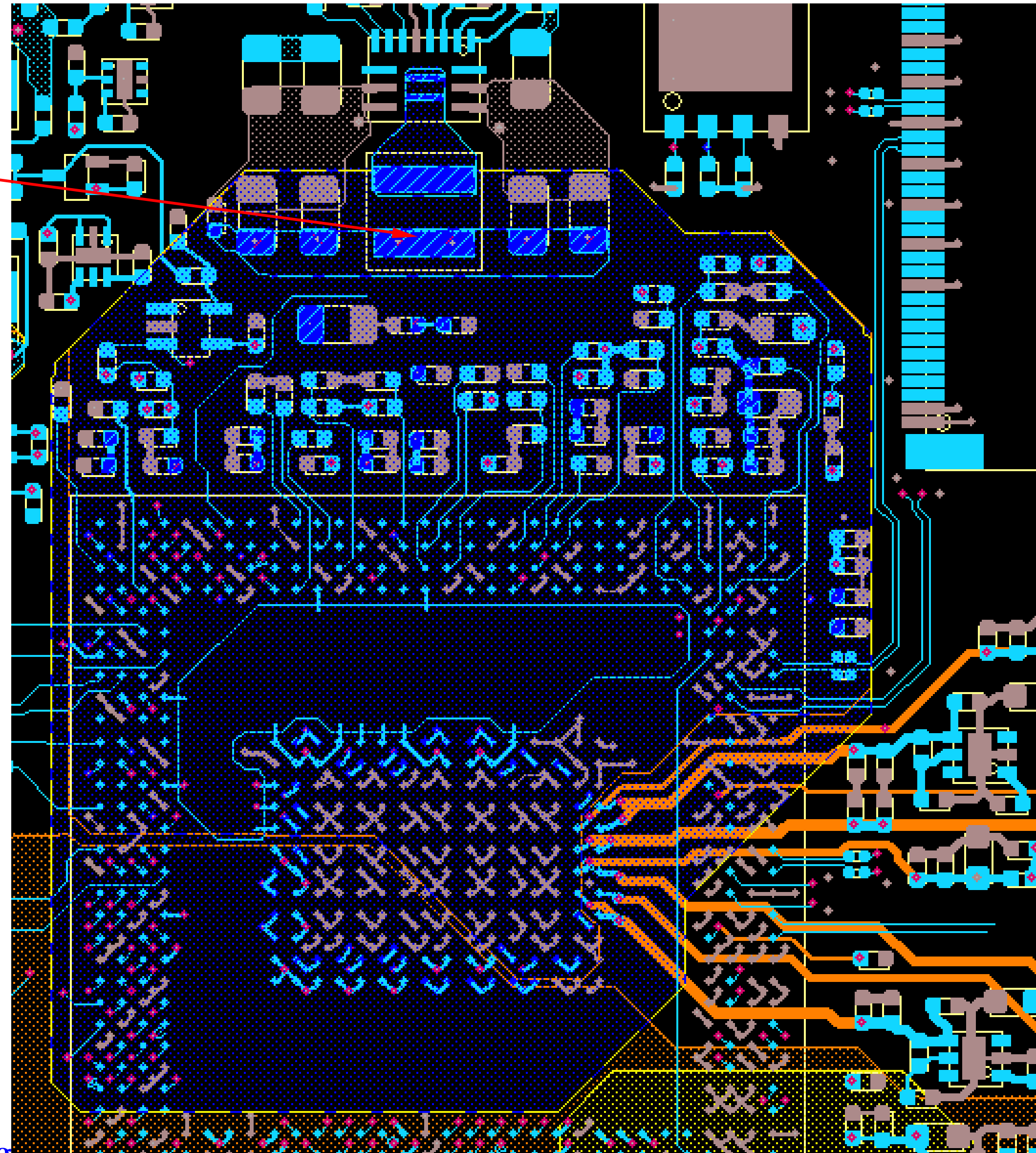


- **Flatter is better** in this chart.
- The Right Angle bend can be seen very clearly with the ~98ohm dip.
- The Curved and Mitred have very much the same TDR profile.

Power Integrity Example 1

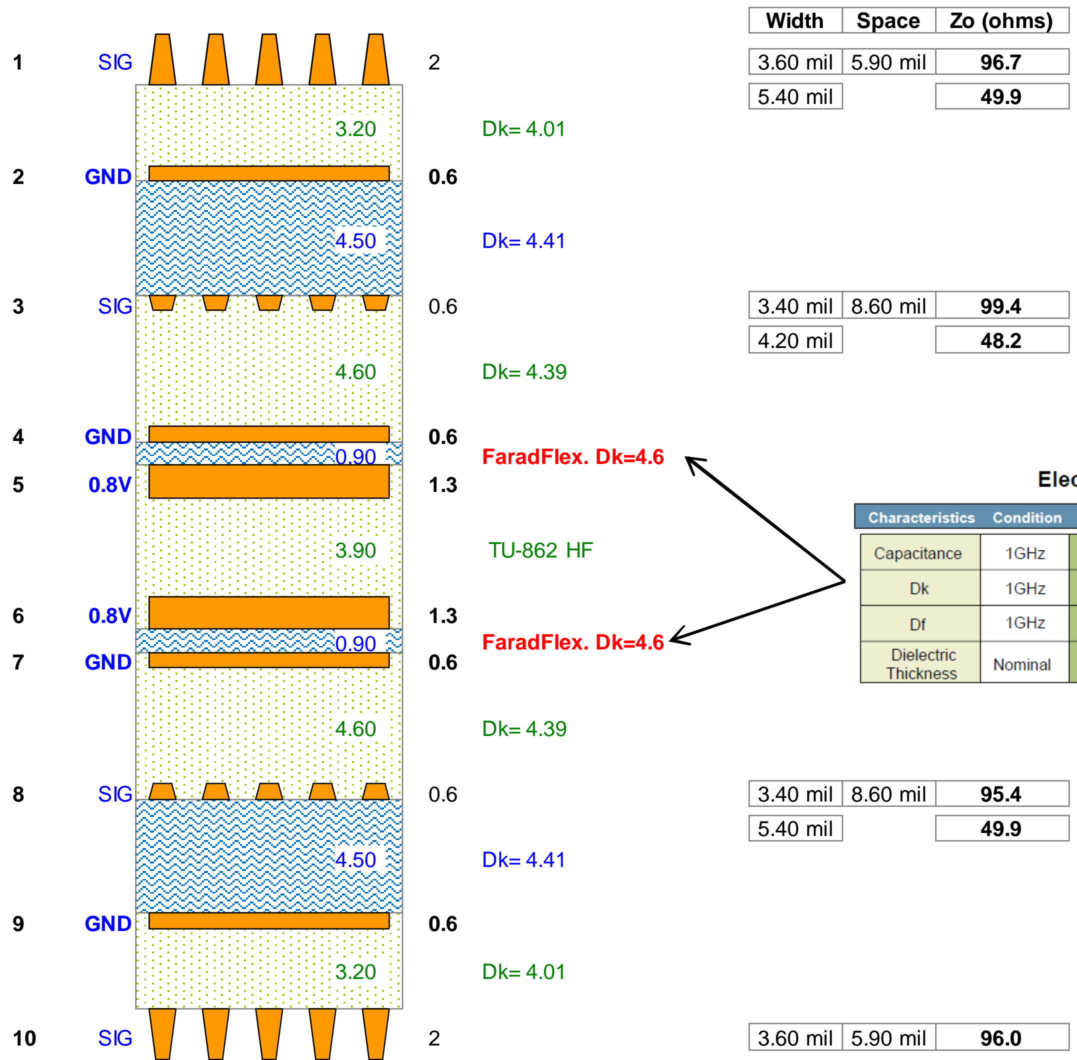
Example CPU CORE VOLTAGE Layout

Input Power Inductor at 0.86V



Assume a Total of 4 Amps DC evenly distributed at all the CPU CORE VOLTAGE pins at the device.

Stackup: With FaradFlex Embedded Capacitor Layers



Width	Space	Zo (ohms)
3.60 mil	5.90 mil	**96.7**
5.40 mil		**49.9**
3.40 mil	8.60 mil	**99.4**
4.20 mil		**48.2**
3.40 mil	8.60 mil	**95.4**
5.40 mil		**49.9**
3.60 mil	5.90 mil	**96.0**

Electrical Properties

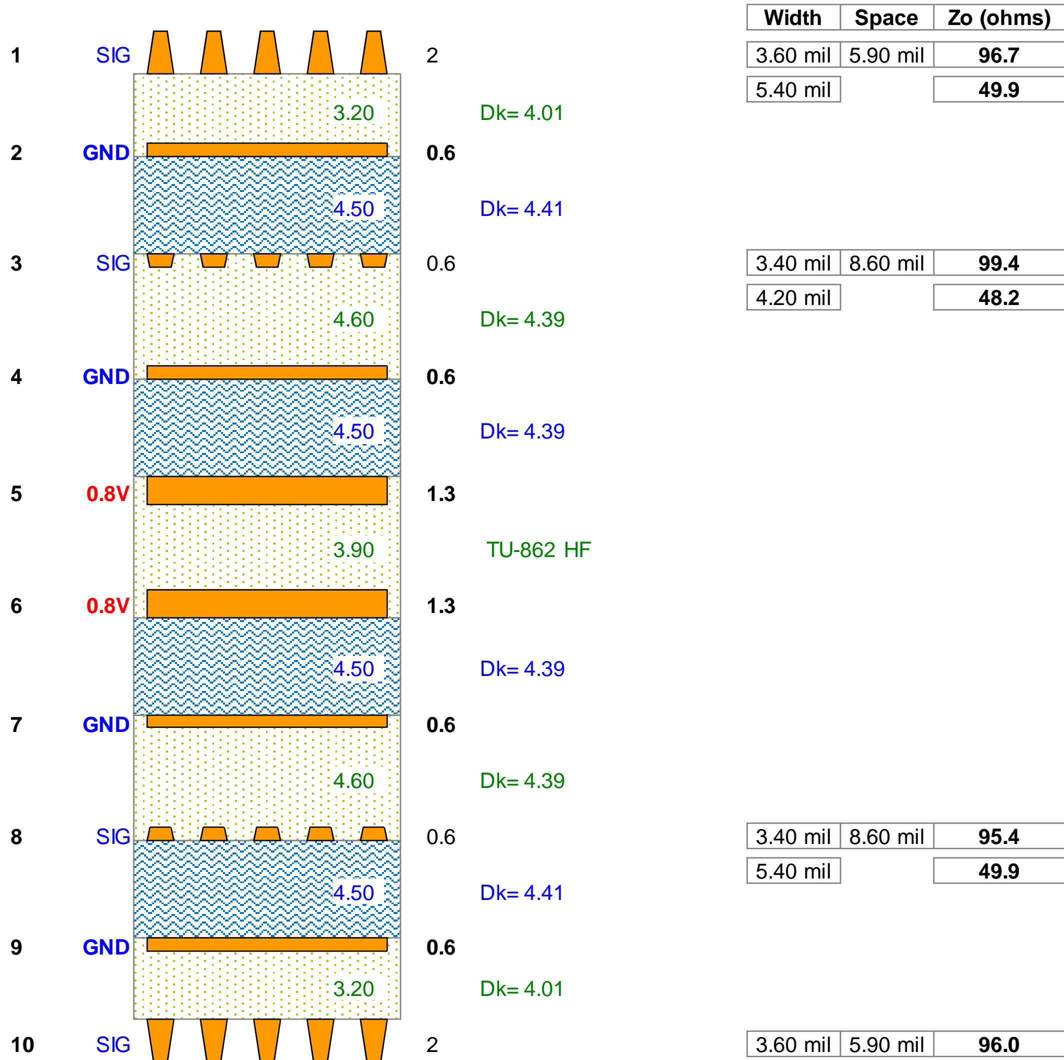
Characteristics	Condition	Unit	BC 24	BC 16	BC 12	BC 16T
Capacitance	1GHz	pF/in	900	1500	2000	10,000
Dk	1GHz	N/A	4.6	4.6	4.6	25.0
Df	1GHz	N/A	0.012	0.012	0.012	0.014
Dielectric Thickness	Nominal	Micron Meter	24	16	12	16

Thickness Over Copper = 40.5 mils

Thickness Over Soldermask = 42.1 mils

CSH Consulting LLC www.cshconsulting.net chris.heard100@gmail.com. 603-494-9277

Stackup: Without FaradFlex



Thickness Over Copper = 47.7 mils

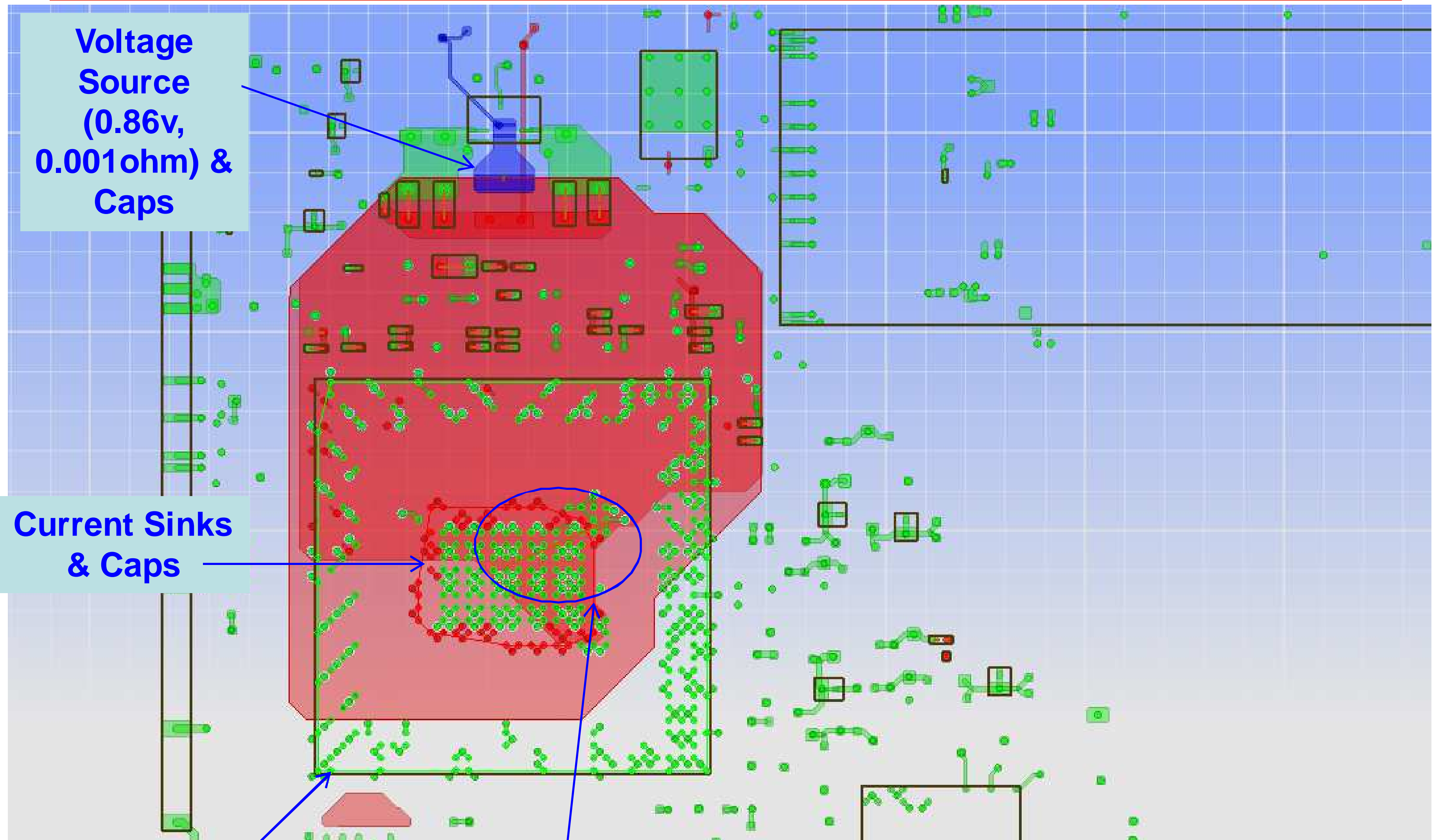
Thickness Over Soldermask = 49.3 mils

CPU CORE VOLTAGE: Active Caps

Part Number	RefDes	Capacitance (F)	Parasitic L (H)	Parasitic R (ohms)
EMK105BJ104	C618	1.00E-07	4.30E-10	0.0144259
EMK105BJ104	C705	1.00E-07	4.30E-10	0.0144259
JMK105F105	C706	1.00E-06	1.71E-10	0.0023298
EMK105BJ104	C727	1.00E-07	4.30E-10	0.0144259
EMK105BJ104	C739	1.00E-07	4.30E-10	0.0144259
EMK105BJ104	C743	1.00E-07	4.30E-10	0.0144259
JMK105F105	C744	1.00E-06	1.71E-10	0.0023298
JMK105F105	C748a	1.00E-06	1.71E-10	0.0023298
EMK105BJ104	C752	1.00E-07	4.30E-10	0.0144259
CL21A476MQMNRN	C758	4.70E-05	5.97E-10	0.00247449
CL21A476MQMNRN	C762	4.70E-05	5.97E-10	0.00247449
C0603C106K9PAC	C768	1.00E-05	7.86E-10	0.00390001
CL21A476MQMNRN	C1603	4.70E-05	5.97E-10	0.00247449
CL21A476MQMNRN	C1604	4.70E-05	5.97E-10	0.00247449
EMK105BJ104	C1606	1.00E-07	4.30E-10	0.0144259
CL21A476MQMNRN	C1607	4.70E-05	5.97E-10	0.00247449
TMK105BJ103	C1927	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1928	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1929	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1930	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1931	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1952	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1953	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1954	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1955	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1956	1.00E-08	4.70E-10	0.0317317
TMK105BJ103	C1957	1.00E-08	4.70E-10	0.0317317

Cap Value (uF)	Quantity
0.01	11
0.1	7
1.0	3
10	1
47	5
Totals	27

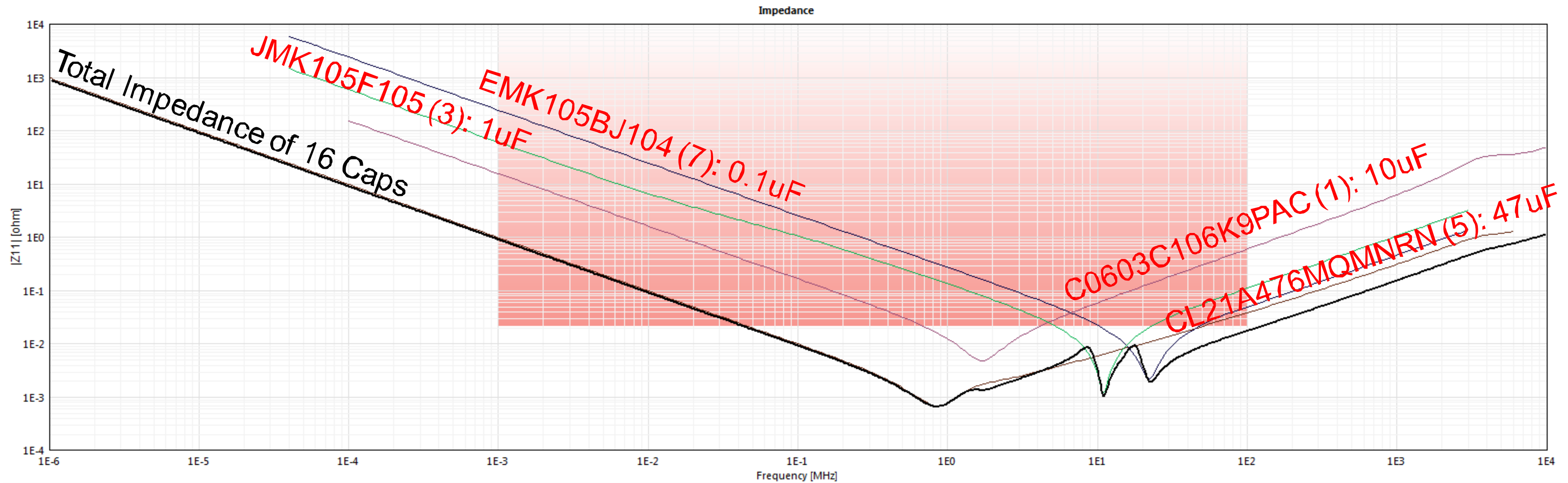
CPU CORE VOLTAGE Plane SI Wave Import



IC200

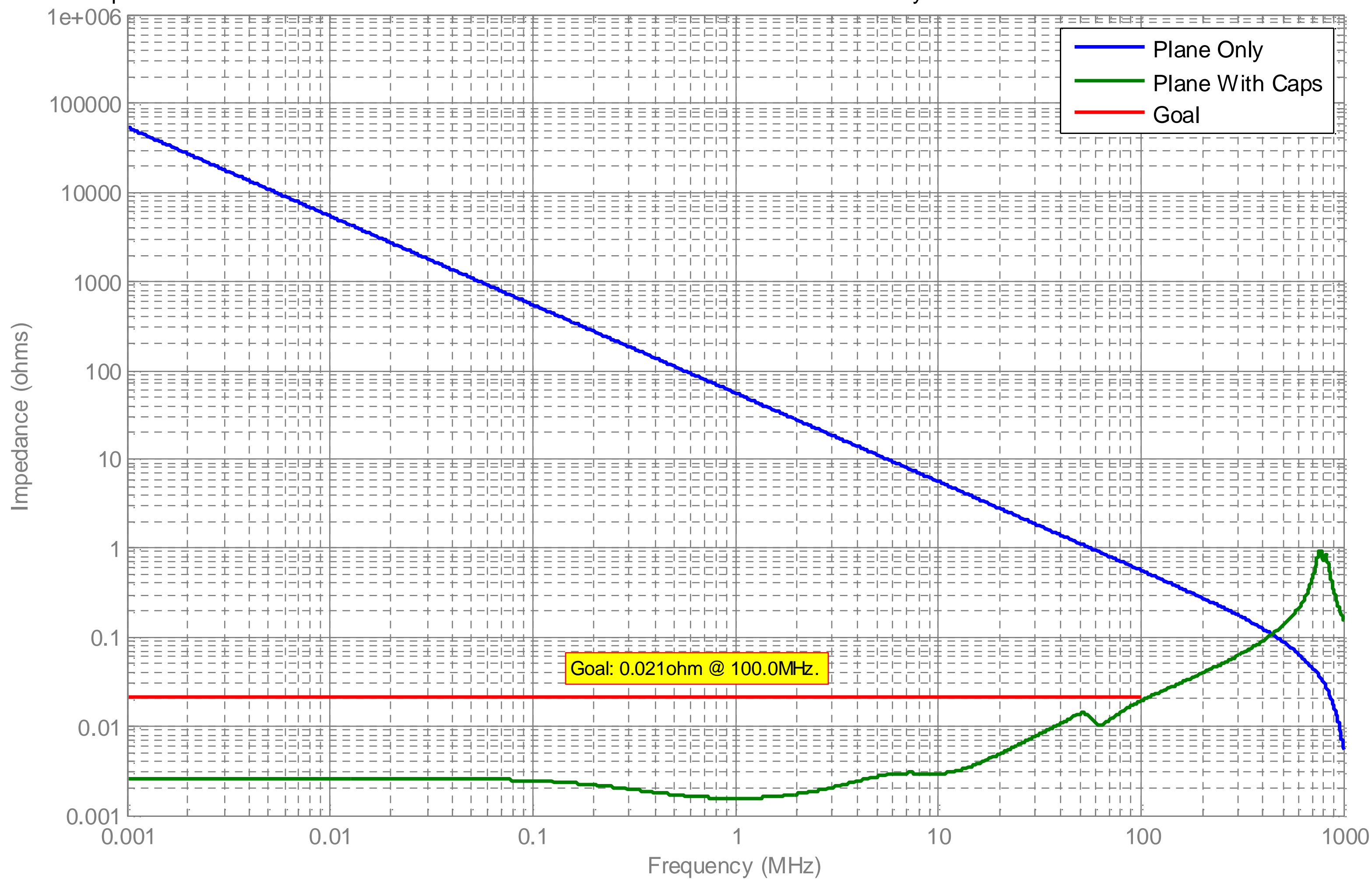
Port

Capacitor Plots

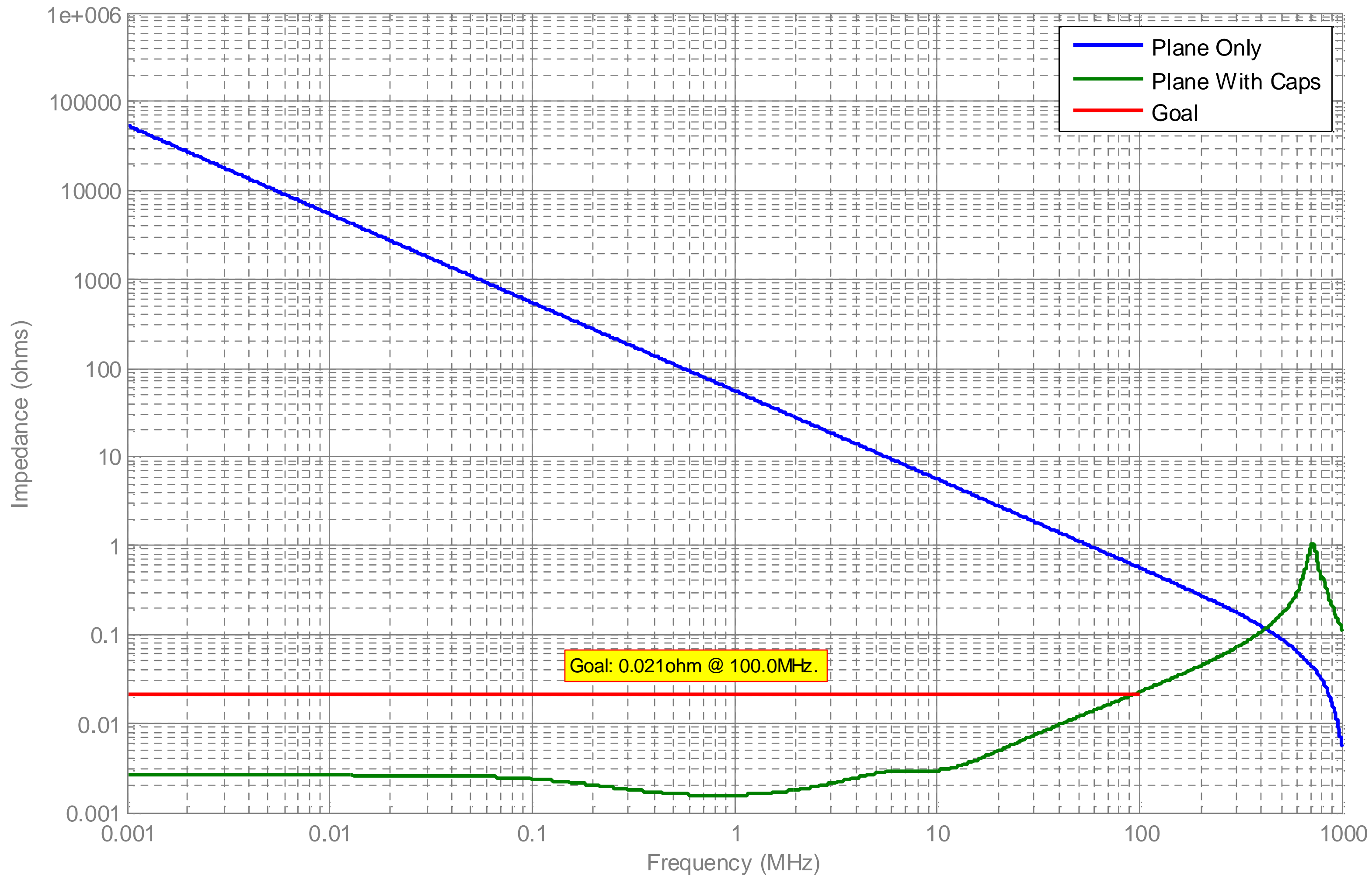


Vendor	Series	Part Name	Plot	Value (F)	# Acti...	EIA Size	Price	L_mnt (H)	R_mnt (ohms)	SRF (Hz)	S_min (dB)	ESR (ohms)	ESL (H)
YUDEN	Standard_Class2_1005(0...	EMK105BJ104	☑	1E-07	7	0402	0	1E-10	0.001	2.42763E+07	-76.5692	0.0144259	4.29808E-10
Samsung	2012	CL21A476MQMNRN	☑	4.7E-05	5	0805	0	1E-10	0.001	950113	-91.9274	0.00247449	5.97024E-10
YUDEN	Standard_Class2_1005(0...	JMK105F105	☑	1E-06	3	0402	0	1E-10	0.001	1.21622E+07	-91.0282	0.0023298	1.71246E-10
Kemet	C0603C	C0603C106K9PAC	☑	1E-05	1	0603	0	1E-10	0.001	1.79497E+06	-88.1604	0.00390001	7.86188E-10

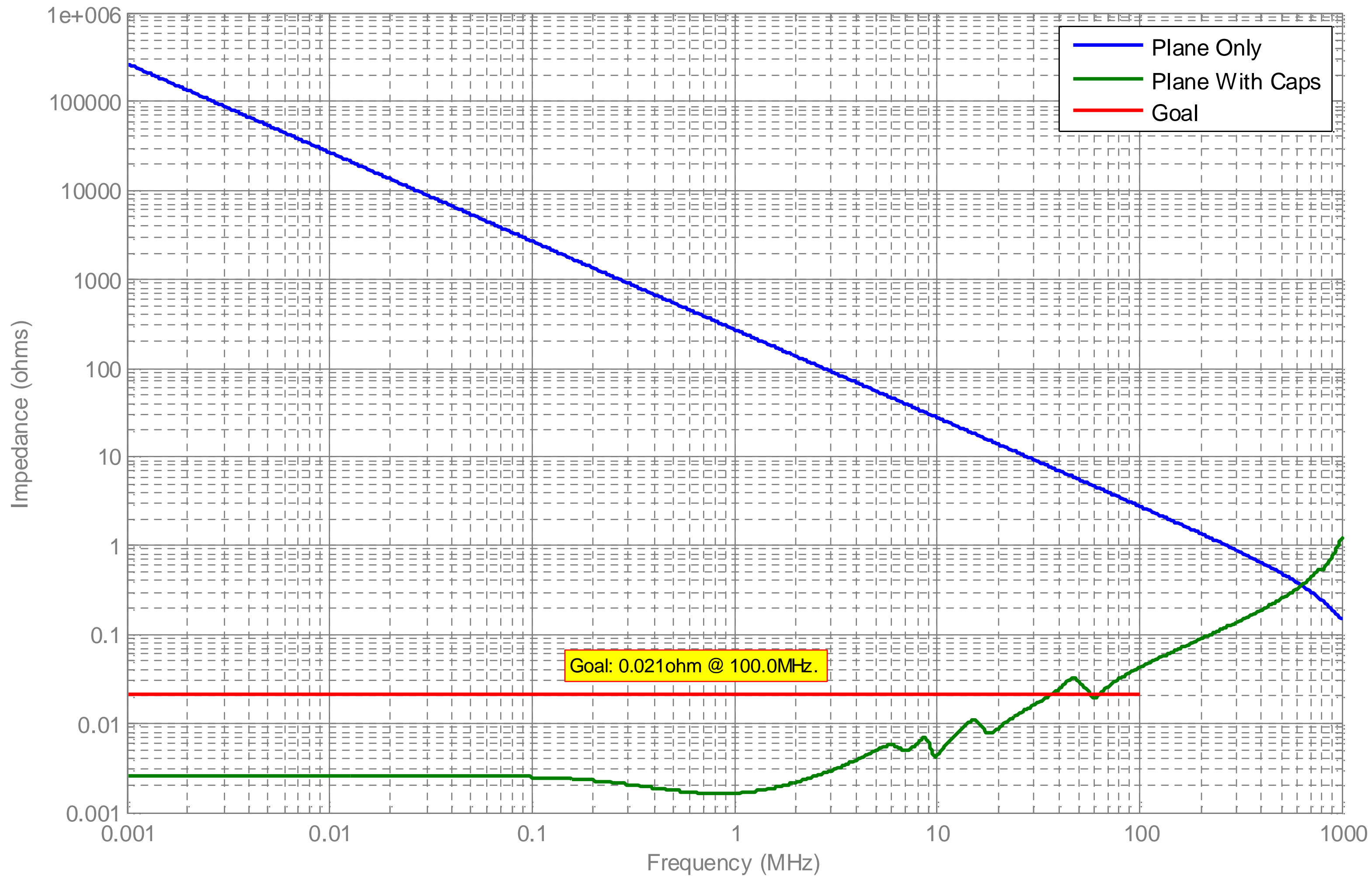
Example CPU CORE VOLTAGE: Zo vs Freq With Faradflex Layers



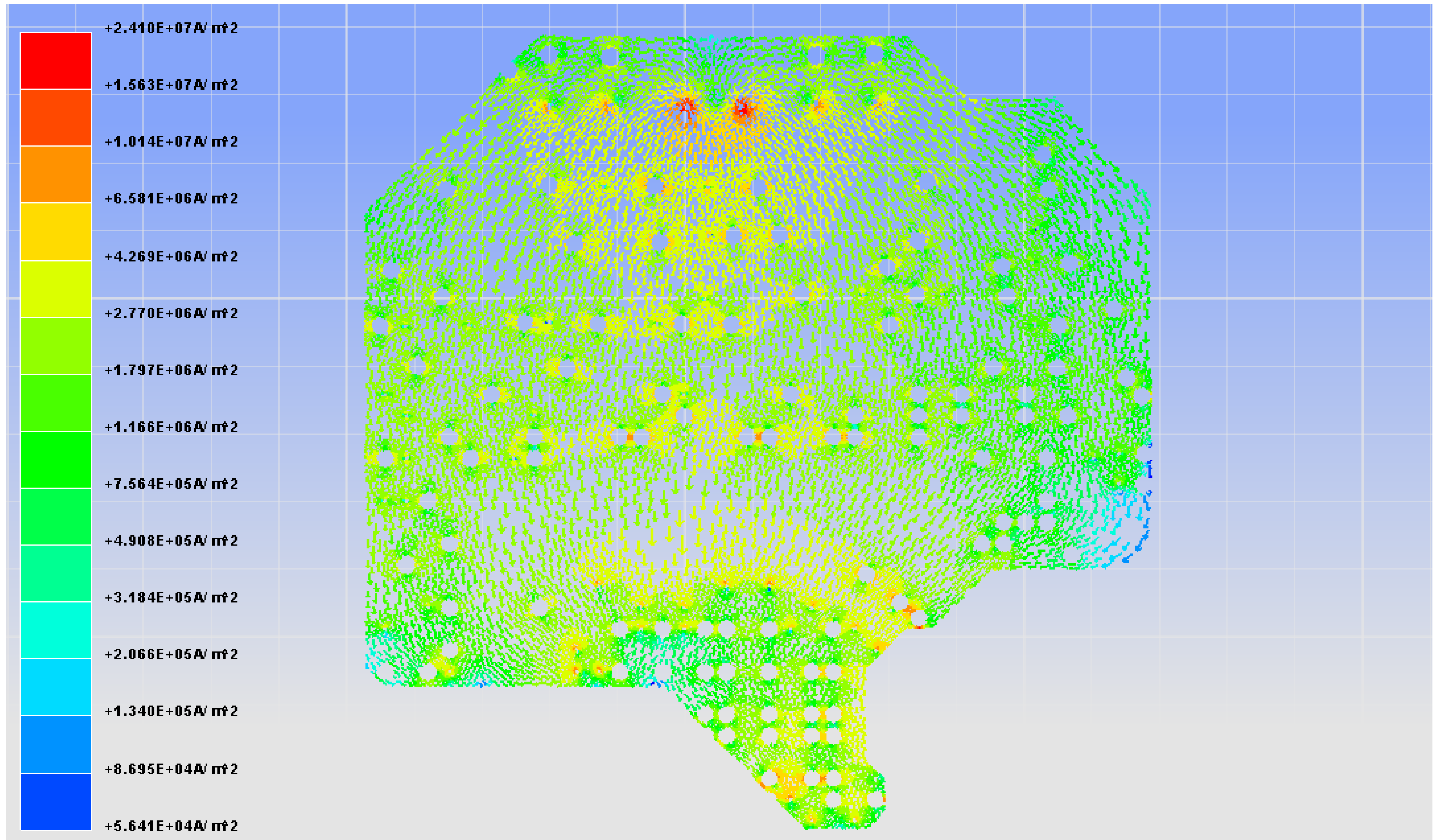
Example CPU CORE VOLTAGE: Zo vs Freq With Faradflex Layers and No 0.01uF Caps



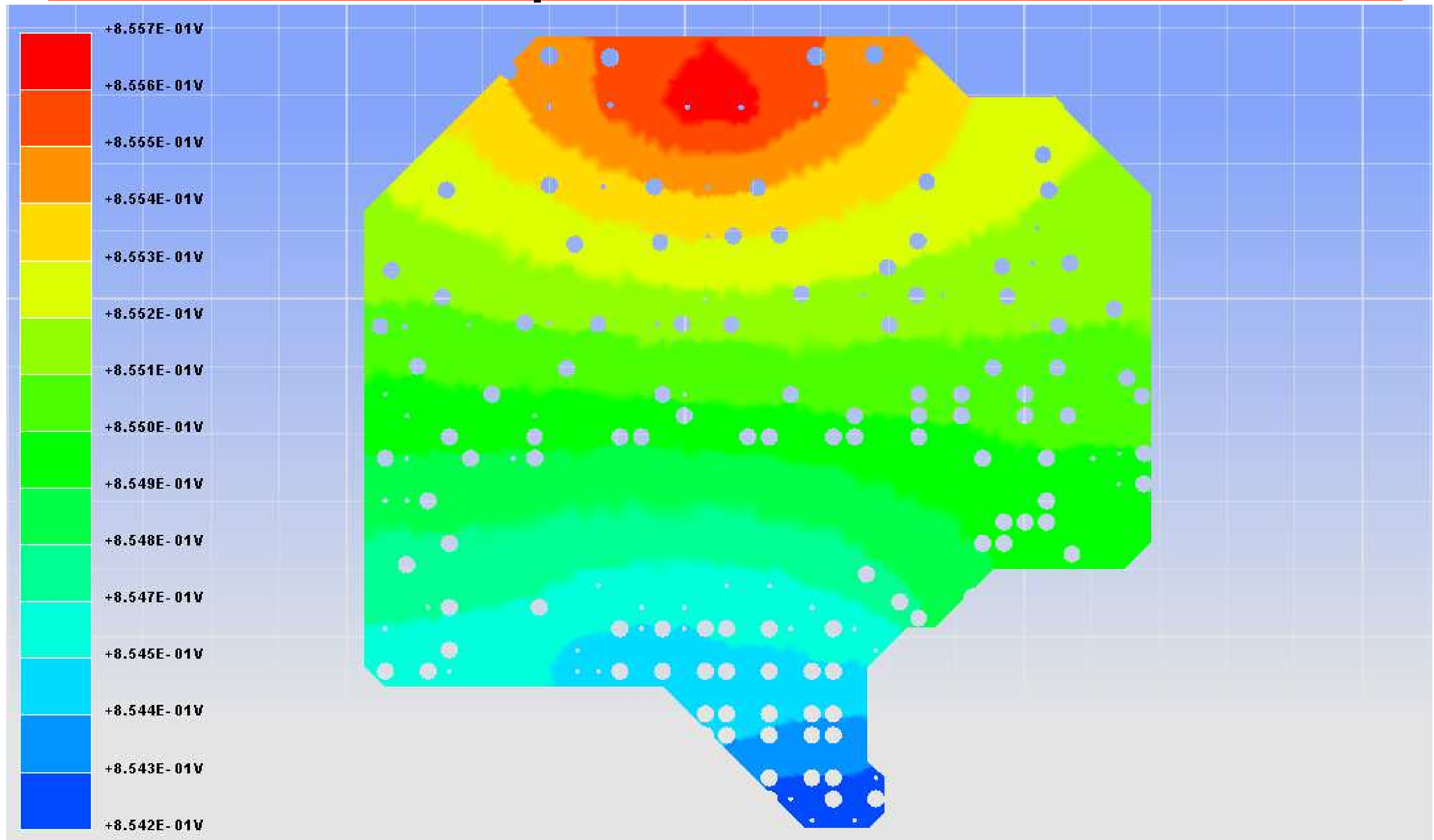
Example CPU CORE VOLTAGE: Zo vs Freq Without Faradflex Layers



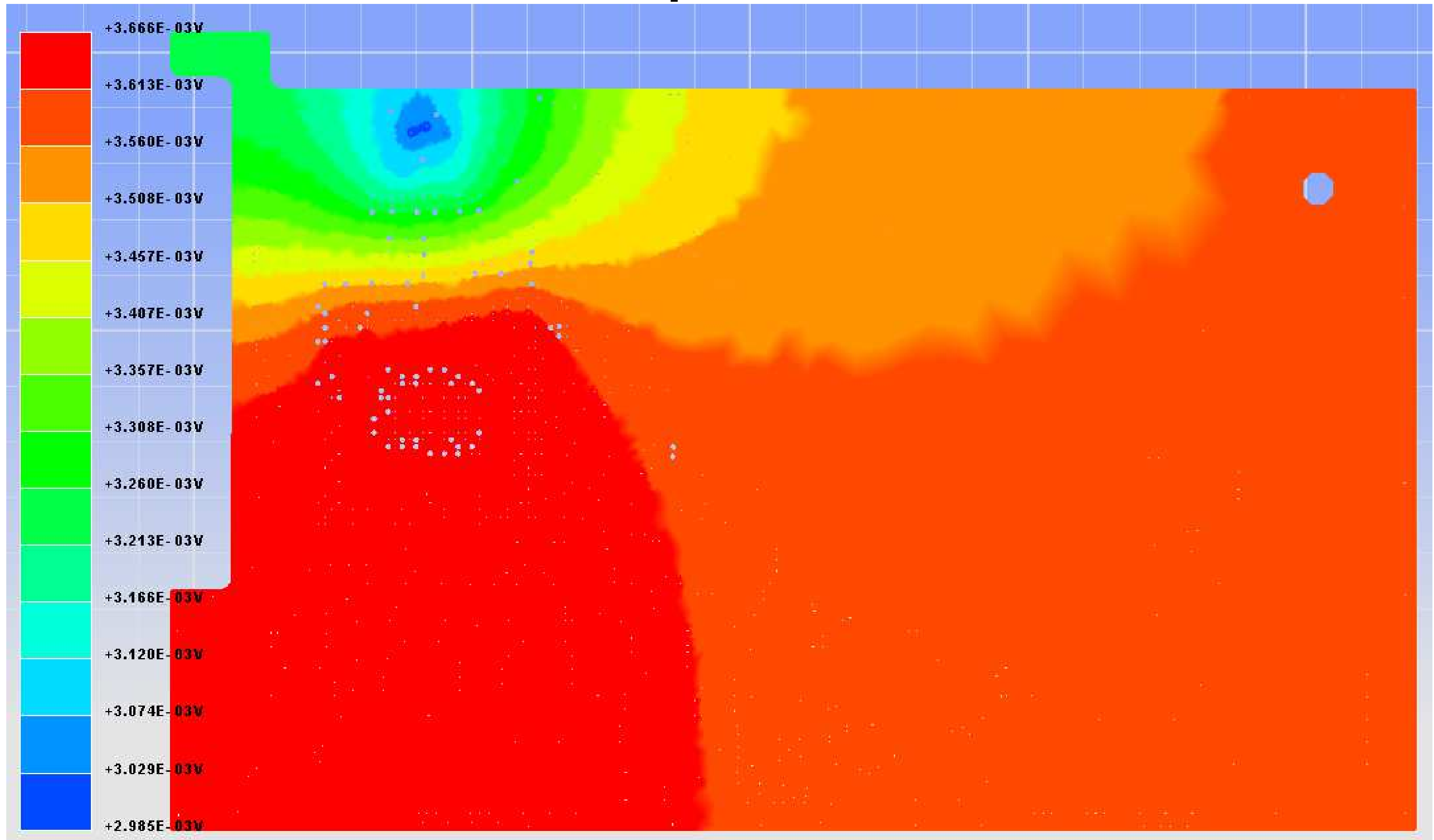
Example CPU CORE VOLTAGE Current Plot



Layer 6 Example CPU CORE VOLTAGE Voltage Plot: IR Drop: 1.5mV, 4A. 0.375mΩ

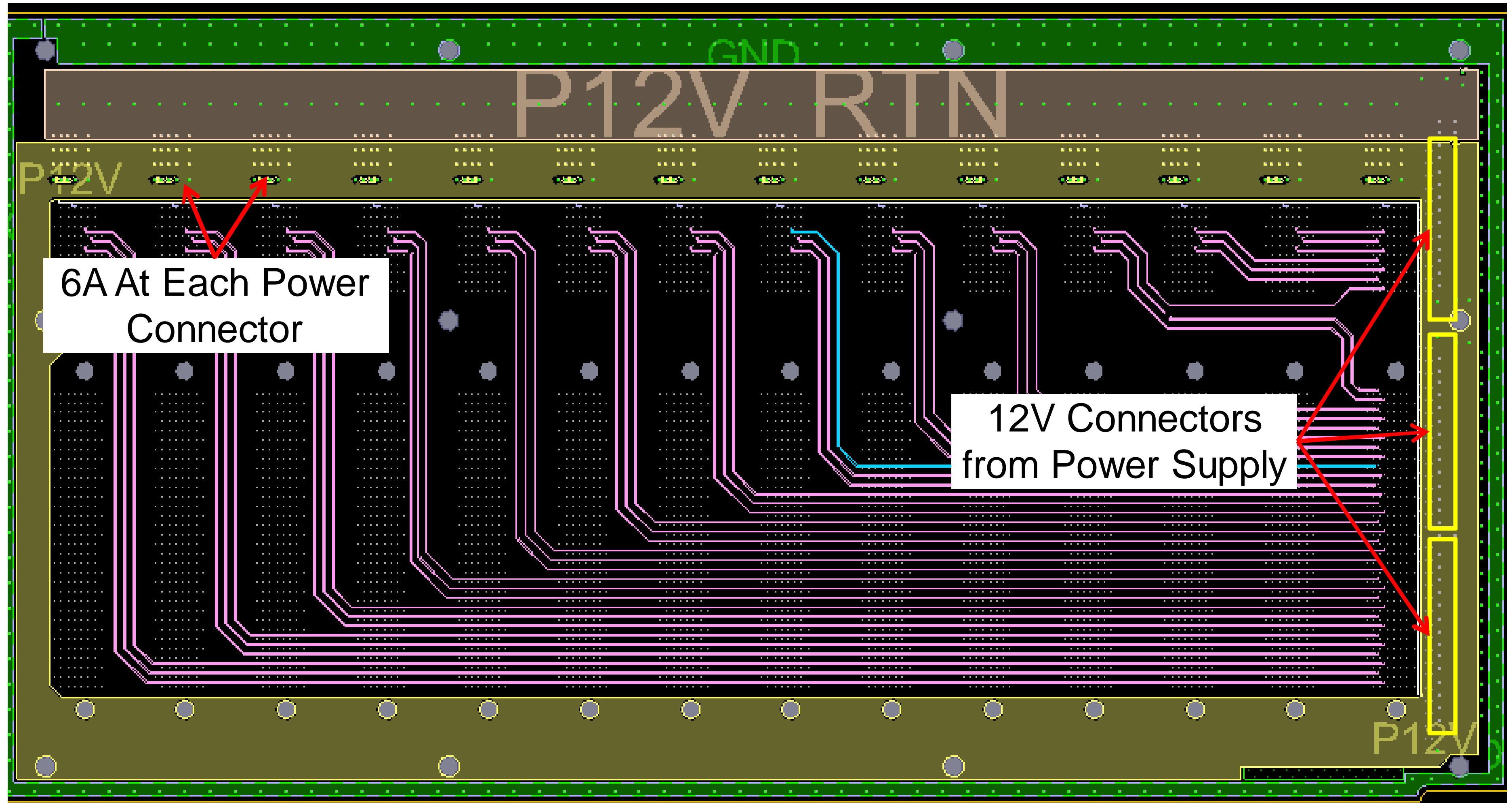


Layer 7 Voltage Plot: GND
IR Drop: 0.681mV



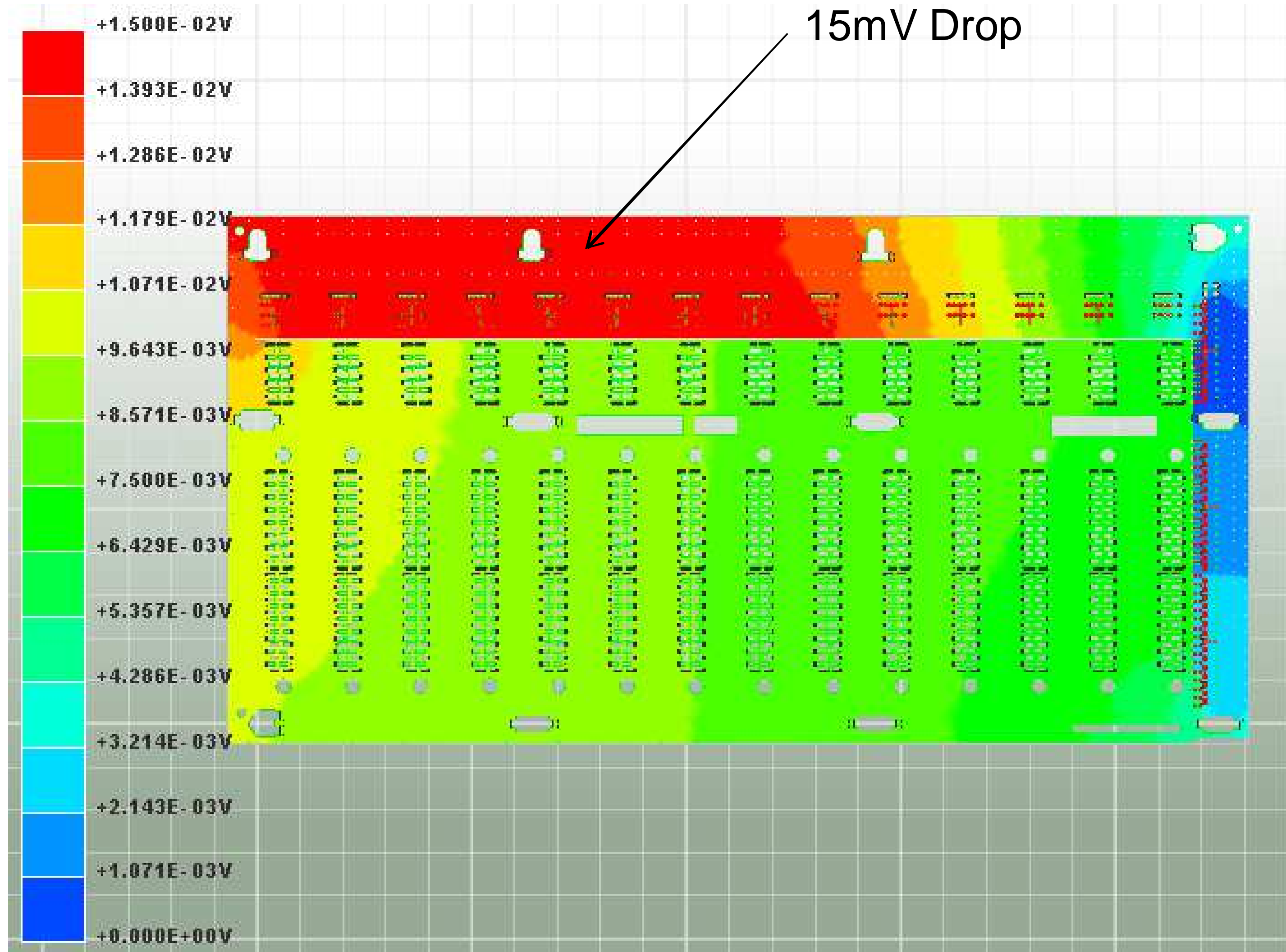
Power Integrity Example 2

Backplane 12V Current

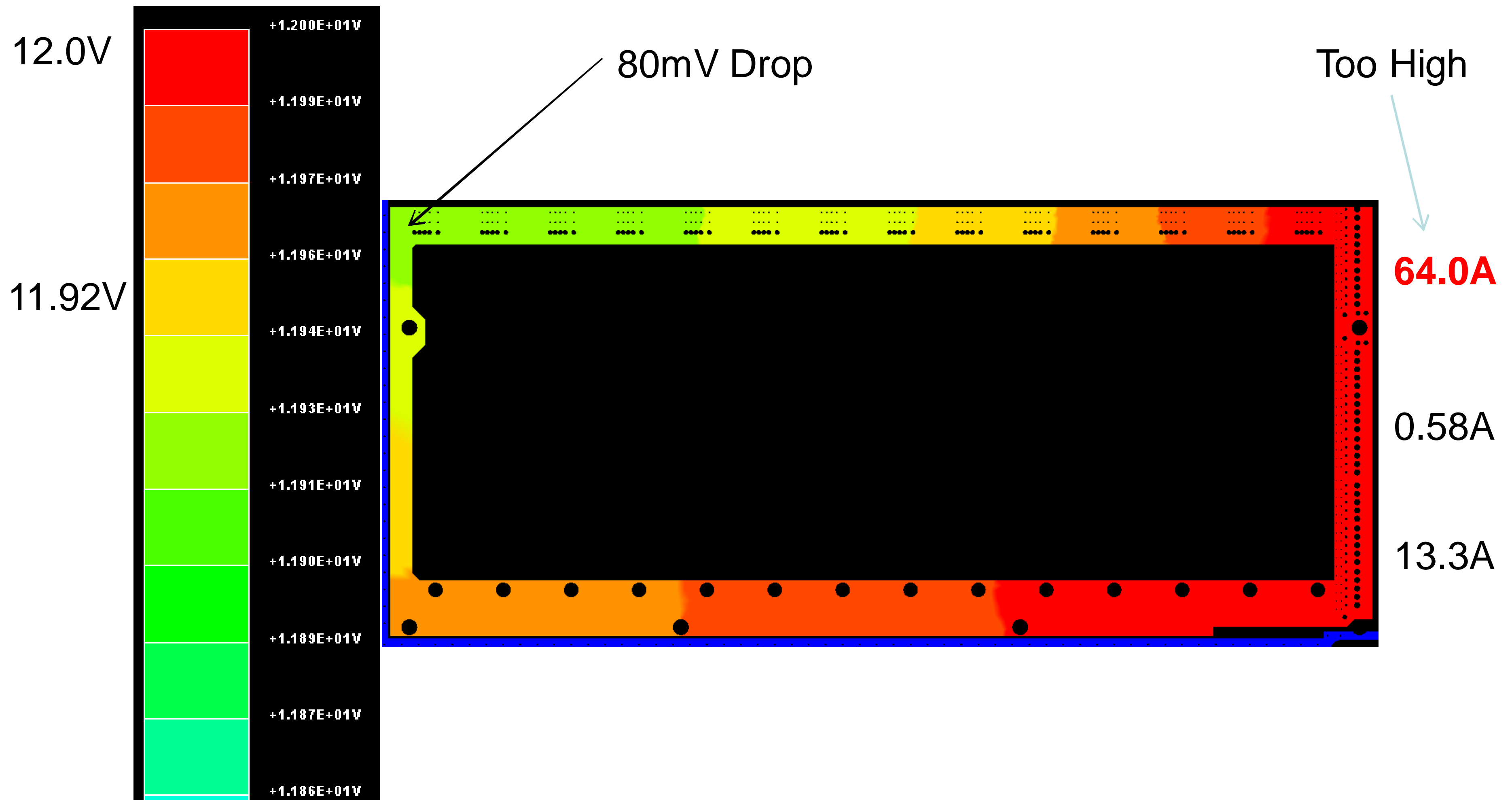


78 amps total.

Voltage Plot. Gnd Plane: 15mV Total



Voltage Plot: +12V Plane: 80mV Total



+12V Current Density