Mistakes even the best engineers make

How & why to build better libraries

Natasha Baker, Founder & CEO

Overview

Why libraries matter

Common symbol & footprint errors

The need for verification

Tools that can help

SnapEDA

In today’s talk, you’ll learn:

1. Why high-quality libraries matter
2. Common mistakes among a) the newbies and b) the pros
3. Tips & tricks to stay focused on building the best electronics possible!

Bio

- 12 years working on PCB design tools and libraries
- Electrical & computer engineer from the University of Toronto
- Founder of SnapEDA, electronics library used by 1M engineers

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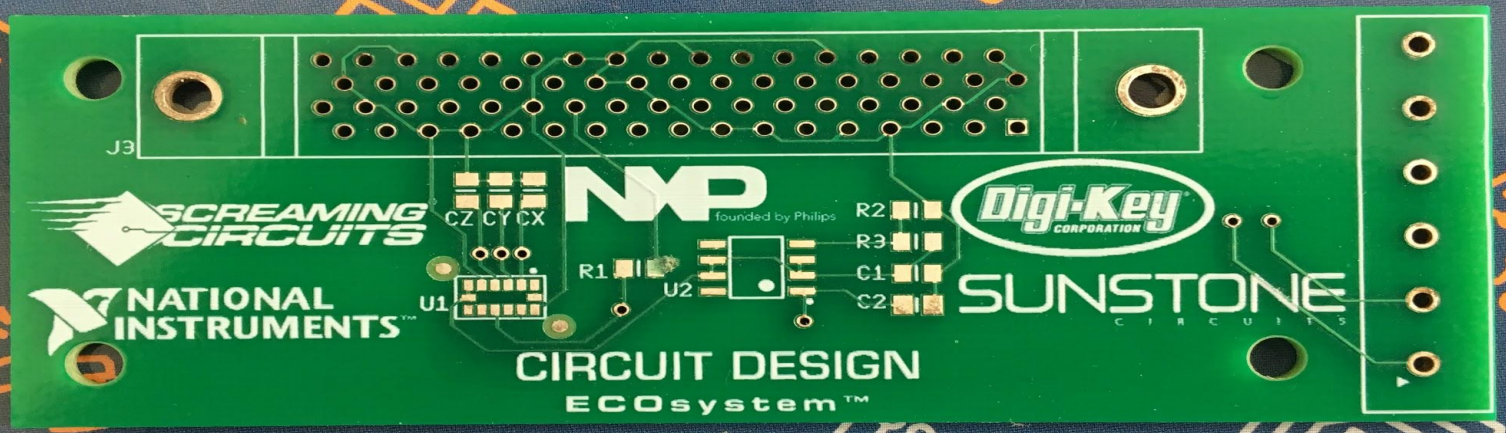
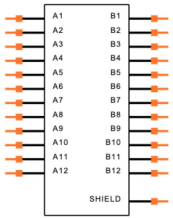
Why Libraries Matter


J3
SCREAMING CIRCUITS
CZ CY CX
NXP
founded by Philips
Digi-Key
CORPORATION
R2
R3
C1
C2
R1
U2
U1
NATIONAL INSTRUMENTS
SUNSTONE
CIRCUITS
CIRCUIT DESIGN
ECOsystem™

What is the scope of today's talk?

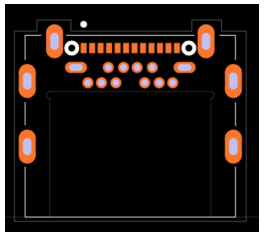


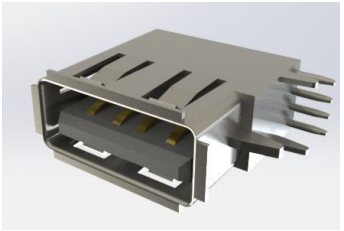
Schematic Capture & Simulation

Each component requires a **schematic symbol** which describes the pin functions and types. Engineers may also simulate their designs.

PCB Layout

The **footprint** is used when designing the physical layout of the circuit board. It describes where the component will get soldered onto the board





Mechanical Design

To see if a PCB will fit within the casing, **3D models** are used to check for clearances, and other factors.

Why well-defined libraries matter

1. Necessary for ensuring proper manufacturing
2. To enable other CAD tool features to function properly (ex: ERC)
3. Documentation (ensure readability and re-use through consistency)

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Why are libraries so hard to get right?

1. Extremely detail-oriented
2. Lack of datasheet consistency and standards
3. Lack of industry standards or alignment
4. Varying manufacturing capabilities
5. Lack of universal file format
6. Libraries get no glory

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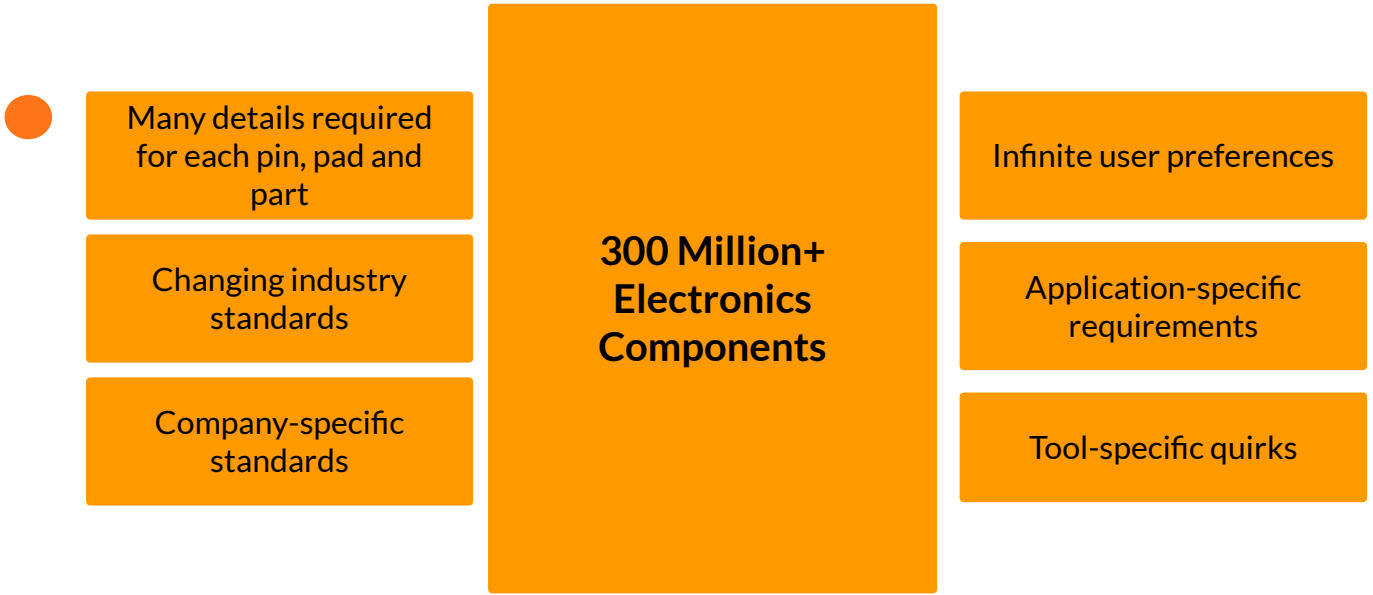
Standards

The scope is massive



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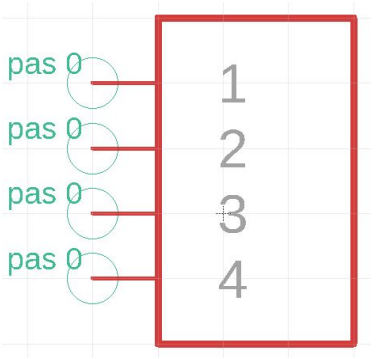
“Never discuss politics, religion or PCB library standards in polite company.”

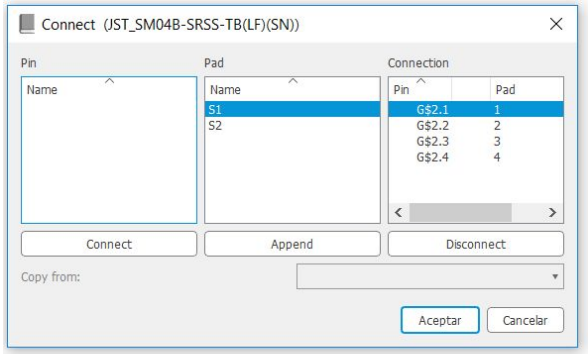
Library Errors - The Basics

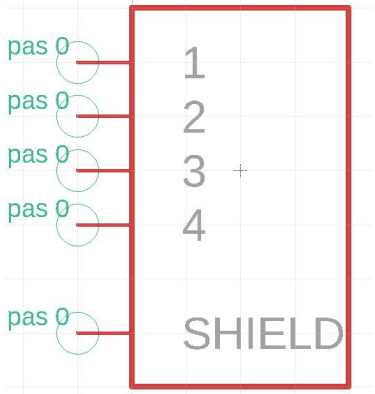
1 Pin mapping issues

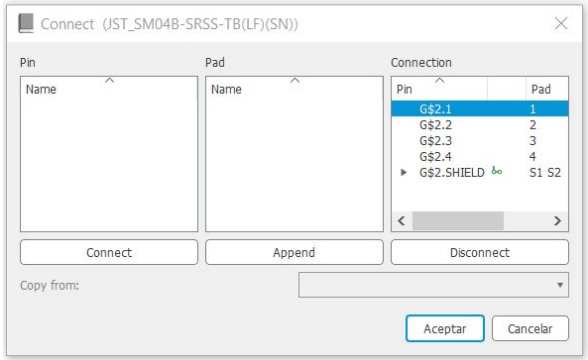
Mapping pins to the wrong pads is a critical mistake, causing improperly connected pins, or even worse, creating shorts.

How to avoid: Double check all connections.









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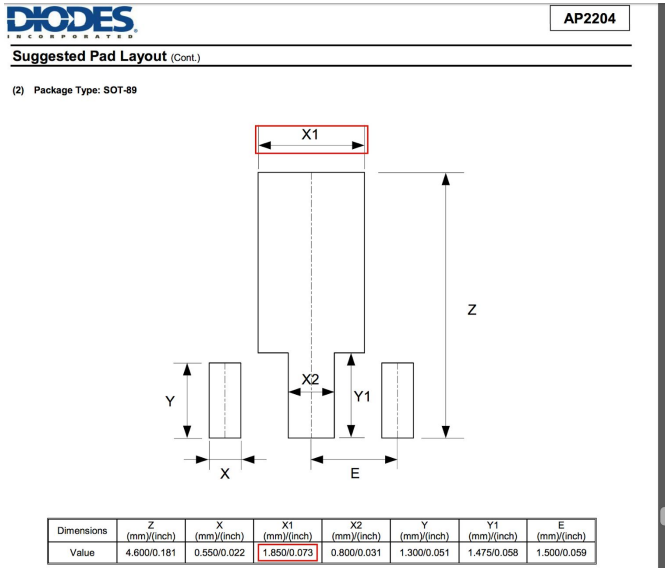
#2 Pad dimension errors

If you are manually drawing pad layouts, it is easy to make mistakes.

If you get one pad length off by a fraction of a millimeter it can cause soldering issues.



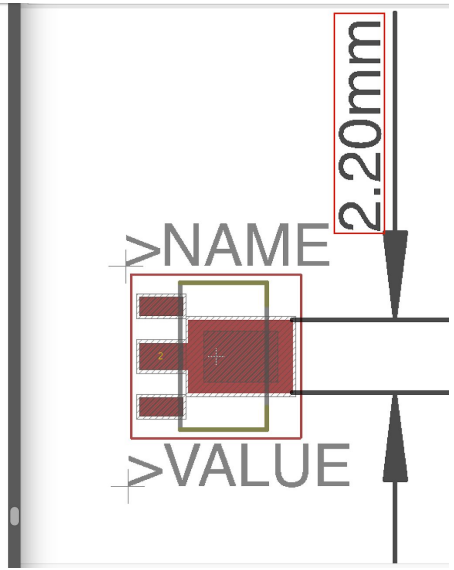
DIODES INCORPORATED

AP2204

Suggested Pad Layout (Cont.)

(2) Package Type: SOT-89

Dimensions	Z (mm)/(inch)	X (mm)/(inch)	X1 (mm)/(inch)	X2 (mm)/(inch)	Y (mm)/(inch)	Y1 (mm)/(inch)	E (mm)/(inch)
Value	4.600/0.181	0.550/0.022	1.850/0.073	0.800/0.031	1.300/0.051	1.475/0.058	1.500/0.059



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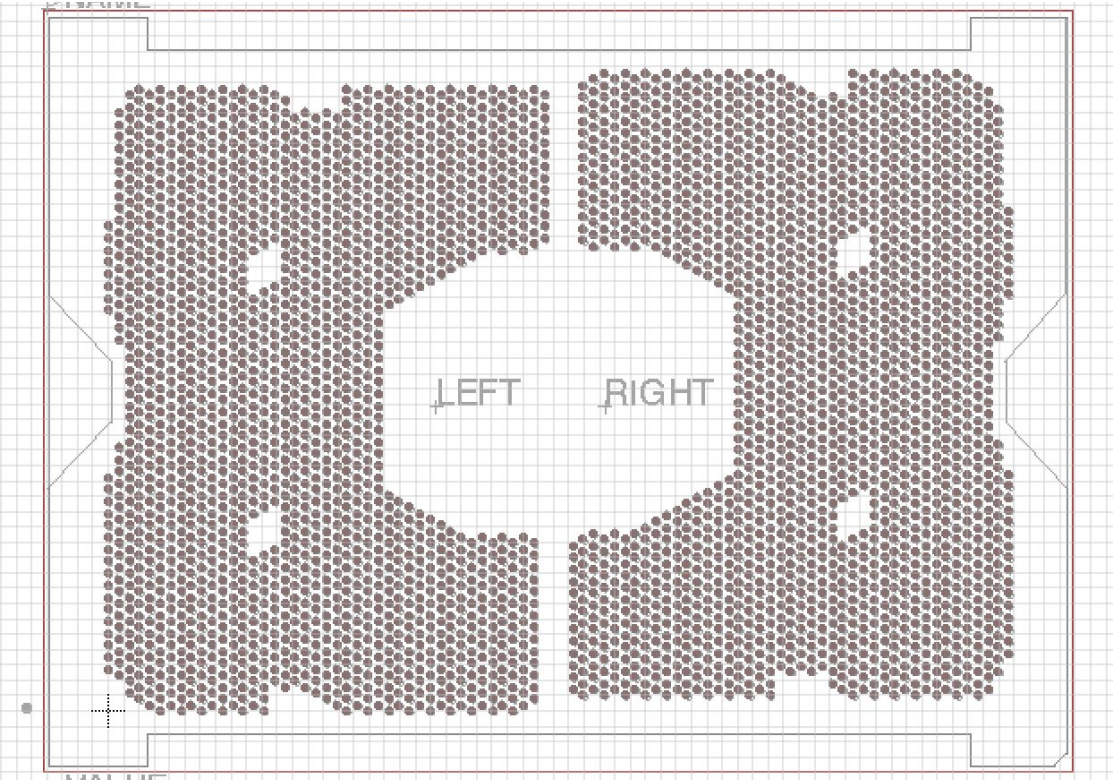
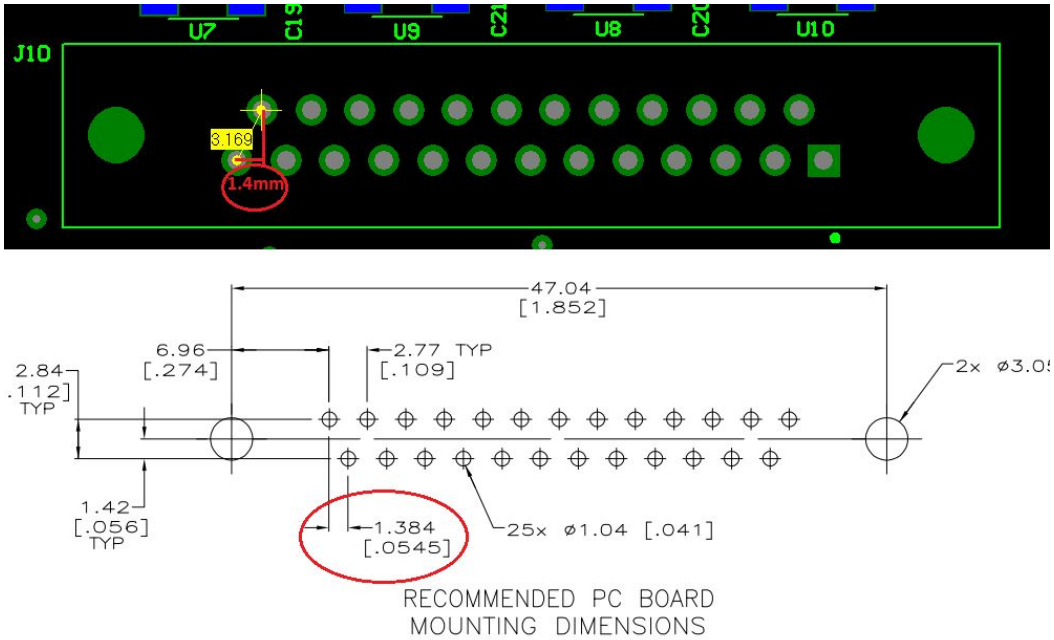


#3 Rounding dimensions

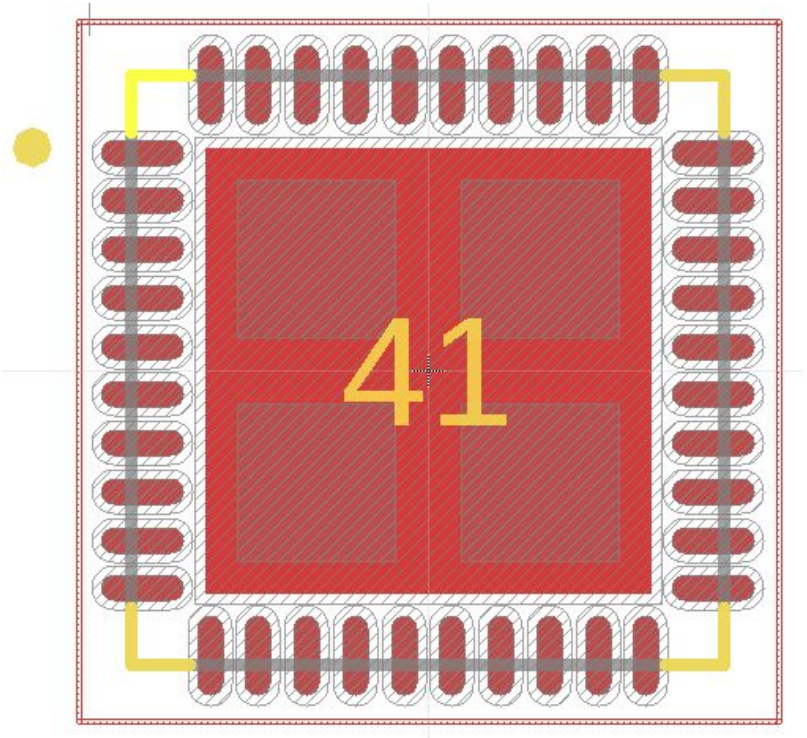
During conversion of metric to imperial units or vice versa, units should never be rounded



#4 Silkscreen too close to pads

One of the most common issues seen in library design is silkscreen overlapping exposed copper on pads.

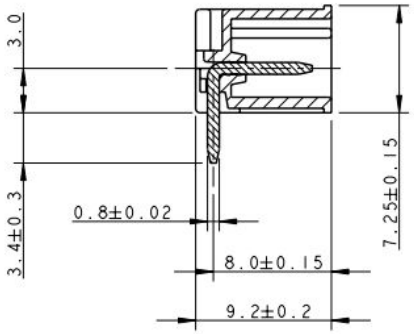
If this happens it could inhibit the solder from flowing and will result in a bad joint.

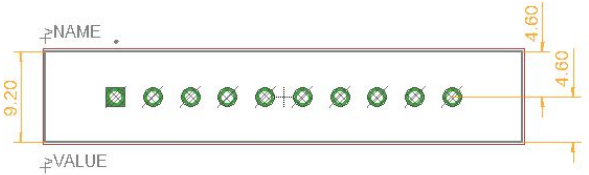


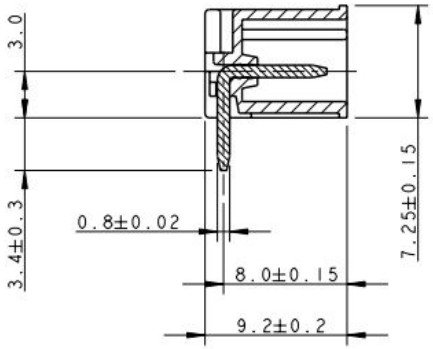
#4 Wrong outline dimensions

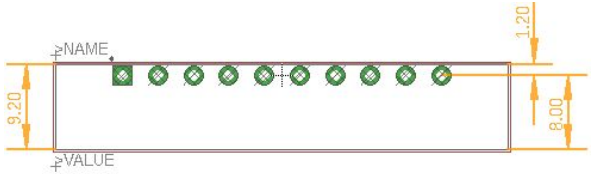
Wrong component outline and courtyard dimensions will cause overlapping of nearby components in the PCB and could produce critical manufacturing issues.

Confusing component outline dimensions may result in trying to fit a RA header on a vertical header footprint, or vice versa.



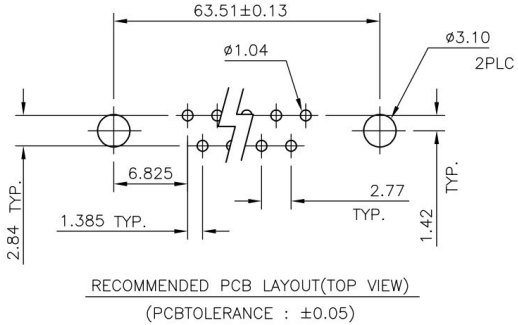


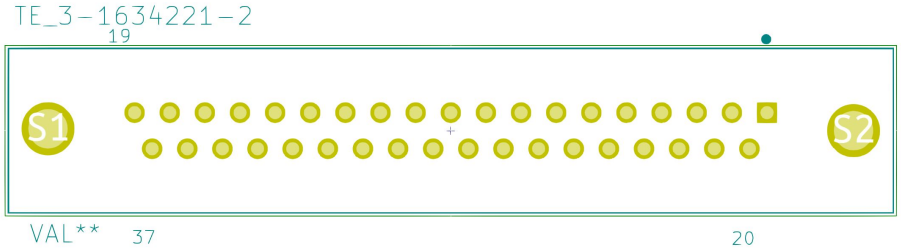




#5 Wrong pin sequence

Some connectors are numbered from top to bottom, others are numbered from left to right. If the pin numbering of your footprint is incorrect you'll have wrong connections.





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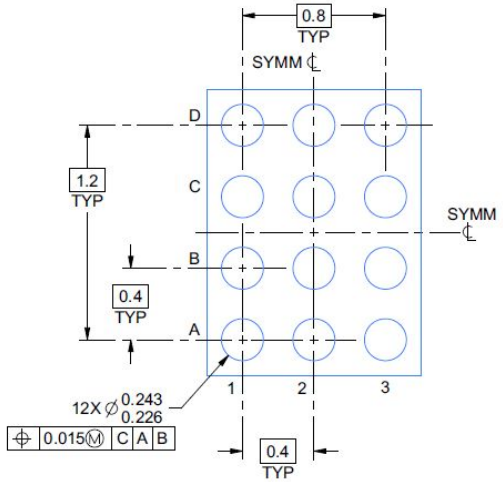
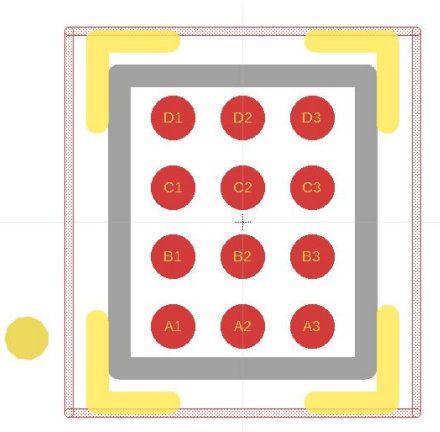
Library Errors - The Ones Even Pros Miss

#1 Mirrored views

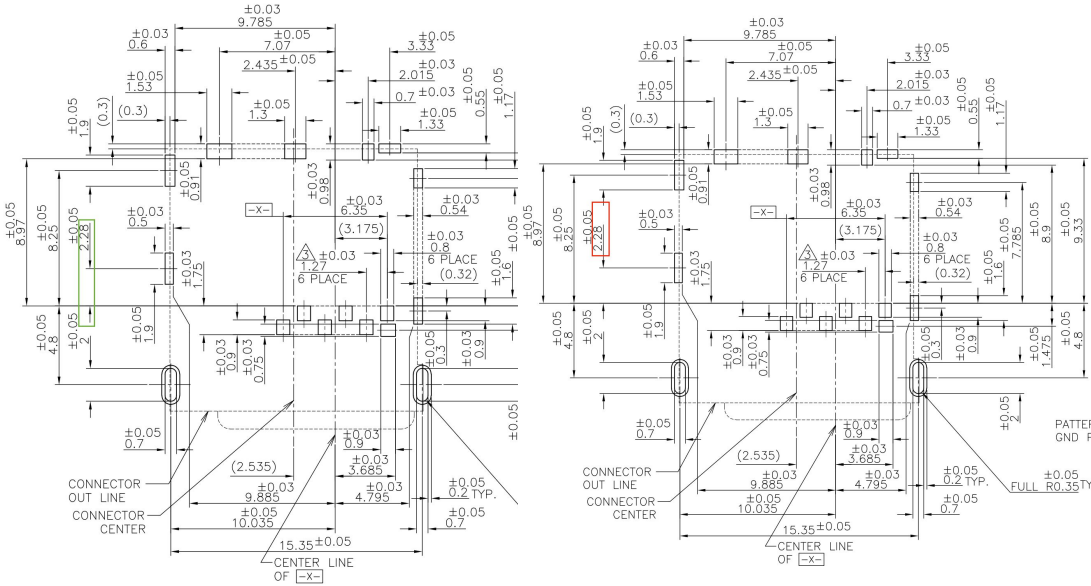
This occurs when the top view of a part is mistaken for the bottom view. Generally, component vendors draw based on the top view. But occasionally, they'll do the opposite.





#2 Wrong or misinterpreted datasheets

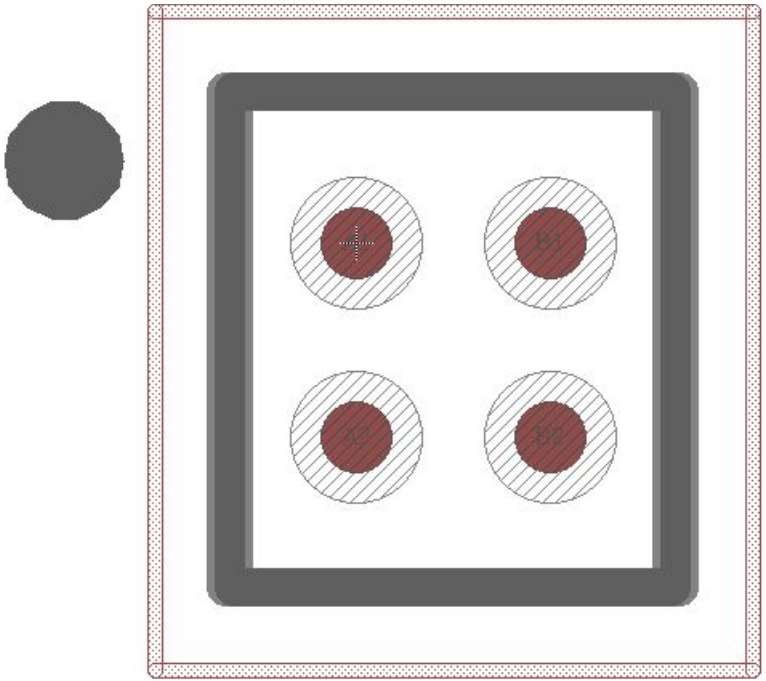
Learning to interpret datasheets and paying attention to the details is key. For senior engineers, many errors result from datasheet misinterpretations.



#3 Wrong centroid

The center-of-mass of a part is defined by an X-Y location and this concept is known as the part centroid.

If your centroid coordinates are off then the pick-and-place machine will try to pick components from a location that may not stick well to the package.



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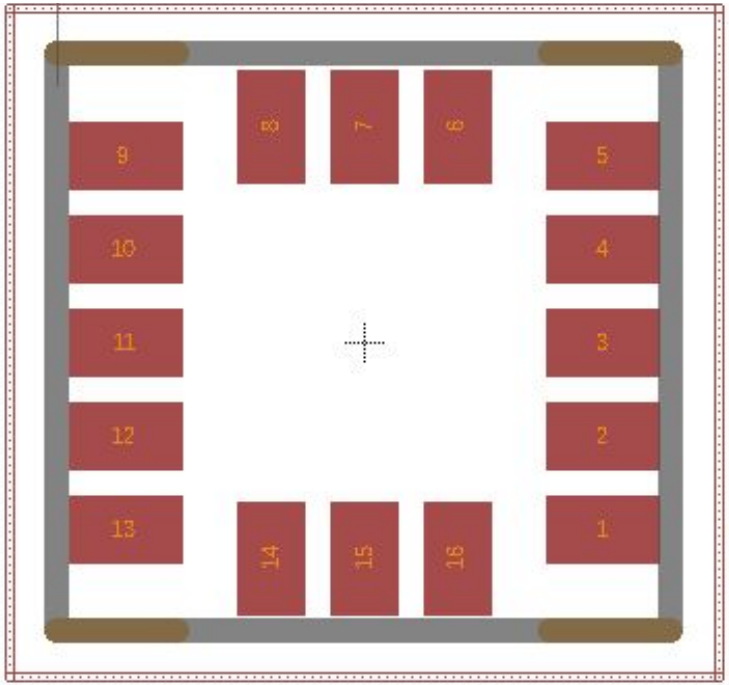
#4 Wrong component zero orientation

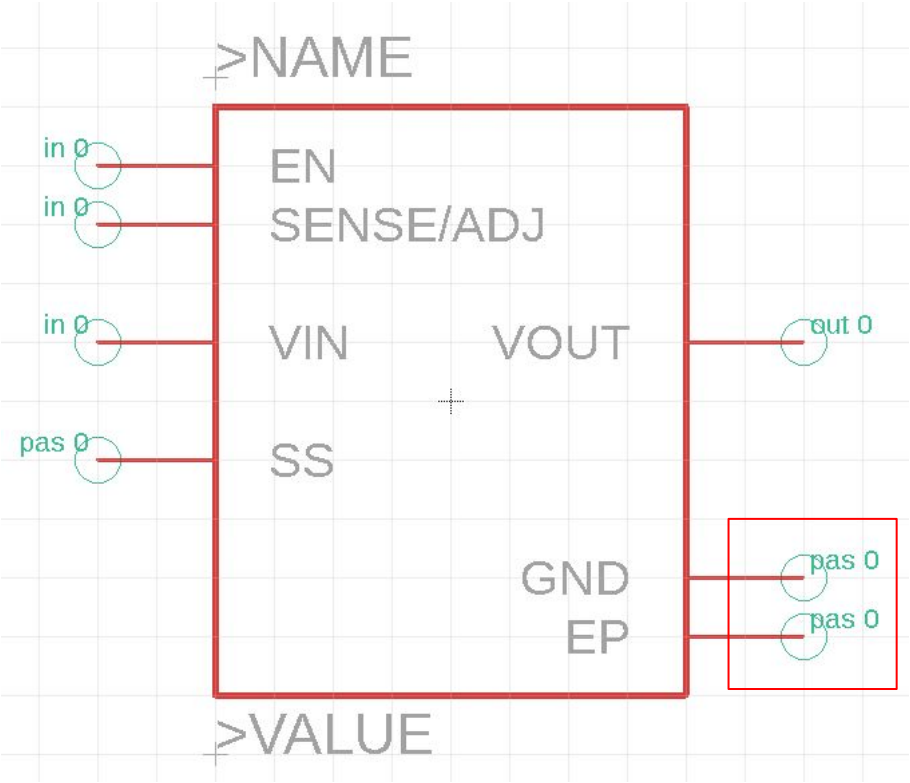
The zero component orientations expressed in IPC-7351 are defined for the description of electronic component orientations. They’re important for the pick-and-place to figure out how to place the component during assembly



#5 Improper pin definitions

To define the logical direction of signal flow in a schematic symbol, you need to understand the function of the component you are creating.

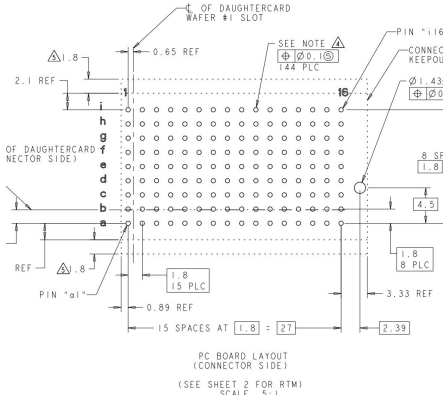
If pins are not defined properly ERC checks will not work .

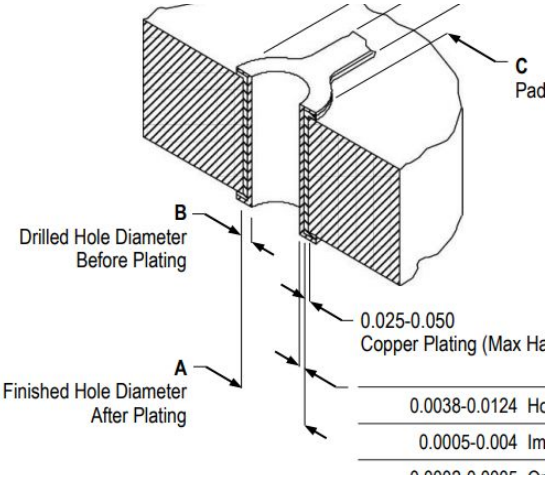


#6 Misinterpreting plated versus non-plated hole sizes

Accidentally overlooking this and choosing the wrong finished hole size, can cause holes to be too big.

Most manufacturers assume that the size you specify is the “finished hole size” (after plating).





CONNECTOR	TIER	DIMENSION		
		A (Nominal)	B	C
Vertical Receptacle (Backplane)	1, 2	0.56 (Ref)	0.63-0.67	1.02
Right-Angle Plug (Daughtercard)	1	0.56 (Ref)	0.63-0.67	1.02
	2	0.46 (Ref)	0.53-0.57	0.92

Figure 4

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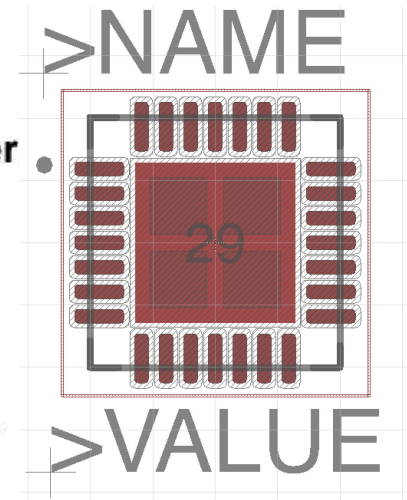
#7 Not breaking up solder paste in thermal pads

This can cause float where the part is too high and doesn't connect to pins.

QFN mounted with too much solder in center pad area

QFN mounted with reduced solder paste in center pad area



Question: Do different assembly shops handle footprints differently?

Question: Do different assembly houses require different footprints?

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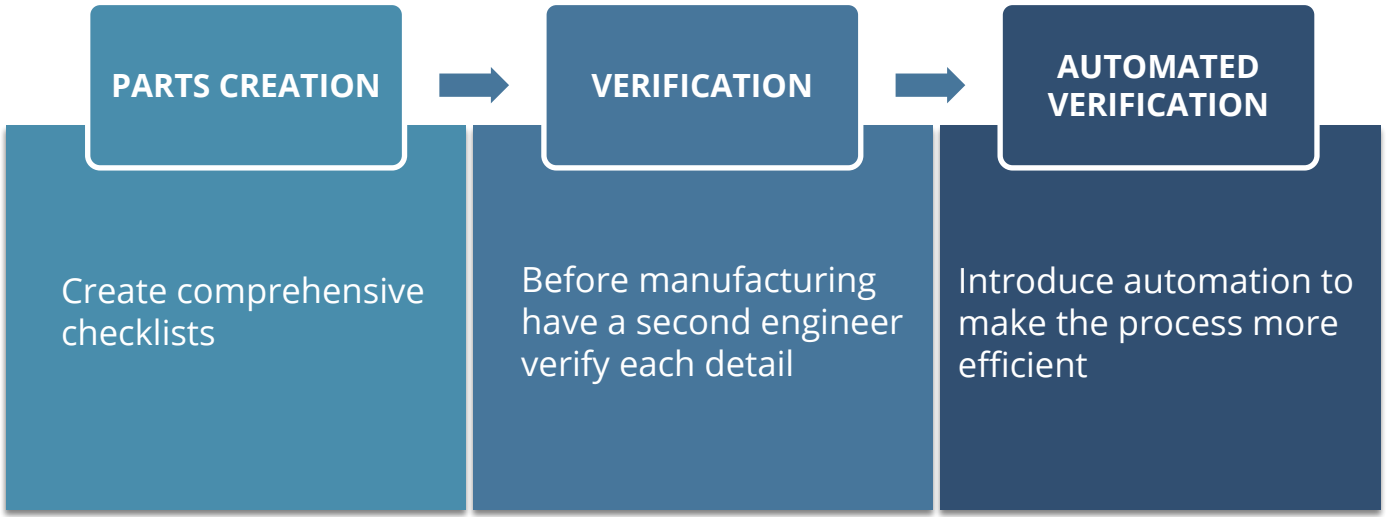
Checklists & Verification

The need to verify libraries

- Regardless of whether you got a library from the web, component vendor website, or made it yourself, it always needs to go through a thorough verification process

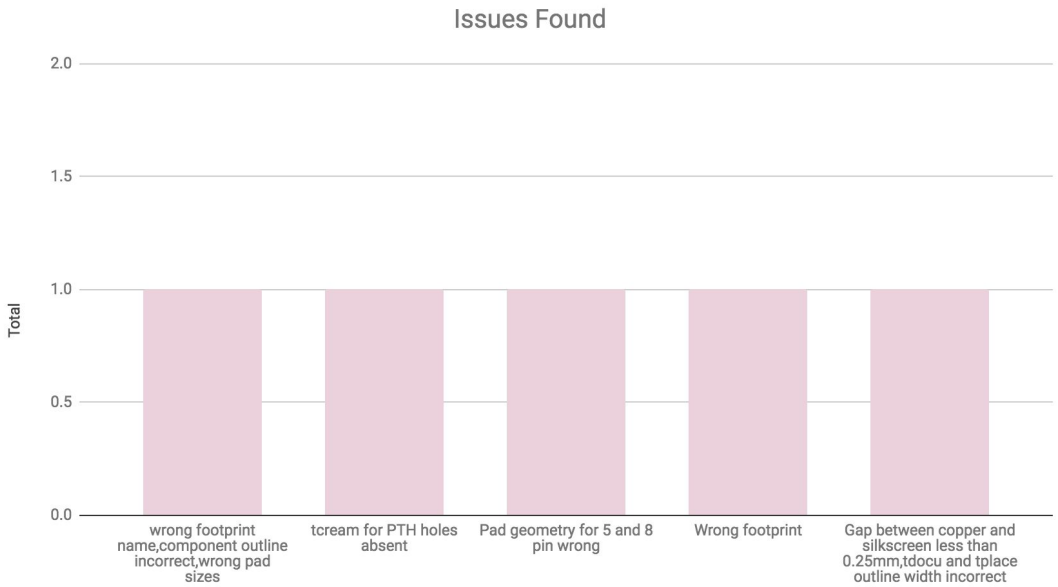
Step 1: Define the process



Step 2: Create, maintain and enforce checklists

- [ ] Package name should follow IPC naming convention
- [ ] Follow IPC Zero orientation with pin 1 upper left
- [ ] Ensure that the pin mapping is the top view of the chip and not a mirrored view from the bottom.
- [ ] Ensure the spacing between silkscreen and copper is at least 0.25mm + 0.0635 (line width / 2) = 0.32
- [ ] Body outlines or any part of the footprint created with the tPlace layer should not collide/overlap with the pads.
- [ ] Add a body outline (0.127 mm lead width) in tDocu and tPlace layer
- [ ] Exposed pad's tCream layer (paste) should be 40%-50% of the area of the exposed pad
- [ ] Add a tKeepout outline with 0.05mm lead width enclosing the footprint (0.25mm away from the pads/component outline)
- [ ] Irregular-shapes pads (including tcream, tstop, tkeepout) created with polygon tool, lead width should be 0.001 mm (not zero)
- [ ] For components with cut-outs, draw the cut-out in Milling layer using line width 0 mm

Step 3: Measure, learn & iterate



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Step 4: Automate

- To prevent human error, and minimize library efforts, automation is your friend!
- What parts of the creation and verification processes can you automate?

What tools are available to help?

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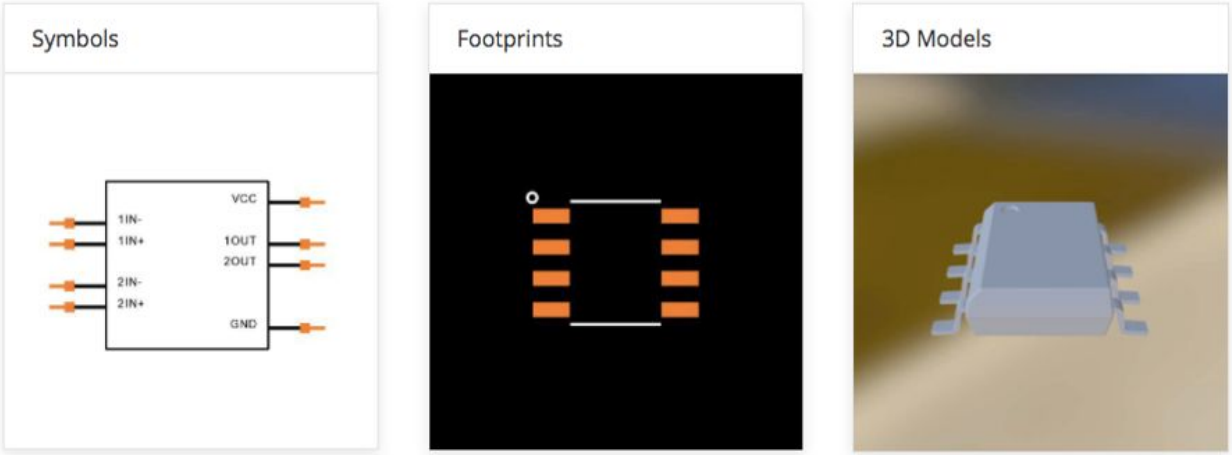
- Symbols, footprints, and 3D models for millions of electronics components



cadence OrCAD Altium CS EAGLE Mentor A Siemens Business KiCad PCB Design Software

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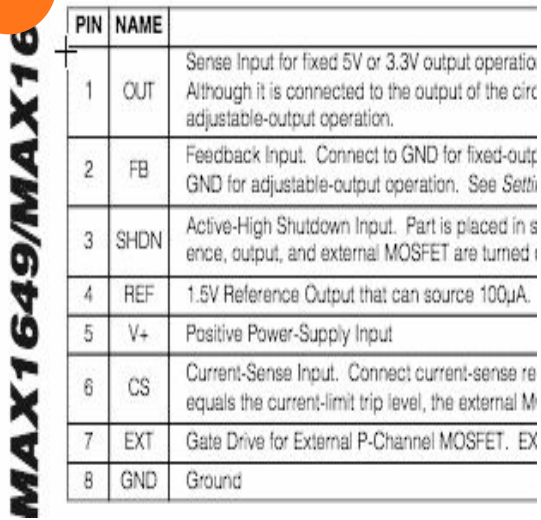
InstaBuild

- Create schematic symbols using simple computer vision and OCR in minutes

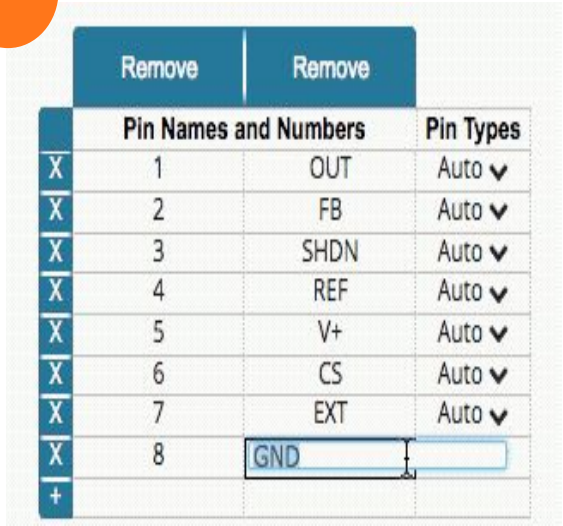
1



MAX1649/MAX16

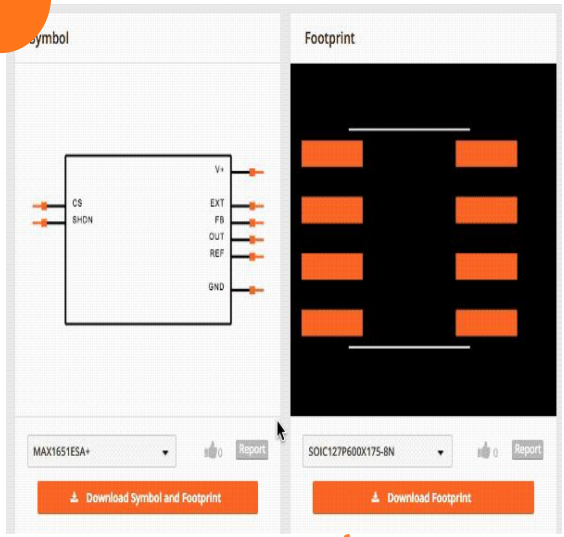
PIN	NAME	
1	OUT	Sense Input for fixed 5V or 3.3V output operatio Although it is connected to the output of the circ adjustable-output operation.
2	FB	Feedback Input. Connect to GND for fixed-outp GND for adjustable-output operation. See *Setti*
3	SHDN	Active-High Shutdown Input. Part is placed in s ence, output, and external MOSFET are turned
4	REF	1.5V Reference Output that can source 100µA.
5	V+	Positive Power-Supply Input
6	CS	Current-Sense Input. Connect current-sense re equals the current-limit trip level, the external M
7	EXT	Gate Drive for External P-Channel MOSFET. EX
8	GND	Ground

2



	Remove	Remove	
	Pin Names and Numbers		Pin Types
X	1	OUT	Auto
X	2	FB	Auto
X	3	SHDN	Auto
X	4	REF	Auto
X	5	V+	Auto
X	6	CS	Auto
X	7	EXT	Auto
X	8	GND	
+			

3



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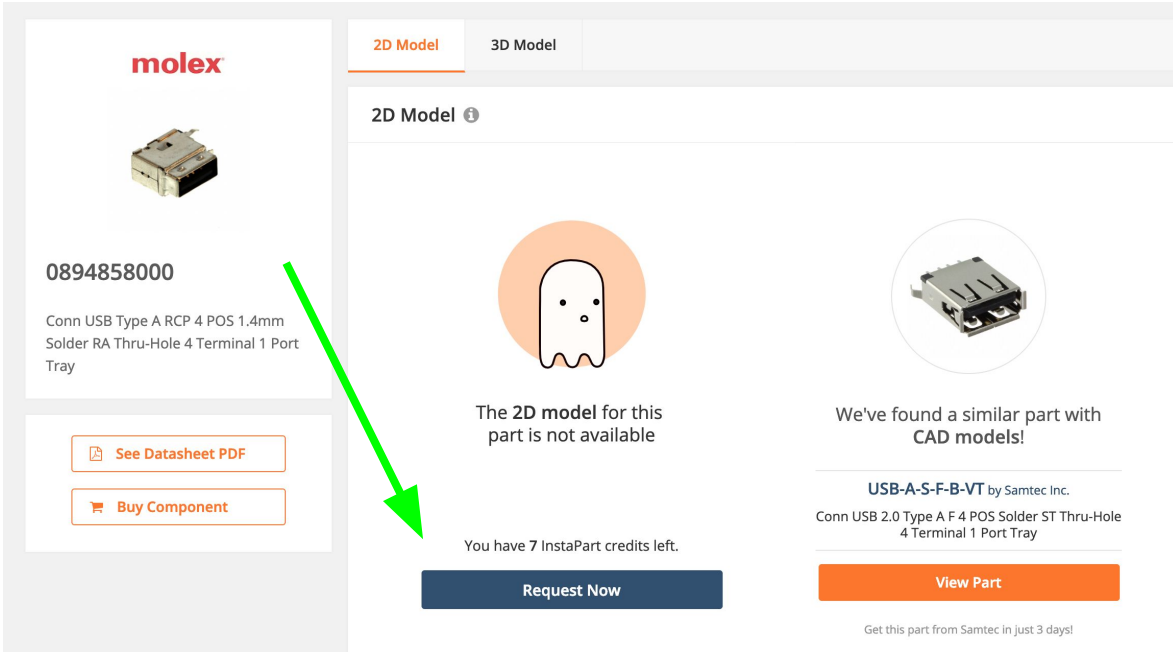
InstaPart

- Request any symbol & footprint and get it in 24h



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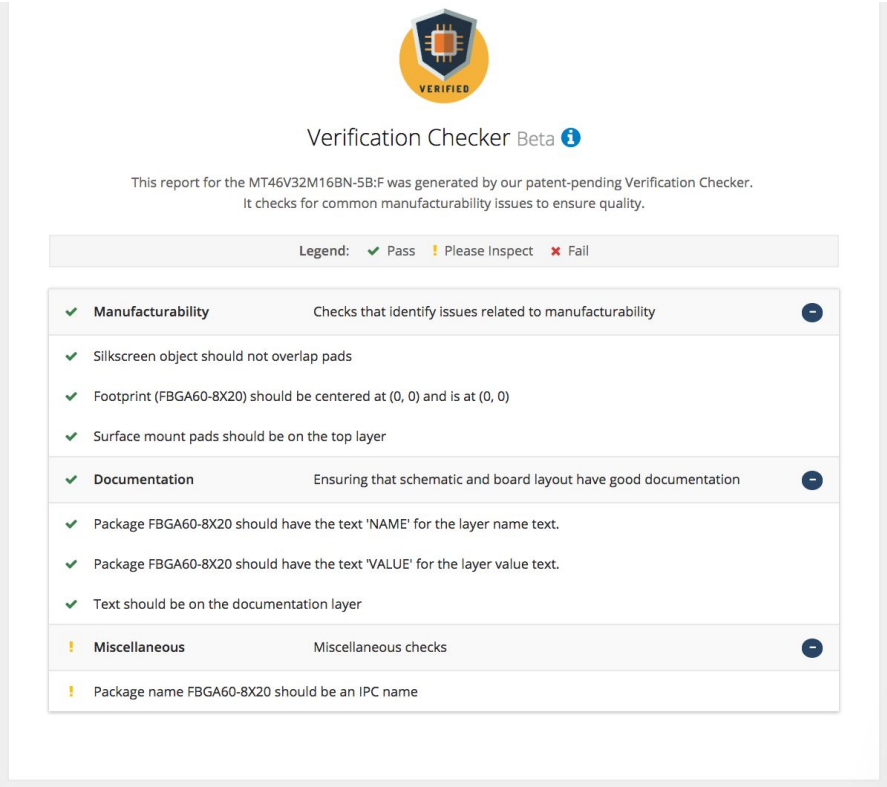
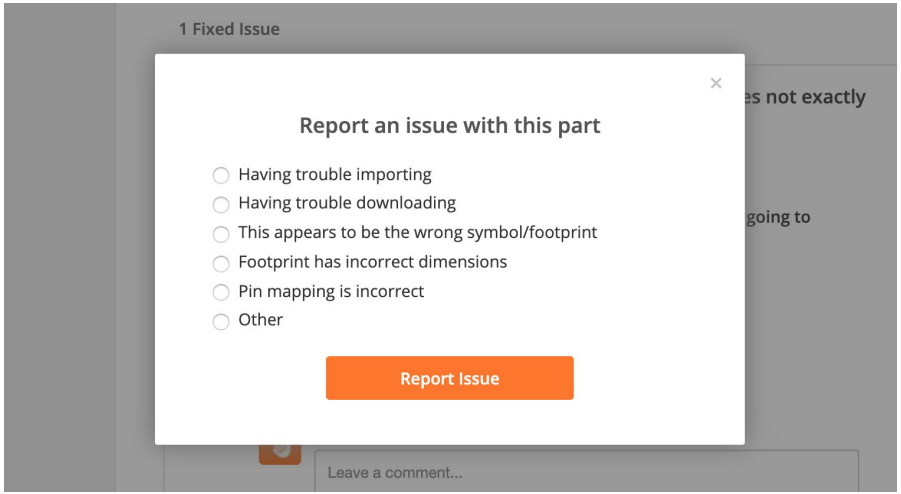
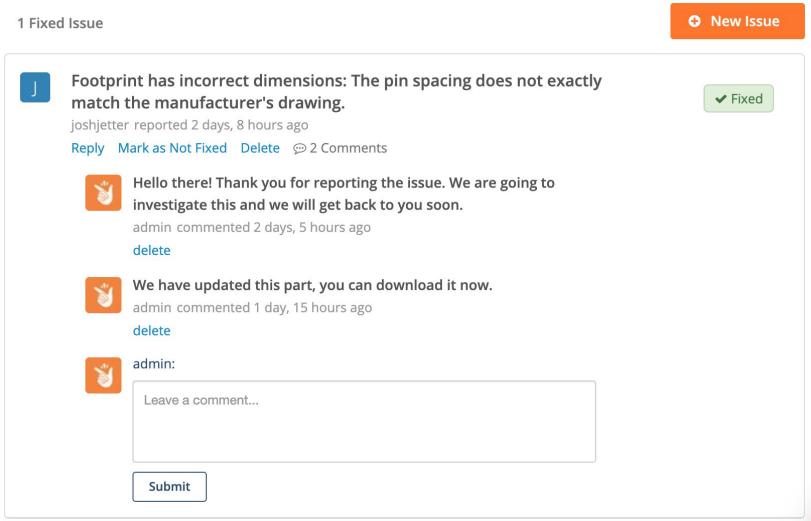
- Validate libraries in real-time

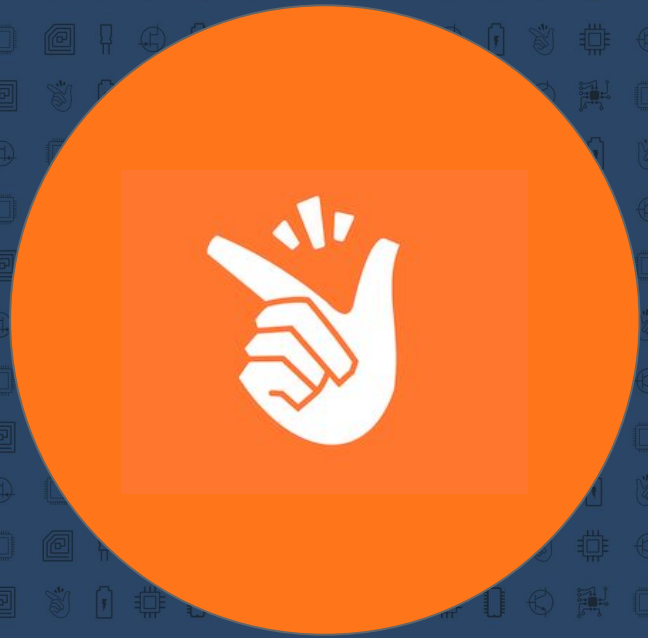


- Share and learn from the engineering community





Summary



Summary

1. Libraries are necessary for reliable manufacturing, readability, and ERC
2. Implementing verification checklists and processes is essential
3. Other tools can help increase the efficiency and productivity

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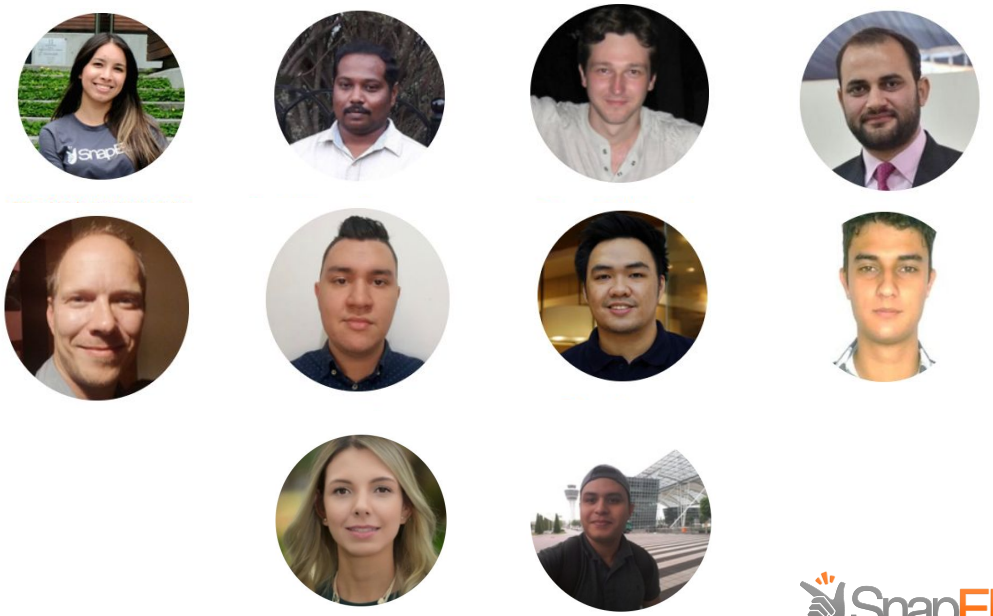
Thanks to SnapEDA's Component Engineering Team!



Questions?

natasha@snapeda.com