PCB Fabrication Enabling Solutions

June 3, 2015

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Military/Aerospace Drove Advanced High Rel Technology…

C-130

C-17

Apache

JSF

F-22

F-18

MIDS-LVT1

JEM Radio

KC-135

Apollo

F-117

T-38

RAM

B-2

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Until the late 90's !

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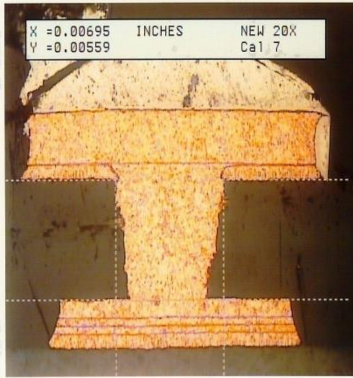
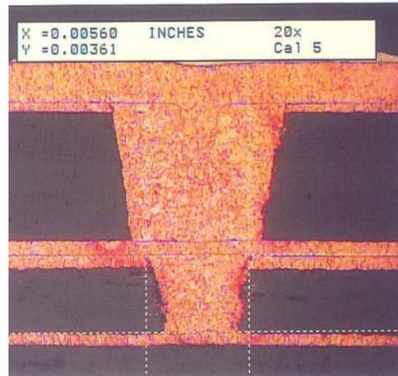
Then things really got complicated…

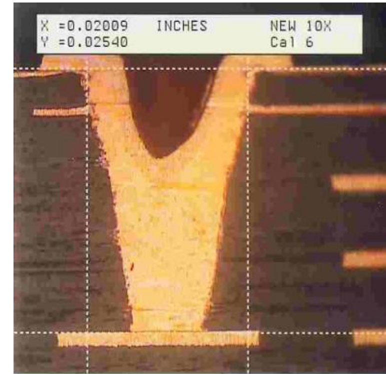
SMV®



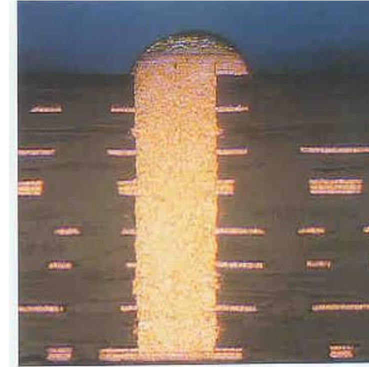
DpMV™



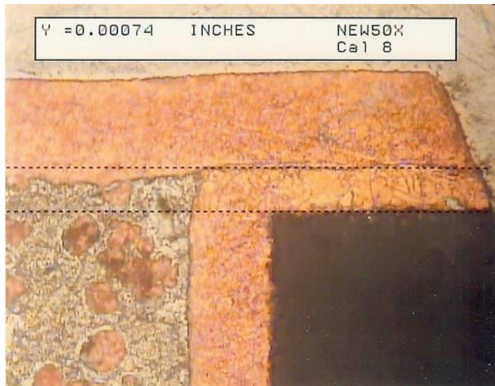
DpSMV™



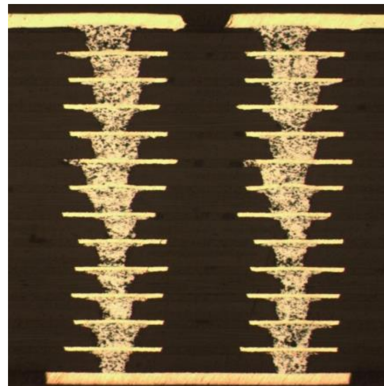
DpBV™



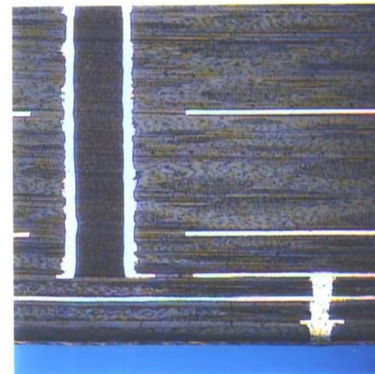
ThermalVia™



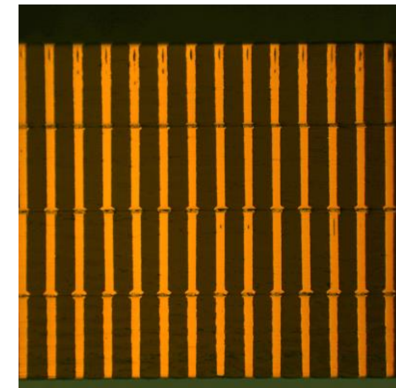
FLAT-WRAP™



NextGen-SMV®



HDI-Link™



Sub-Link™

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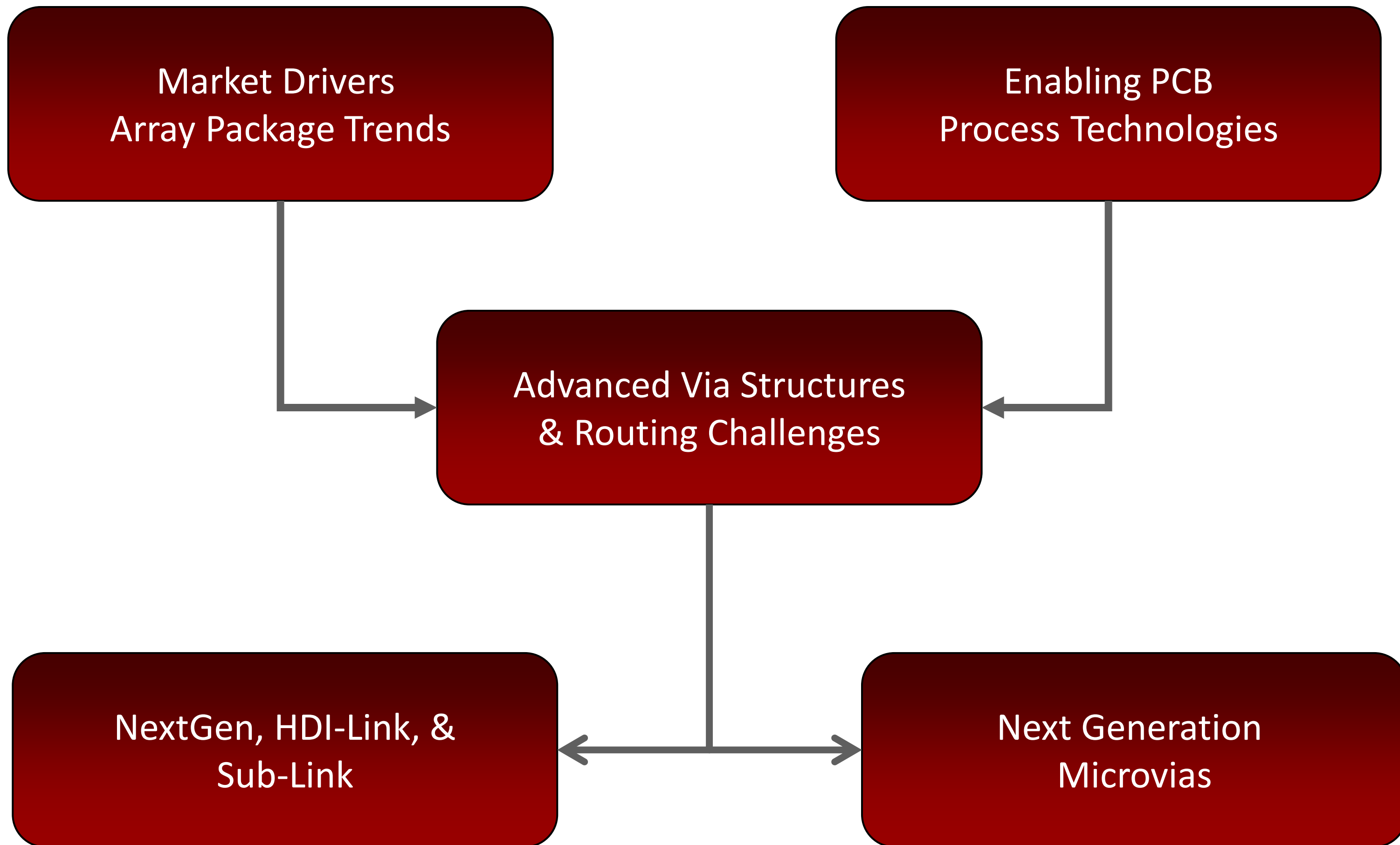
Today's Agenda



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Increasing Complexity

Today's PCB require a complex blend of many process technologies that must work in concert to provide a solution…

- **Small die, shrinking geometries; pushing the limits of annular ring, aspect ratio, and sub 3 mil line & space**
- **Exponentially increasing I/O; Blind, buried, and laser drilled microvias to increase routing channel density**
- **Stacking microvias to accommodate fine pitch devices**
- **Minimizing registration shifts, maximizing resolution**
- **Optimizing Copper plating (Direct Current vs. Reverse Pulse Plating)**
- **Materials and lamination limits vs. design constraints**
- **Improving outer layer etch on multiple lamination designs with FlatWrap**
- **Thermal management**

…The end goal is to put all the pieces together and examine the design and fabrication interactions.

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PCB Market Drivers & Array Package Densities

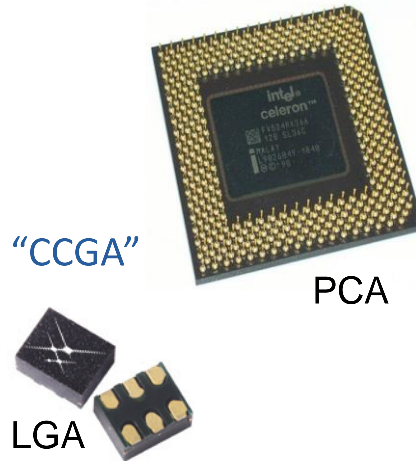
How have Array Packages evolved and what is their impact on PCBs ?

Definition of an Array Package:

Array packages are defined as component packages where the I/O's (Input/Output) or leads can be defined in a "Matrix" pattern in terms of rows and columns. Array packages can provide greatest number of I/O's per unit area of any package since the entire bottom of the package can be used for connections.

Types of Array Packages

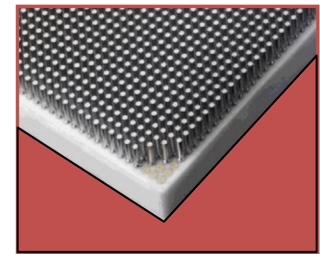
- Pin Grid Arrays "PGA"
- Ball Grid Arrays "BGA"
- Ceramic Column Grid Array "CCGA"
- Land Grid Array "LGA"
- Flip Chip



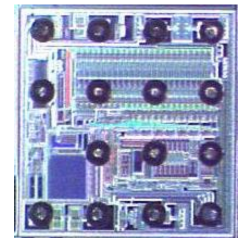
PCA

LGA

BGA



CCGA

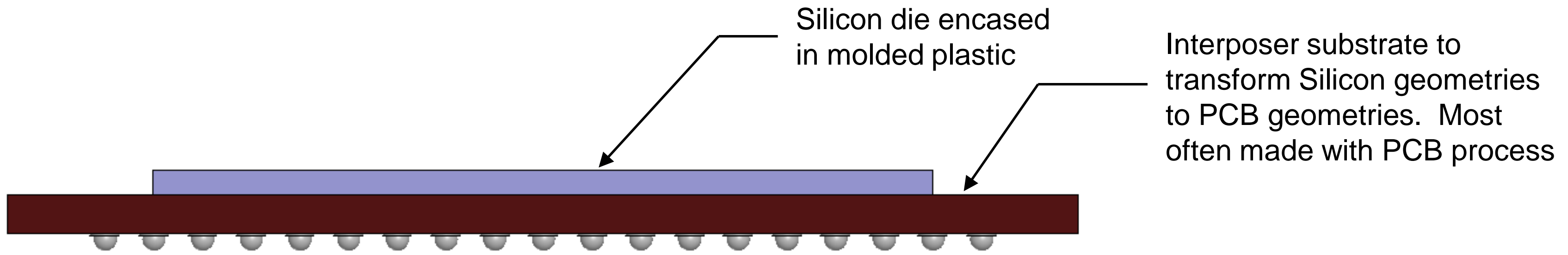


Flip Chip

Design Considerations

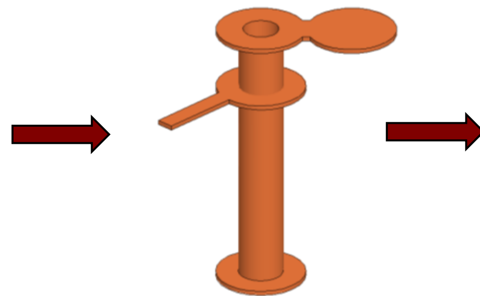
- All Array packages present some form of routing challenges in the design process
- Special consideration must be given to board design with respect to assembly

Ball Grid Arrays "BGA"

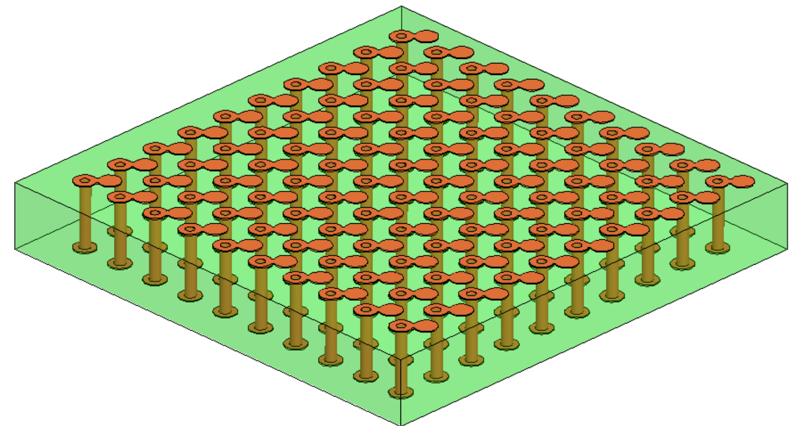


1.27 mm 0.8 mm 0.65 mm 0.4 mm
1.0 mm 0.75 mm 0.5 mm 0.25 mm

357 I/O BGA Package



Drilled hole diameter and
Pitch are reaching limits
and restricting routing



Through hole PCB

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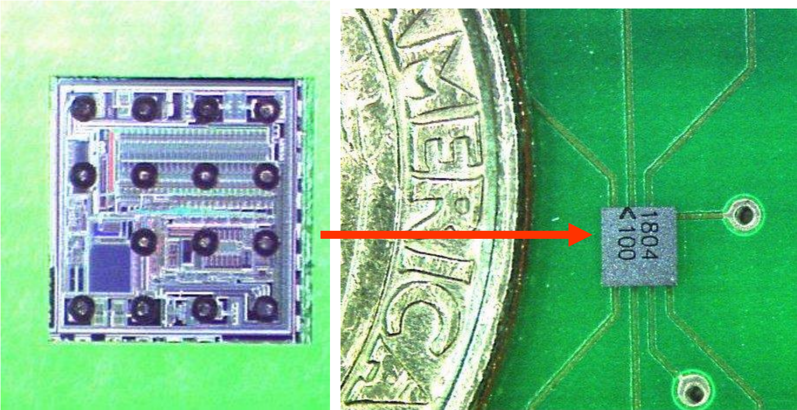
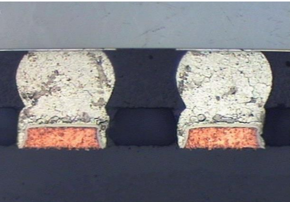
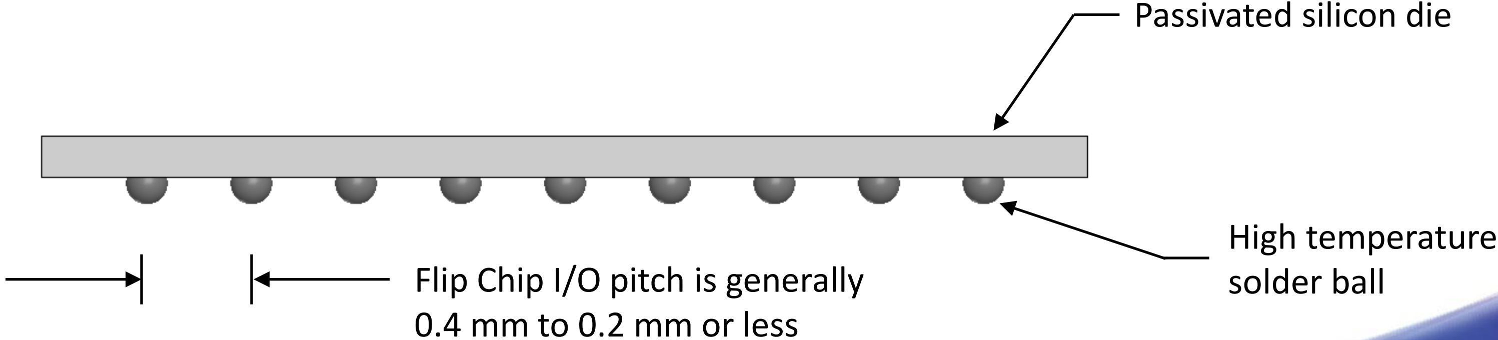
Flip Chip (No Package!)



Flip Chip

- Flip Chip is the extreme form of an array package. High temperature solder balls are attached directly to the silicon die.
- Extremely fine ball pitch can push the limits of PCB geometries
- Larger silicon dies can not tolerate any warpage in the PCB substrate
- Silicon has a much lower CTE than PCB materials (2.5 PPM vs 18 PPM). To prevent damage to the interconnect on very large silicon die, the PCB must be designed with materials with a lower CTE than conventional epoxy or polyimide materials





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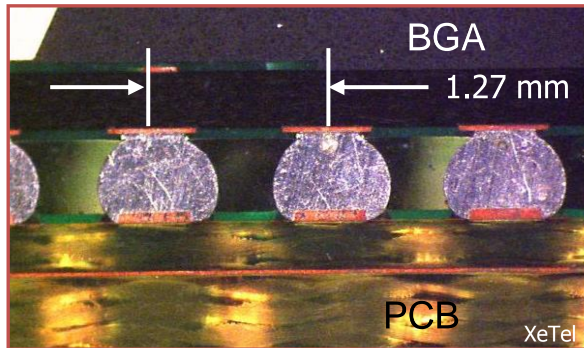
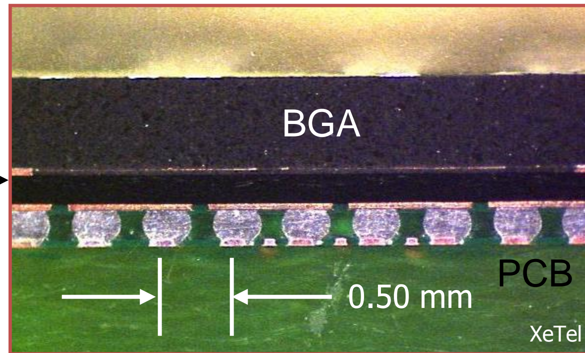
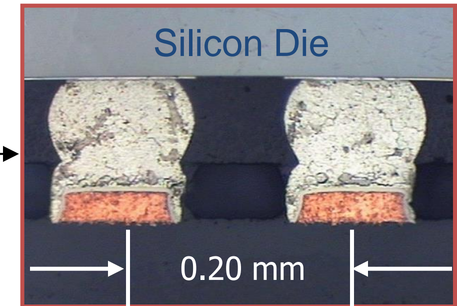
Density Trends In Array Packages
Assembled Cross-Section Views

Increasing I/O Density Chip Scale Packaging Flip Chip Packaging







1.27 mm BGA package
Localized via density
62/cm² (400/in.²)

20 x 20

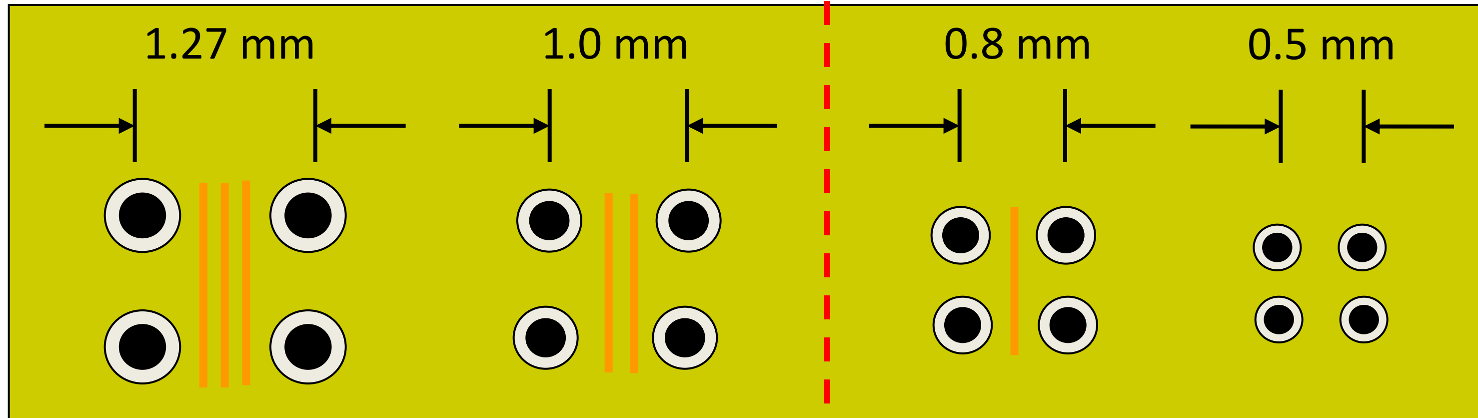
6.45 x Increase
in via density

0.50 mm BGA package
Localized via density
400/cm² (2580/in.²)

6.25 x Increase
in via density

0.20 mm Flip Chip
Localized via density
2500/cm² (16,129/in.²)

Circuit Density & Mechanical Drilling limitations



	1.27 mm	1.0 mm	0.8 mm	0.5 mm
Drill dia.	**0.010" (250 µm)**	**0.010" (250 µm)**	**0.008" (200 µm)**	
Pad dia.	**0.022" (550 µm)**	**0.019" (475 µm)**	**0.018" (450 µm)**	**0.010" (250 µm)**
Line width	**0.004" (100 µm)**	**0.004" (100 µm)**	**0.0045" (112 µm)**	**N/A**
Space	**0.004" (100 µm)**	**0.004" (100 µm)**	**0.0045" (112 µm)**	
Thickness	**Up to 0.100"**	**Up to 0.100"**	**Up to 0.062"**	**Escape Only !**

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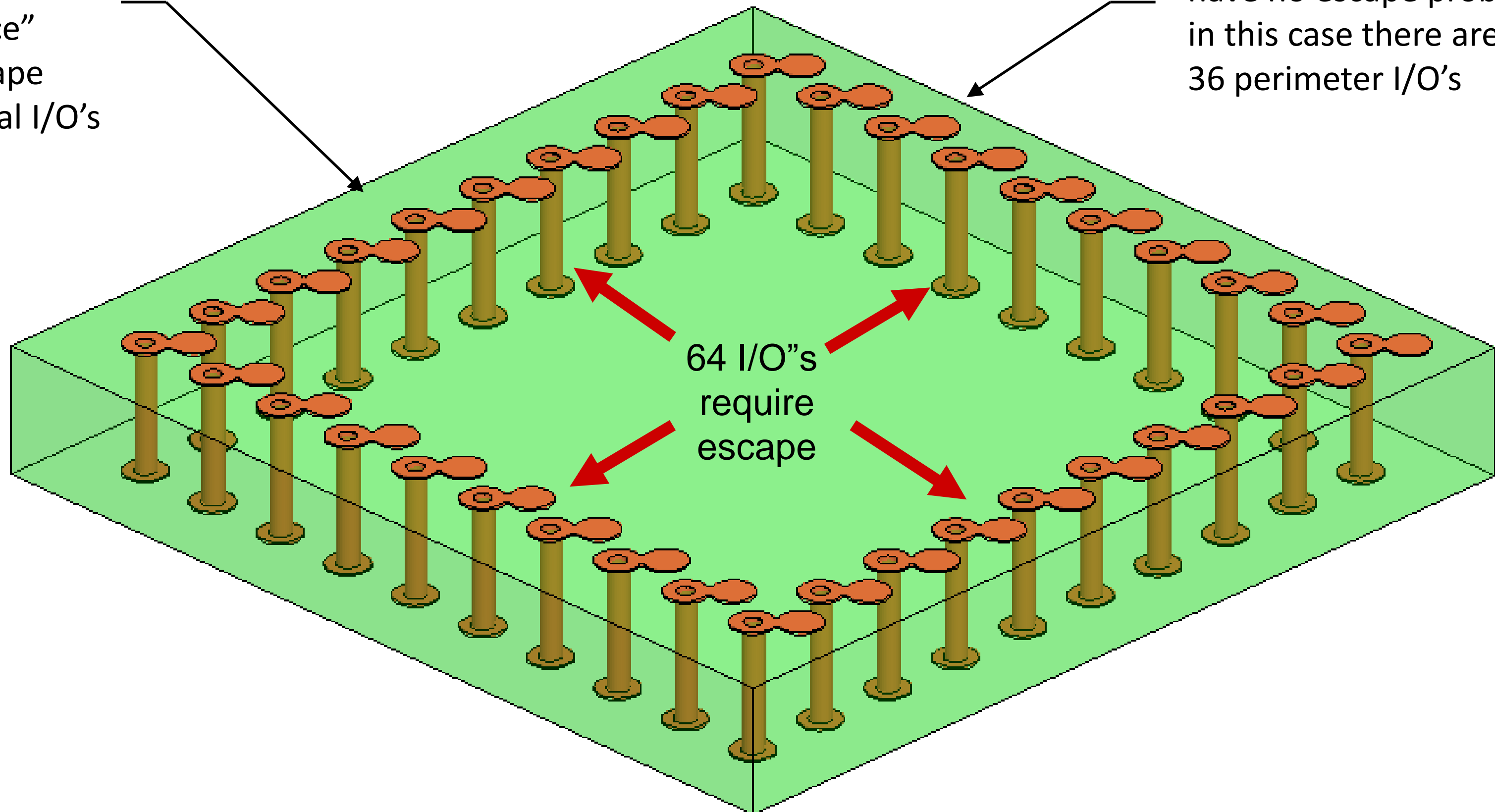
Through Hole Routing dilemma for array patterns

Simplified view of the routing problem

Via holes on the perimeter of the pattern form a "Picket Fence" limiting escape if the internal I/O's

Perimeter I/O's have have no escape problem in this case there are 36 perimeter I/O's



100 I/O BGA Pattern
(Internal vias not shown)

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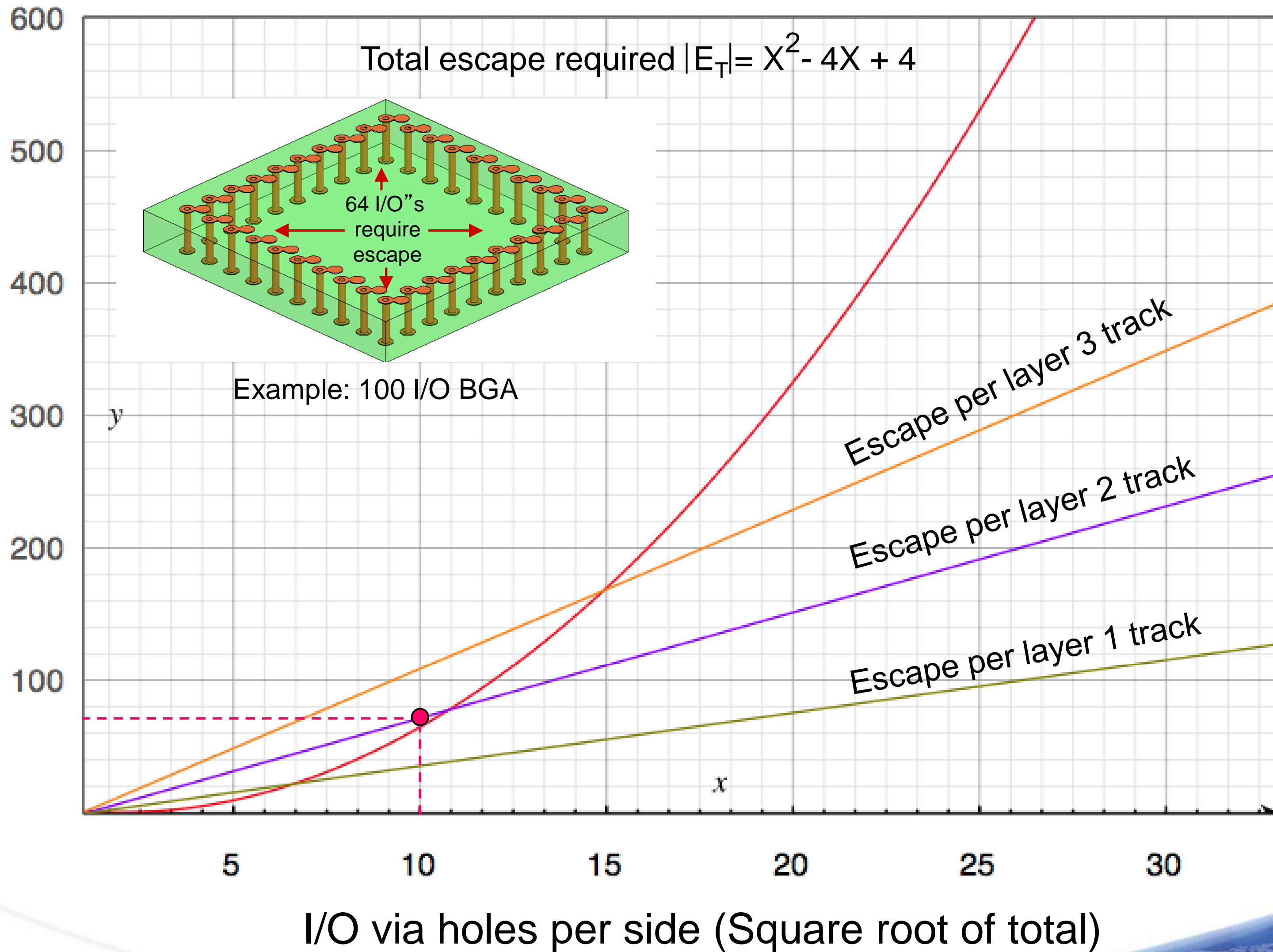
Square Array Escape through Outside Row



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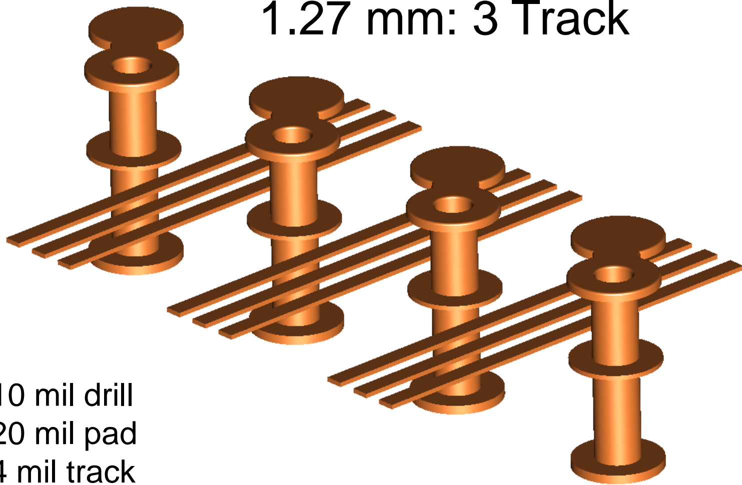
How do we squeeze through the picket fence?

- Determine largest possible via drill diameter with the lowest aspect ratio
- Determine minimum pad diameter to achieve IPC Class II, tangency, or IPC Class III
- Maintain a minimum of 8 mils from the primary drill hole edge to any copper features
- Signal routing channels come in integer values (i.e. 1,2,3….n)
  - Track width and pad diameter should be maximized to take advantage of via or device pitch with respect to the maximum integer value of signal routes (in other words, don’t shrink pads and or track widths if it does not create another signal route !)
  - Signal track width should be selected based on the electrical requirements

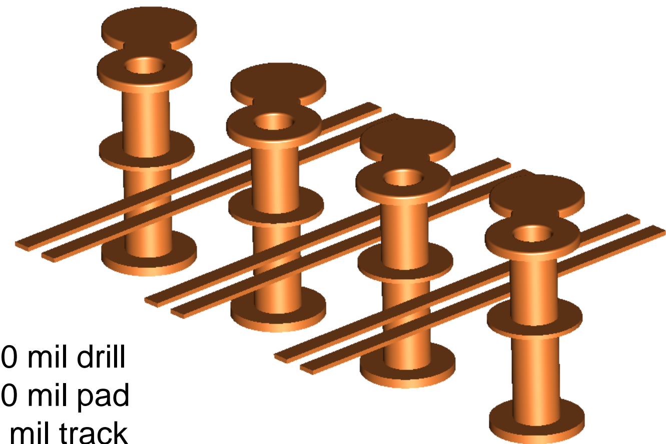
Array Pattern Escape, Through-hole IPC Class 2

1.27 mm: 3 Track



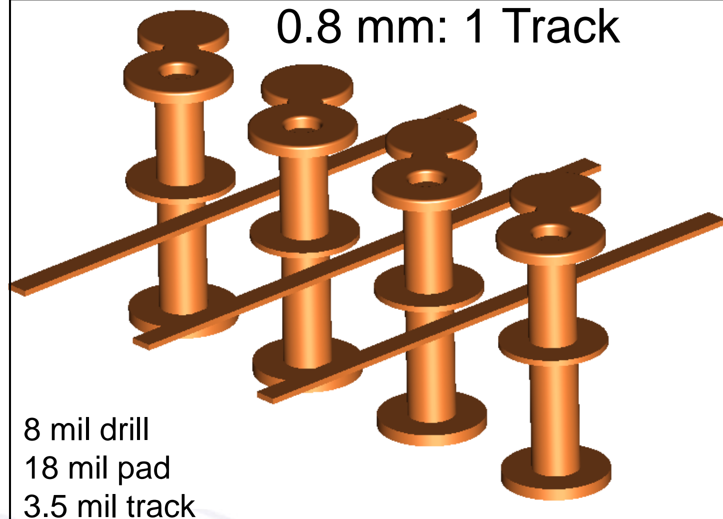
10 mil drill
20 mil pad
4 mil track

1.0 mm: 2 Track



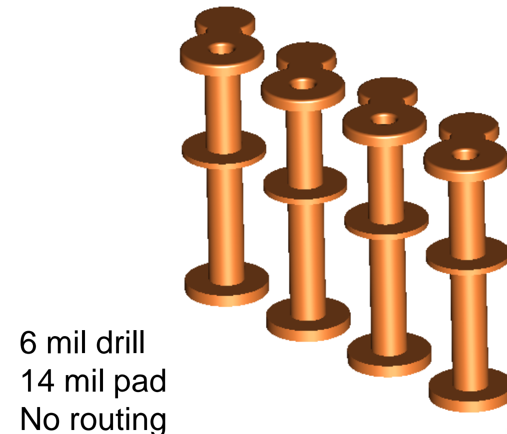
10 mil drill
20 mil pad
4 mil track

0.8 mm: 1 Track



8 mil drill
18 mil pad
3.5 mil track

0.5 mm: 0 Track



6 mil drill
14 mil pad
No routing

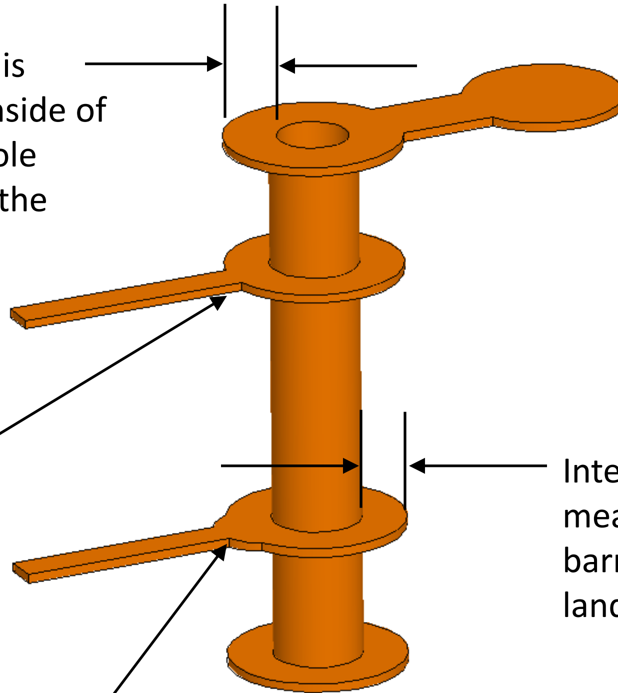
Annular Ring Requirements For IPC Class 2 & 3

Characteristic	Class 2	Class 3
External Plated-through holes	Not greater than 90° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1. The conductor junction should never be less than 50 µm [1,969 µin] or the minimum line width, whichever is smaller.	The minimum annular ring **shall** be 50 µm [1,969 µin]. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1. The minimum external annular ring may have 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes, or splay in the annular ring of isolated areas.
Internal Plated-through holes	90° hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.[1]	The minimum internal annular ring **shall** be 25 µm [984 µin].
External Unsupported holes	Not greater than 90° breakout of hole from land when visually assessed.[1] The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	The minimum annular ring **shall** be 150 µm [5,906 µin]. The minimum external annular ring may have a 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes or splay in the annular ring of isolated areas.

Annular Ring requirement drives pad diameter
Drill diameter +10 Mils (up to 100 mils thick) = pad diameter IPC Class 2
Pad diameter +10 Mils = anti-pad diameter

Annular Ring Measurement

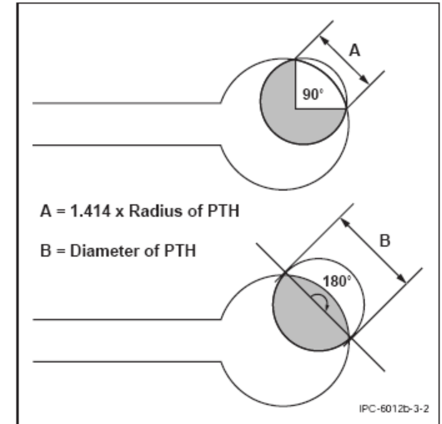
External annular ring is measured from the inside of the plated through hole barrel to the edge of the land pad



Non-Teardrop pad

Internal annular ring is measured from the hole barrel to the edge of the land pad

Teardrop pad to maintain required minimum trace connection when breakout is allowed



IPC 6012C Breakout definition

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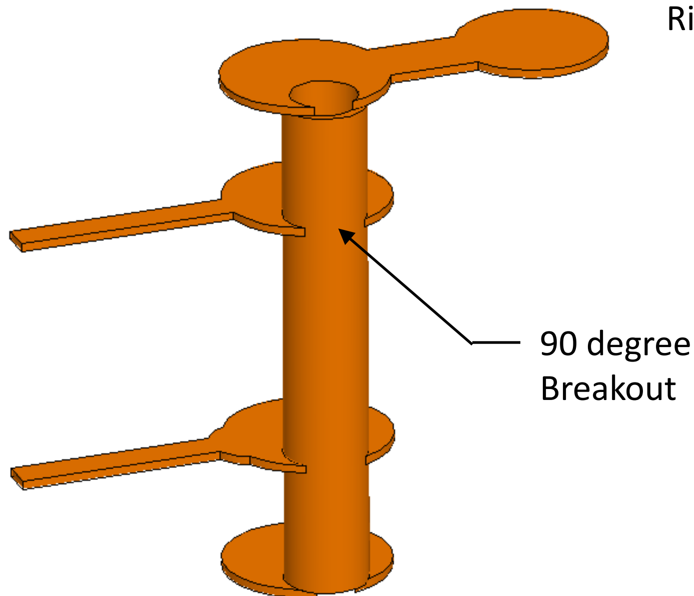
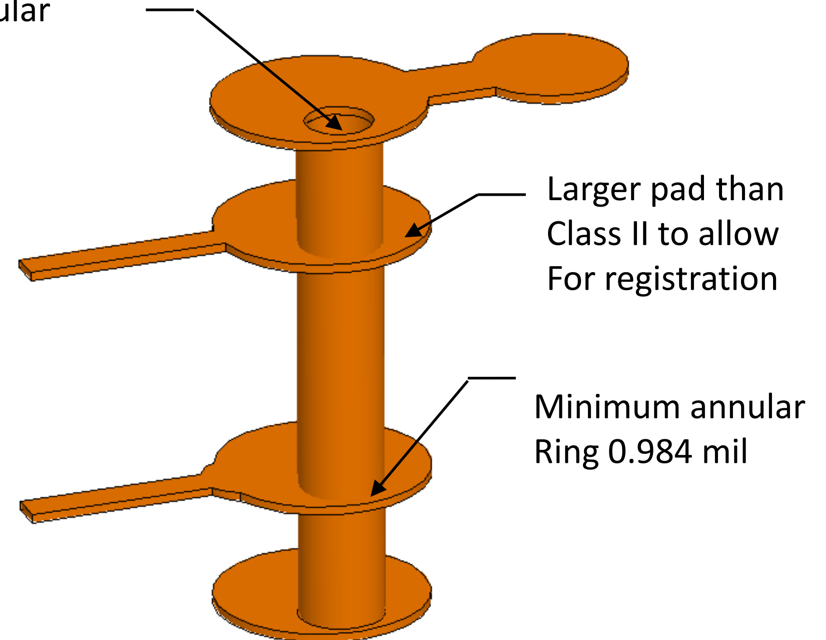
Annular Ring Requirements For IPC Classes II & III

IPC 6012C Class 2

IPC 6012C Class 3

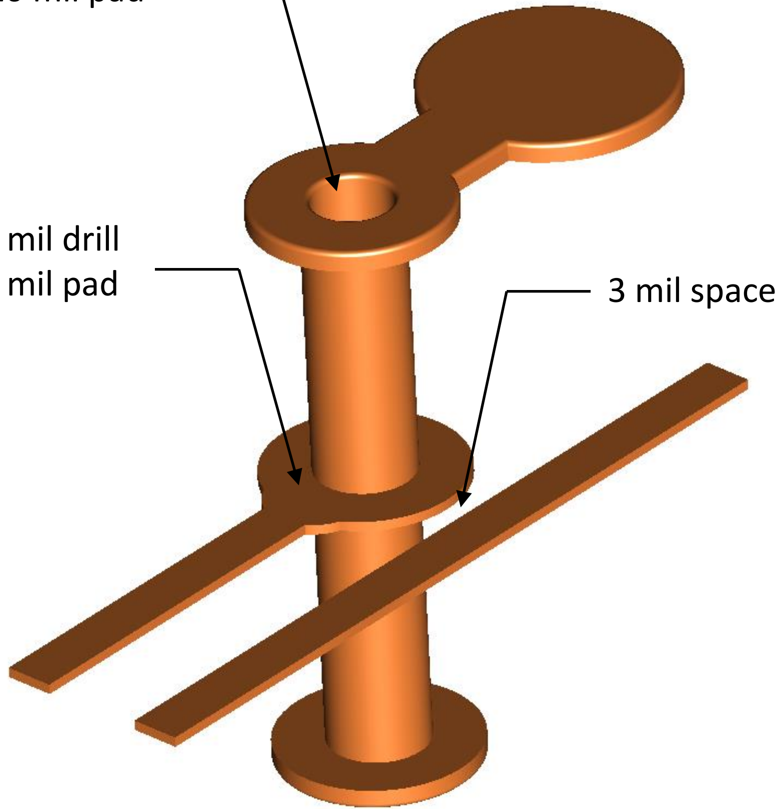


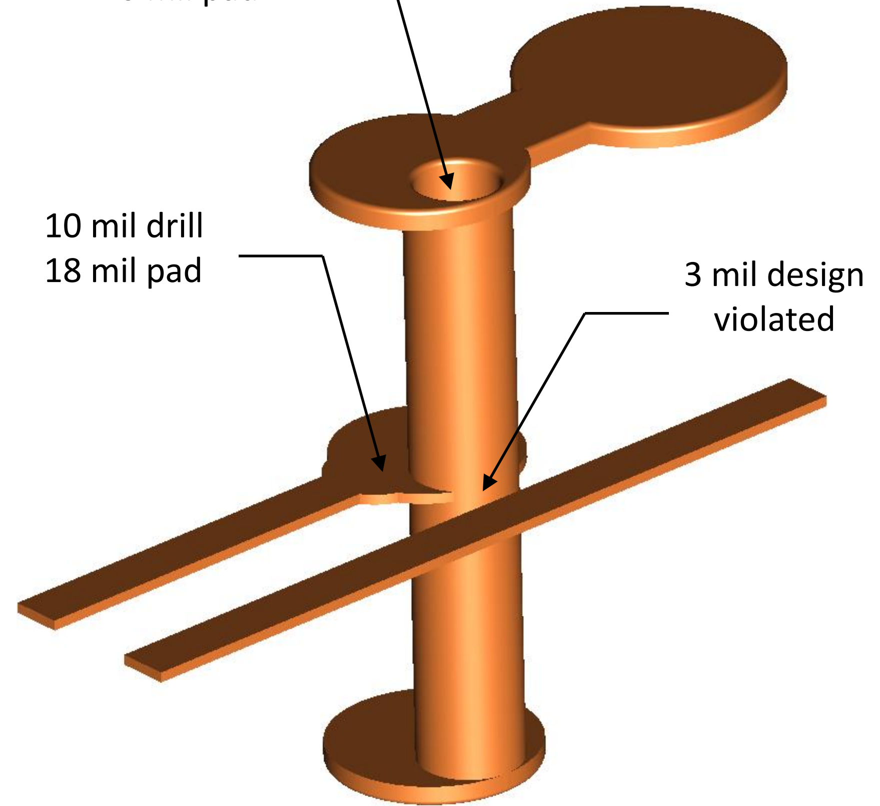


Worst case registration allowed by IPC Class II

Worst case registration allowed by IPC Class III

Minimum Drilled Hole To Copper & Minimum Class II Pad





- Internal pad designed for tangency
- Drilled hole to copper of 8 mils
- 3 mil space maintained

- Internal pad designed minimum with breakout
- Drilled hole to copper of 7 mils
- 3 mil space can be violated

Array Pattern Routing for BGAs

0.65 mm BGA

~~Through-hole Vias~~

Through-Hole Vias

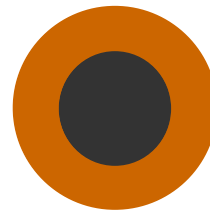
0.0256”

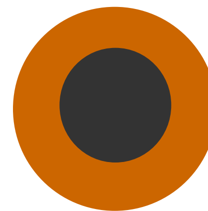
0.016” (400 µm) via pad

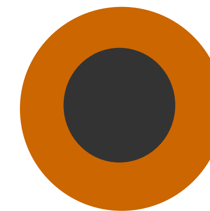
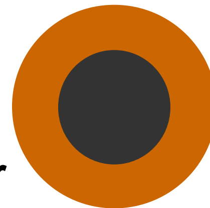
0.008” (200 µm) drill .0096”

0.003” (75 µm) trace

0.0033” (83 µm) space





0.0073” (185 µm) drill-to-copper

Violates hole-to-copper min

Break-out allowed

Requires additional Engineering $$$$$

Internal Layer

Aspect Ratio 7.75:1

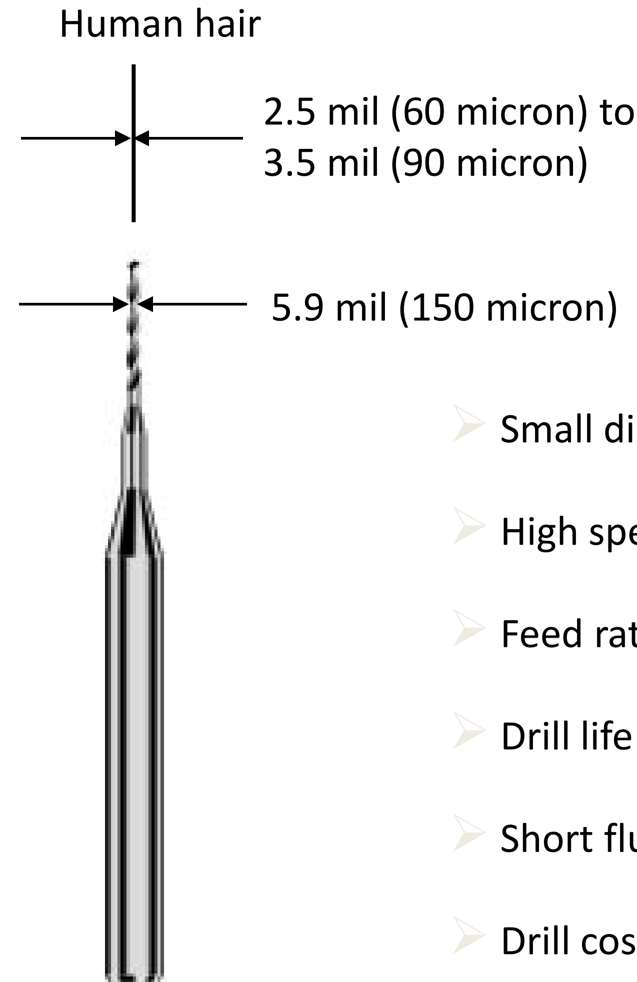
Thickness of 0.028” (0.711 mm) - 0.062” (1.575 mm)

Mechanical Drilling: How small can we go?

← Same process, smaller drills ! →

- Alignment issues
- Drill wander
- Drill life
- Hole quality

Putting Small Diameter Drills Into Perspective



Carbide drill bit

- Small diameters are very fragile
- High speed spindles are required
- Feed rates are about 50% of standard via diameters
- Drill life of 300 to 600 hits depending on material
- Short flute length limits hole depth
- Drill cost is higher
- Limited availability from offshore PCB production

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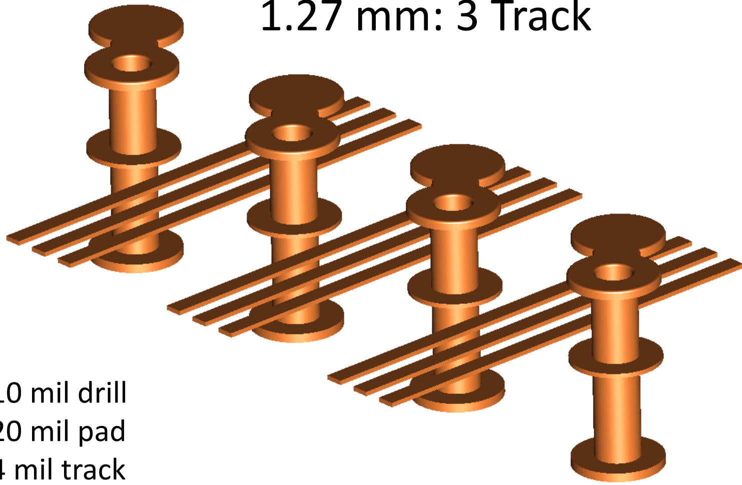
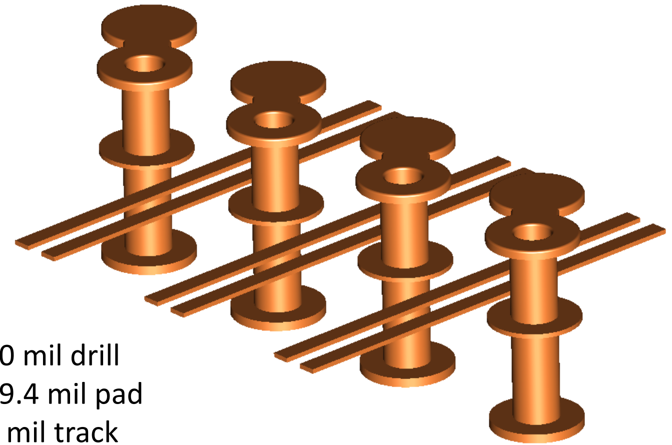
Array Pattern Escape: Through Hole IPC Class 2

1.27 mm: 3 Track



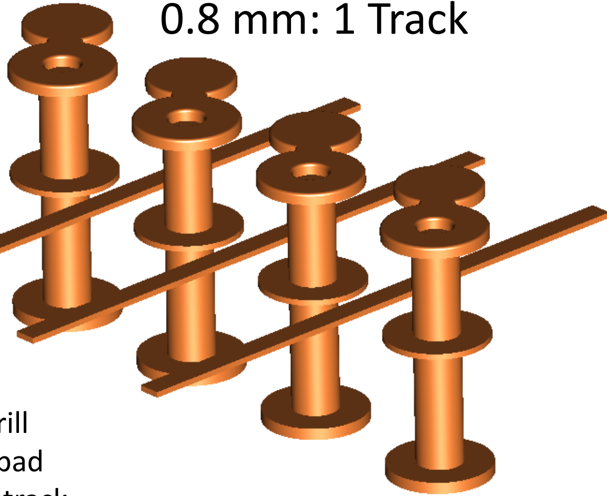
10 mil drill
20 mil pad
4 mil track

1.0 mm: 2 Track



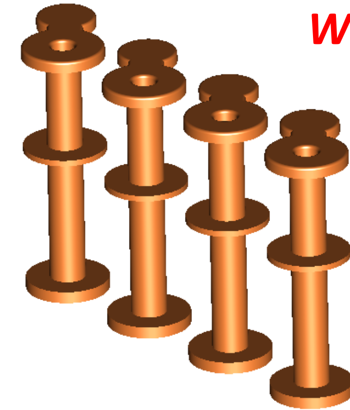
10 mil drill
19.4 mil pad
4 mil track

0.8 mm: 1 Track



8 mil drill
18 mil pad
4.5 mil track

0.5 mm: 0 Track



What now ?

6 mil drill
16 mil pad
No routing

Enabling PCB Equipment

- Laser Drilling
- Laser Direct Imaging
- Reverse Pulse Plating

Laser Drilling Technology Overview

- Hole diameters range from 4 to 8 mils and are typically in the 5 to 6 mil range
- Pad sizes are reduced (via +5 or 6 mil, instead of +10 mil), leaving more space for routing and smaller antipads
- Hole depth is limited by copper plating aspect ratio, typically 0.5: to 0.6:1 however higher aspect ratios can been achieved
- Both YAG and CO_2 lasers are used for PCB drilling. YAG lasers are in the ultra violet spectrum and can drill both copper and dielectric. CO_2 lasers are in the infrared spectrum and can drill dielectric materials
- The combined use of YAG and CO_2 lasers allow lasing of all common PCB materials at optimum speed
- Three step lasing operation provide optimum hole quality i.e. YAG to remove copper, CO_2 to remove dielectric and YAG to clean the copper pad
- It is not practical to laser drill all the way through a board unless it is less than about 10 mils thick

Laser Drilling Technology: The Quest For Speed !

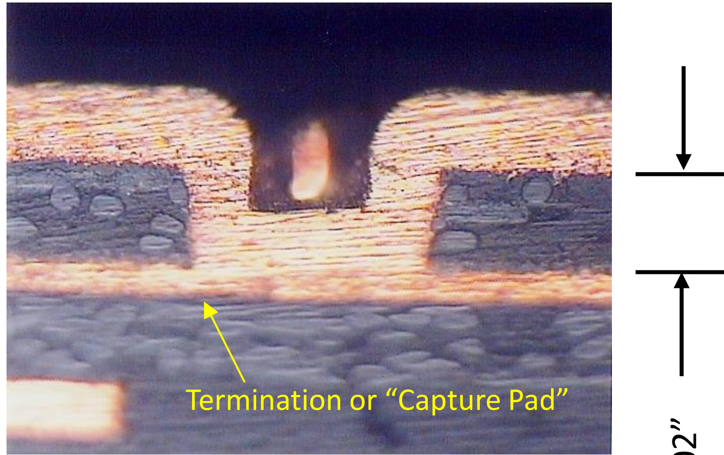
Combination ND:YAG CO_2
Forms holes by removing copper with the ND:YAG laser and the dielectric and re-enforcing material with the CO_2 laser (Approximately 3,500 to 13,000 holes per minute)

$C0_2$ (Infrared)
Capable of drilling most re-enforcing materials and laminate resin systems. Not effective for drilling copper (copper is reflective in the infrared spectrum and must be window etched) Forms holes by pulsing a larger high energy beam (Approximately 17,000 holes per minute)

ND:YAG (Ultra-Violet)
Capable of drilling copper, all re-enforcing materials and all laminate resin systems. 25 to 50 micron beam forms holes by spiraling, or trepanning, the beam (Approximately 600 to 1,400 holes per minute)

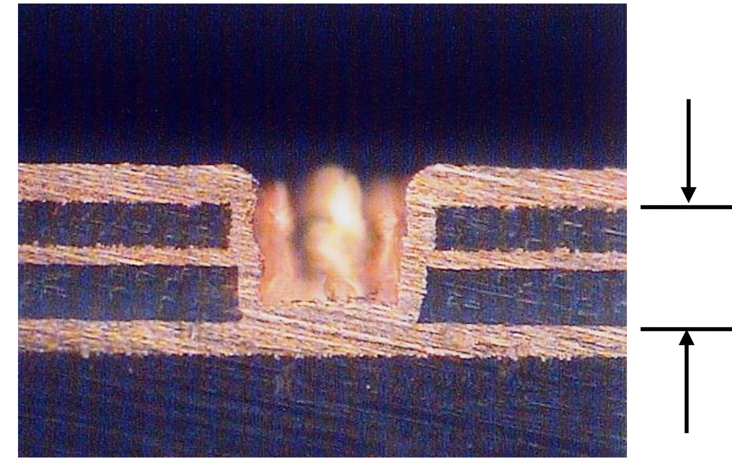
Laser Drilled Hole Geometry

Typical Via Diameter



Laser drilled Microvia
Layer 1 to 2

Maximum Via Diameter



Laser drilled Microvia
Layer 1 to 3

Note:

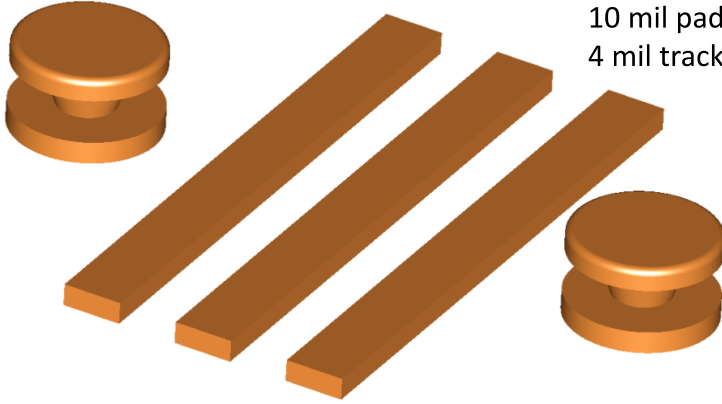
1- Hole depth is limited by plating aspect ratio(depth/diameter)
Typical aspect ratio on laser drilled holes is 0.5:1 to 0.6:1 max

2- Holes greater than 0.005” are generally considered too large to be placed in component pad

Array Pattern Routing: Microvia

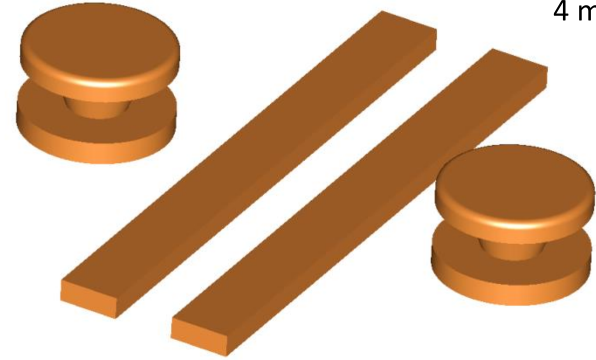
1.0 mm: 3 Track

5 mil Laser
10 mil pad
4 mil track

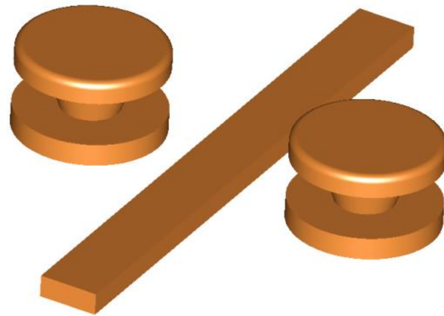


0.8 mm: 2 Track

5 mil Laser
10 mil pad
4 mil track

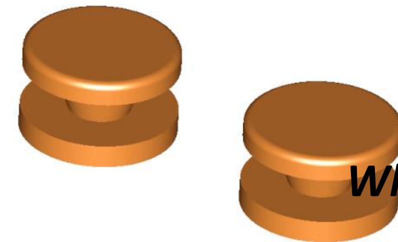


0.5 mm: 1 Track



5 mil Laser
10 mil pad
3 mil track

0.4 mm: 0 Track

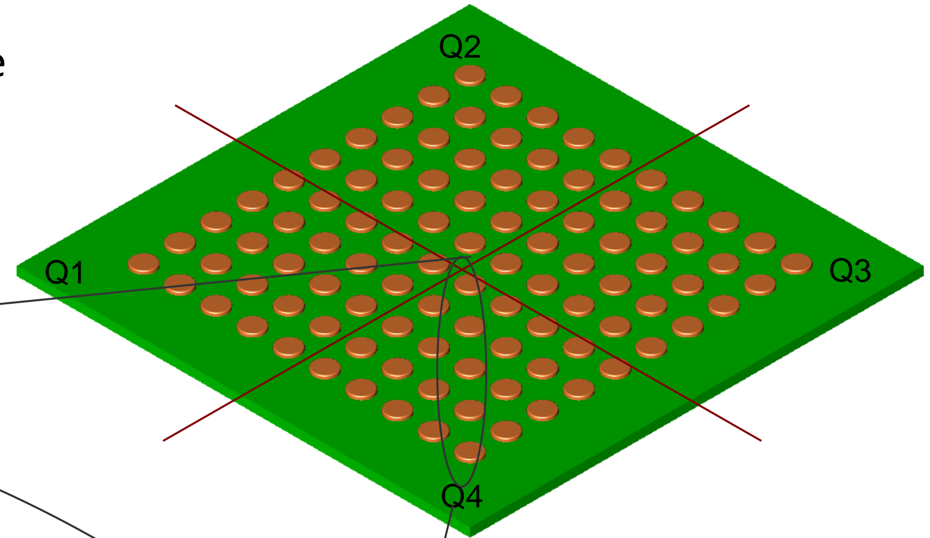


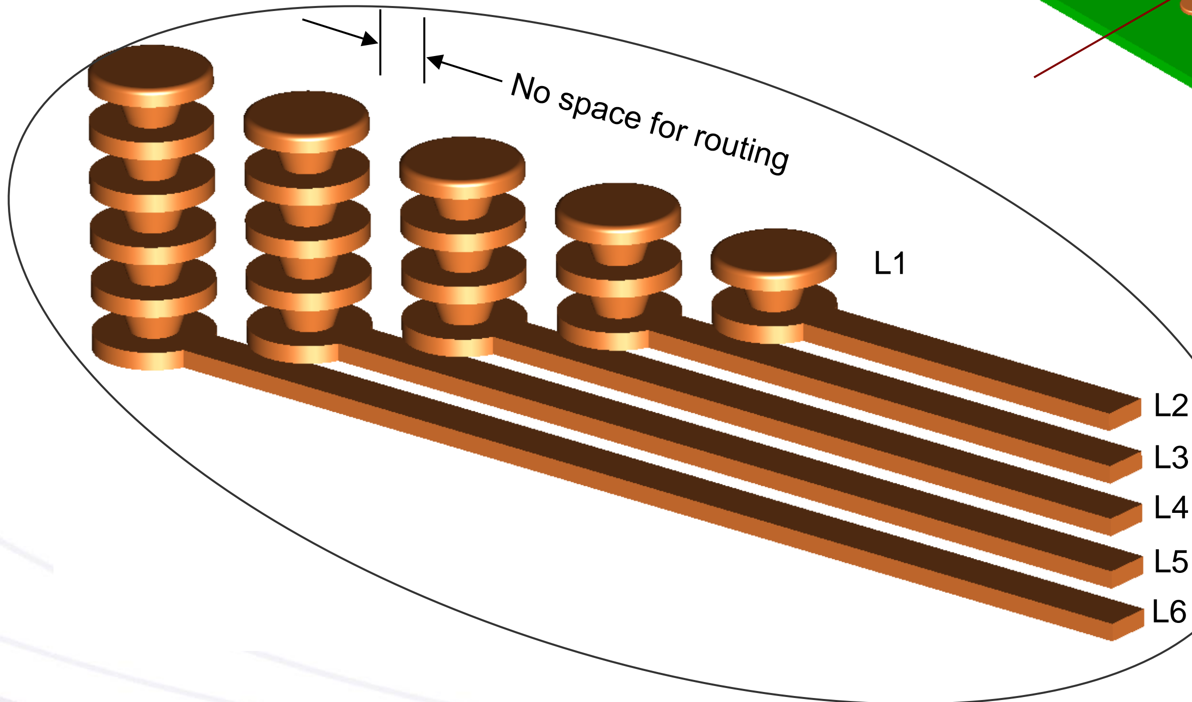
What now ?

5 mil Laser
10 mil pad
No track
Routing is possible with smaller internal pads and sub 3 mil lines reducing yields

Routing By Via Row Reduction

Once routing channels are eliminated by current process limitations, each row of the array pattern will require a unique routing layer. As each row is connected it will open routing for the next.

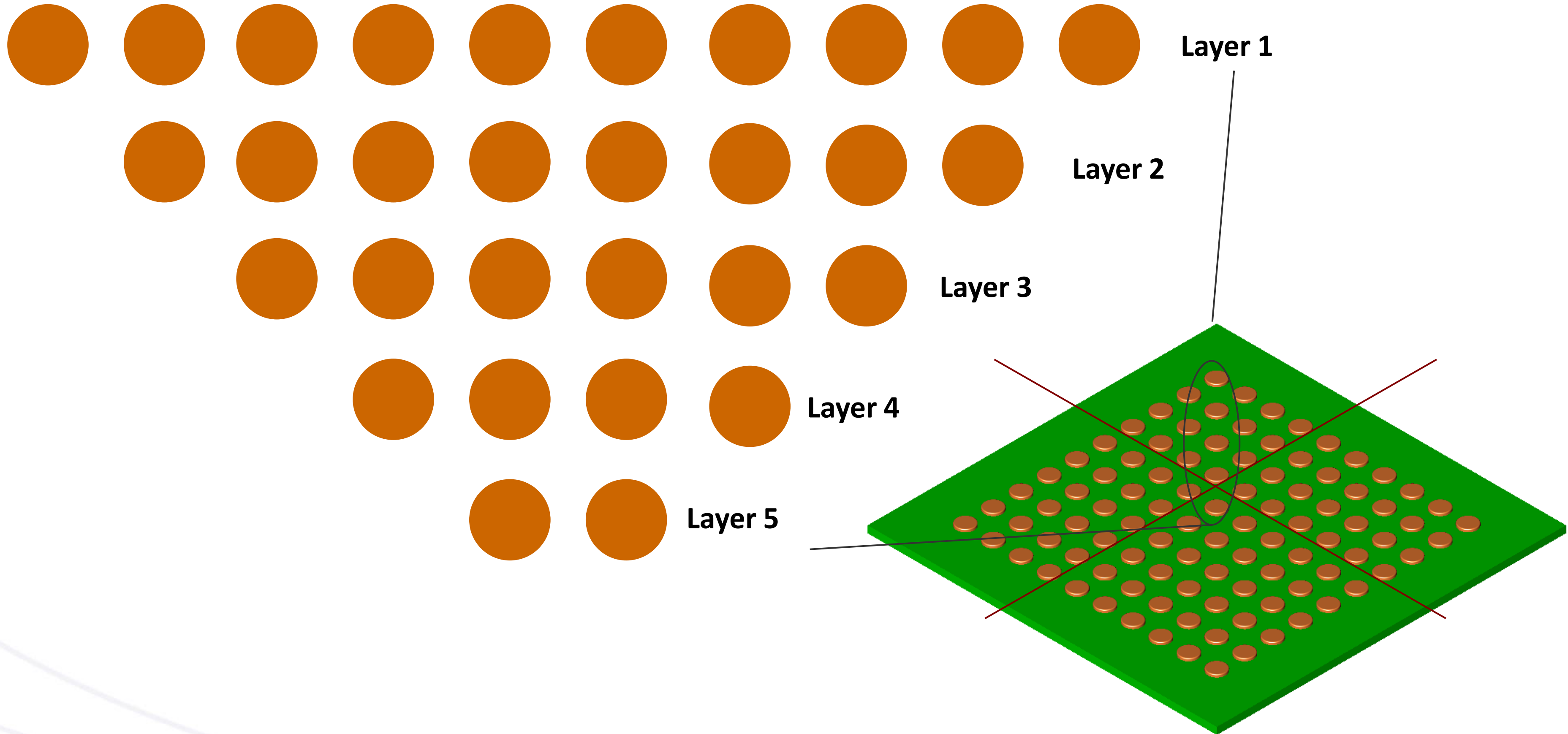




This approach dramatically Increases PCB complexity !

Second Generation Microvia Geometries: Routing by via row reduction

Example of 100 I/O 0.4 mm Pitch Fan out Inverted Pyramid Approach

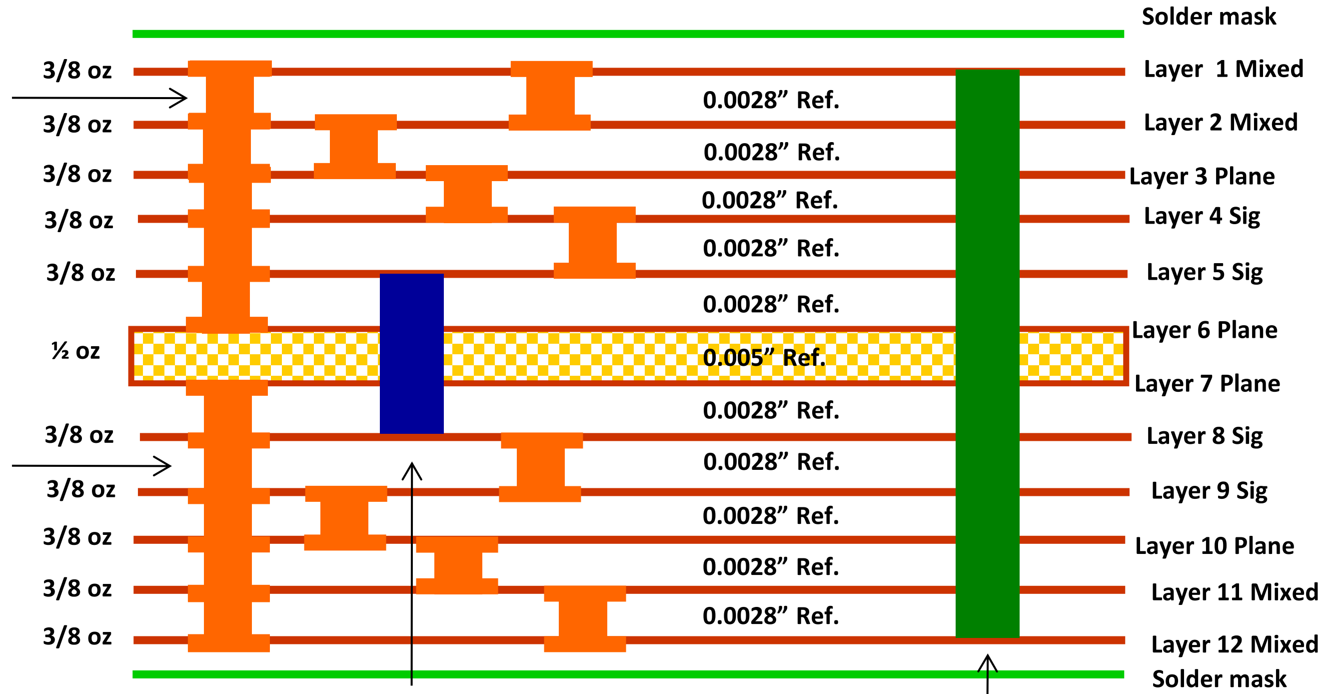


TTM Technologies

Stacked MicroVia (SMV®)

Stacked MicroVias
Layer 1 - 2
Layer 2 - 3
Layer 3 – 4
Layer 4 – 5
Lauer 5 – 6
0.011” pad internal
0.005” laser drill
Solid copper plate

0.4 mm BGA Advanced Construction



Stacked MicroVias
Layer 13 – 12
Layer 12 – 11
Layer 11 – 10
Layer 10 – 9
Layer 9 - 8
0.011” pad internal
0.005” laser drill
Solid copper plate

Layer 5- 8 = through holes
0.016” pad
0.006” drill

Layer 1- 12 = through holes
0.018” pad
0.008” drill

Finish Thickness = 0.054” +/- 0.005”

Material = Isola 370 HR

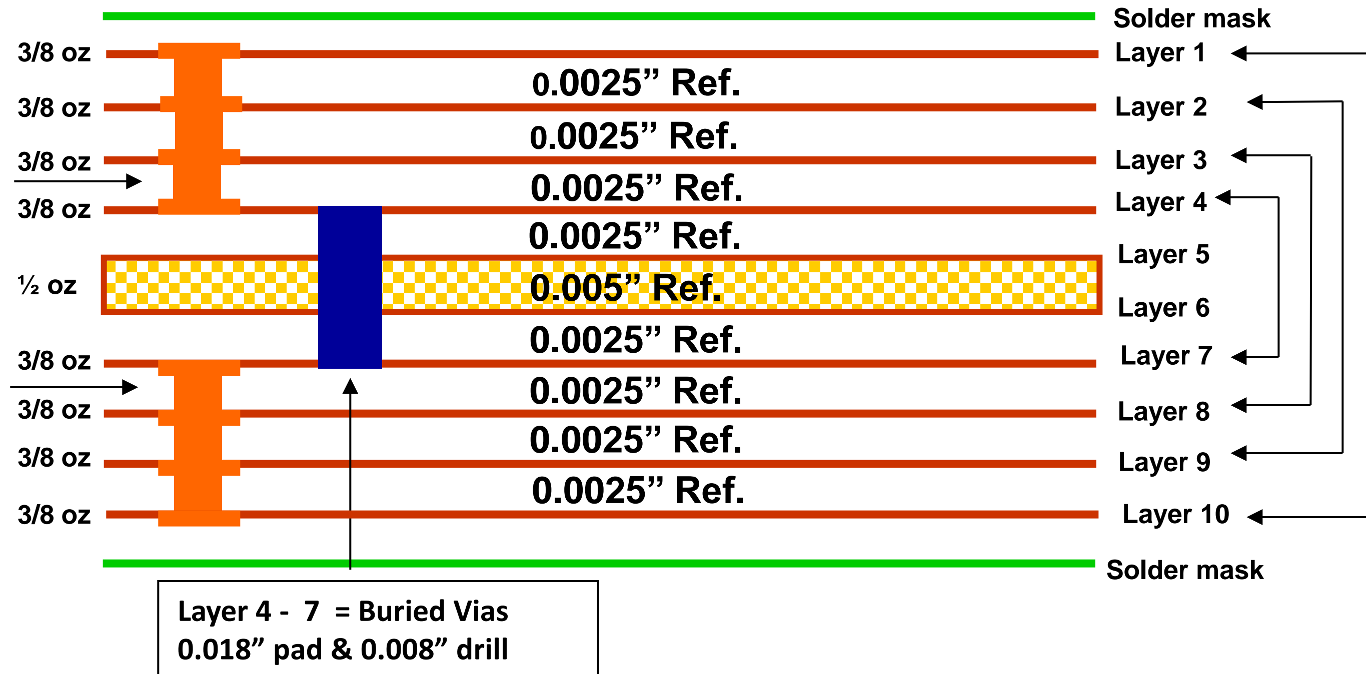
TTM Technologies

Stacked MicroVia (SMV®)

0.4 mm BGA Advanced Construction

4 lams

Stacked MicroVias
Layer 1 – 2, 2 – 3 & 3 - 4
Layers 10 – 9, 9 – 8 & 8 - 7
0.009" external
0.011" pad internal
0.005" laser drill
Solid Copper Plate



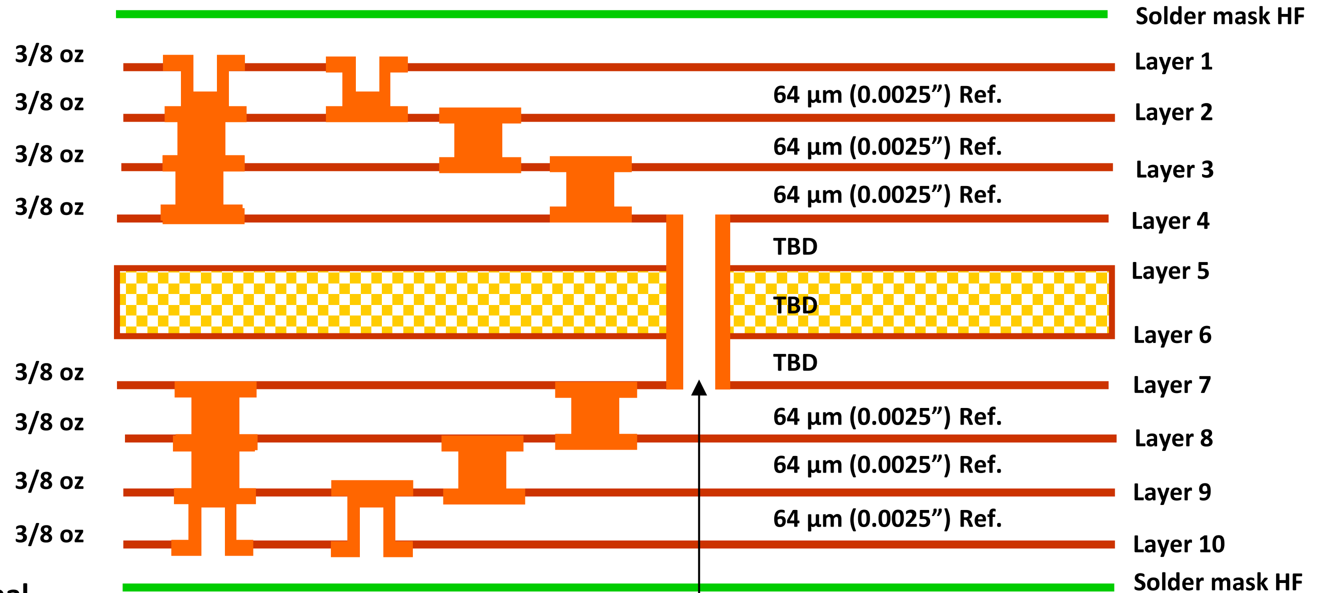
Layer 4 - 7 = Buried Vias
0.018" pad & 0.008" drill

Finish Thickness = 0.0315" +/- 0.004" (0.8 mm)
Material = Isola 370 HR

TTM Technologies

Stacked MicroVia (SMV®)

0.4 mm BGA Advanced Construction



Stacked MicroVias
Layer 1 - 2
Layer 2 – 3
Layer 3 – 4
Layer 10 - 9
Layer 9 – 8
Layer 8 - 7
225 µm (0.009”) pad external
200 µm (0.008”) pad internal
88 µm (0.0035”) trace & space external
65 µm (0.00255”) trace & space internal

Layer 4 – 7 buried via
0.008” drill
0.018” pad

Finish Thickness = To be Defined
Material = 370 HR

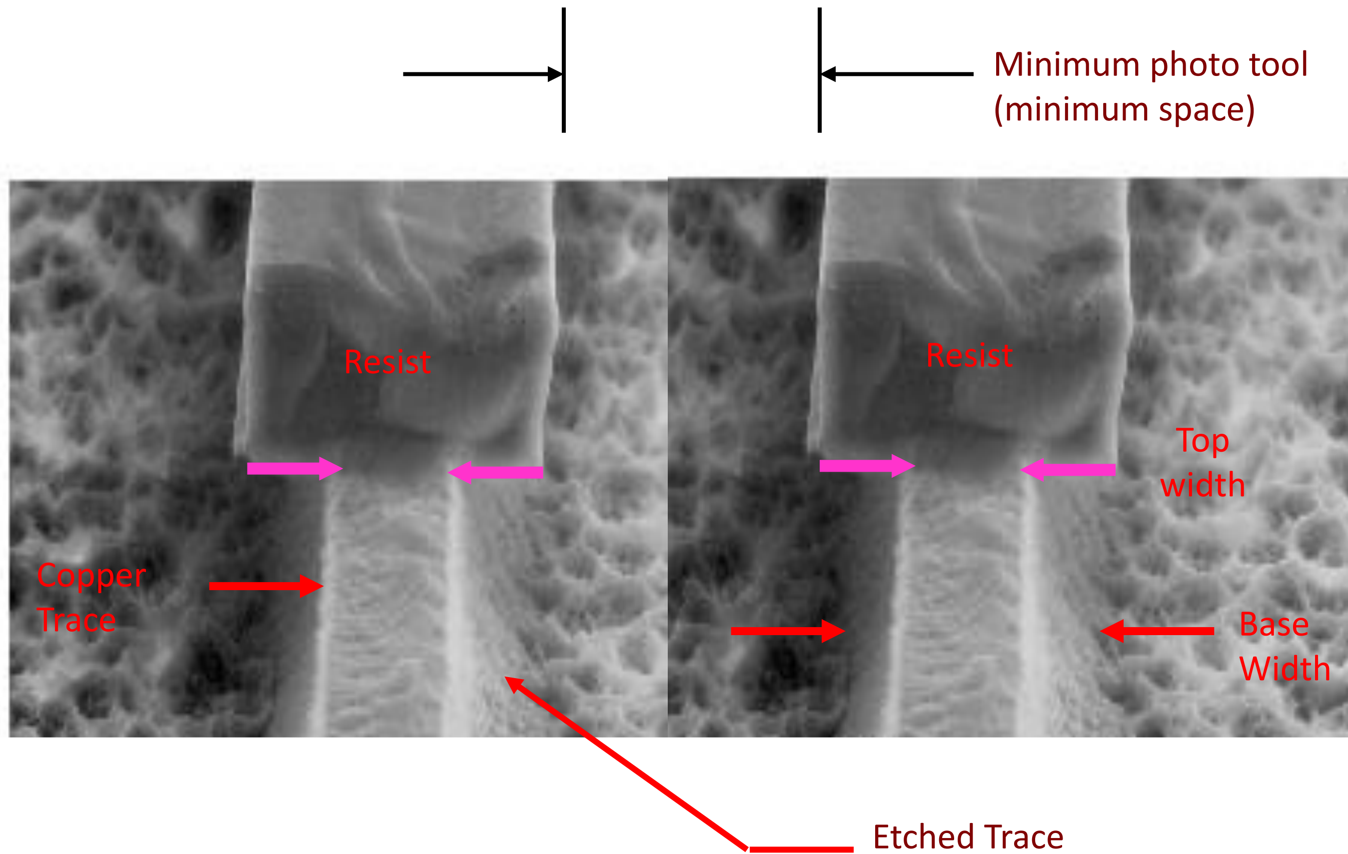
3/8 oz copper plates to 15 µm - 20 µm (0.0006” - 0.0008”)

Why Laser Direct Imaging (LDI) ?

- Current HDI designs require adaptive tooling to meet registration and resolution requirements
- Laser Direct Imaging (LDI) relies on soft tooling eliminating the need for photo tools (Film) saving time and recycling costs of silver base films
- LDI is an off contact imaging method allowing extremely high resolution
- Since LDI is a “soft tooling process” every image can individually registered and scaled for material compensation
- Increased accuracy allows smaller pad diameters while achieving annular ring requirements
- Precision solder mask registration can be achieved with LDI

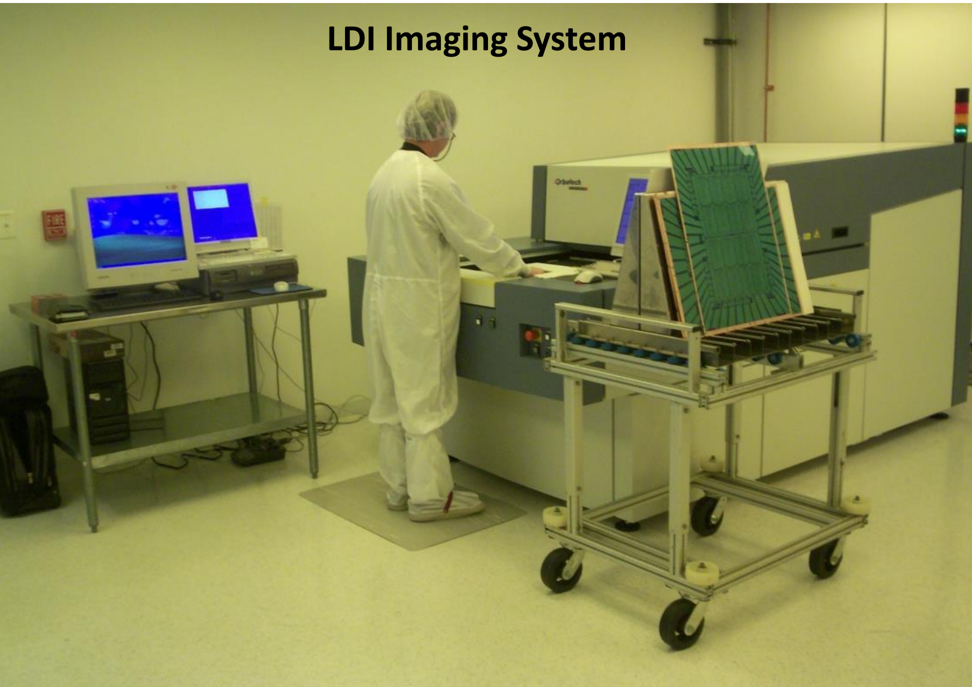
TTM Technologies

Conventional Film-Based Photo Printing Process: The Real Limitation Is Space



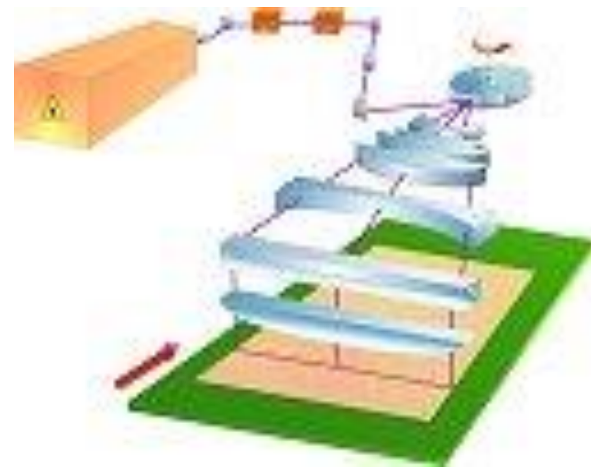
The minimum photo tool opening is limited by the ability to image and fully remove unexposed resist in the narrow gap between traces with high yield

Laser Direct Imaging (LDI)



- Elimination of Photo Tools
- No Film/Artwork Movement
- Quick Turn Made Easy
  - Run product as soon as Engineering releases data to the floor
- Reduction in Defect Count
  - Direct Write = No Film related defects
  - No issues related to loss of vacuum

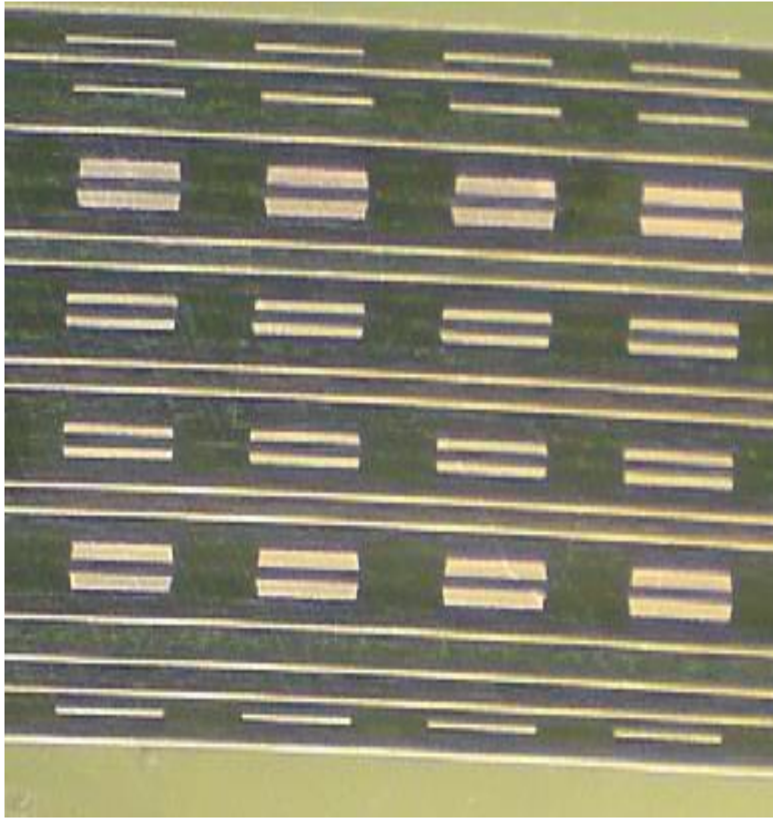
- Improved Resolution, 4000 dpi
- Current process capability (<0.0025”/0.0025”)
- CCD Camera System & Target Fiducials
  - Improved Registration
- Positional Accuracy +/-25µm (.001in)



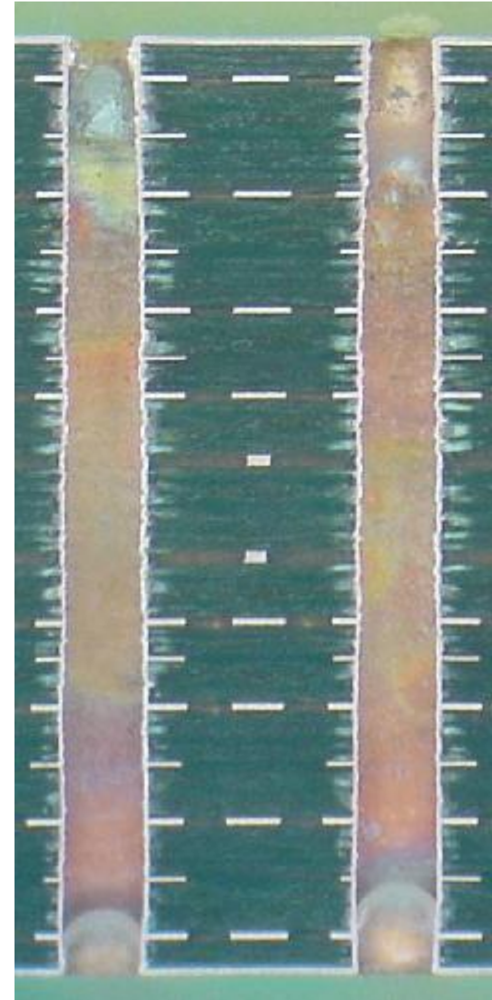
Scanning Optics

Laser Direct Imaging (LDI)

Precise Inner Layer Registration



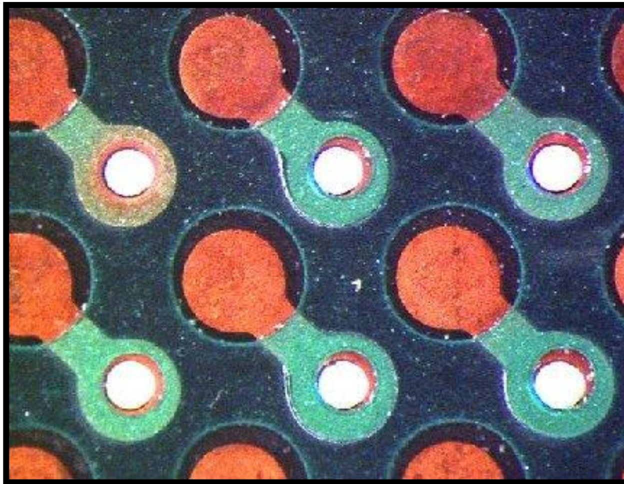
24 Layer PCB Cross-Section



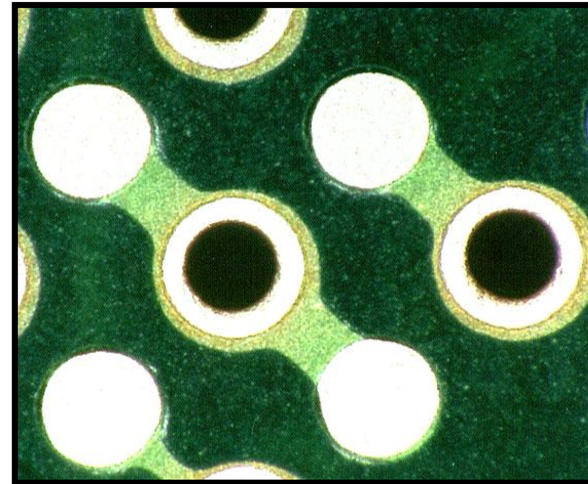
TTM Technologies

Laser Direct Imaging (LDI) Solder Mask (Optional Process)

- Laser Direct Imaged Solder Mask
  - Adaptively tooled
  - Improved Registration +/- 0.001” vs. +/- 0.003”



Standard LPI Solder Mask
+/- 0.003”



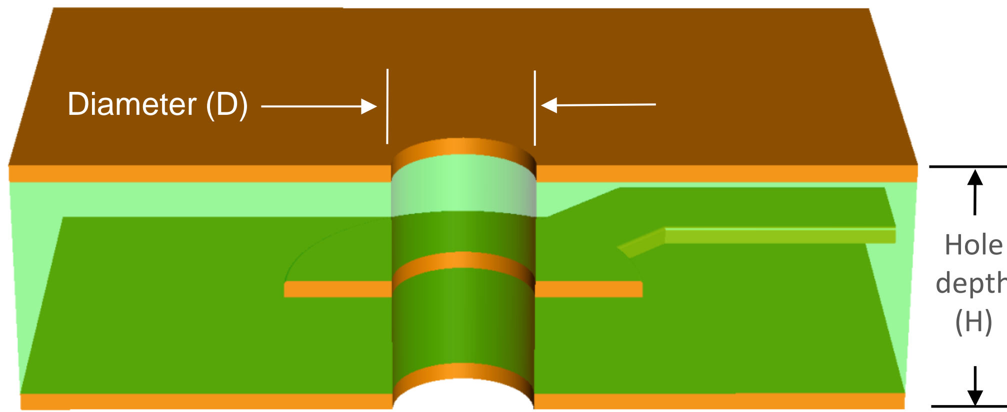
Laser Defined Solder Mask
+/- 0.001”

Consult TTM Engineering For Detailed Information Prior to Design

Advanced Plating Capabilities For HDI

- HDI Circuits often require a variety of different plating operations to meet design requirements
- High quality copper plating is essential for via reliability
- High aspect ratio plated through-holes, microvias, controlled depth holes and solid copper vias present many challenges for electroplating
- Some via structures can require several plating cycles increasing production time and product cost
- Reverse Pulse Plating is the building block to address these challenges

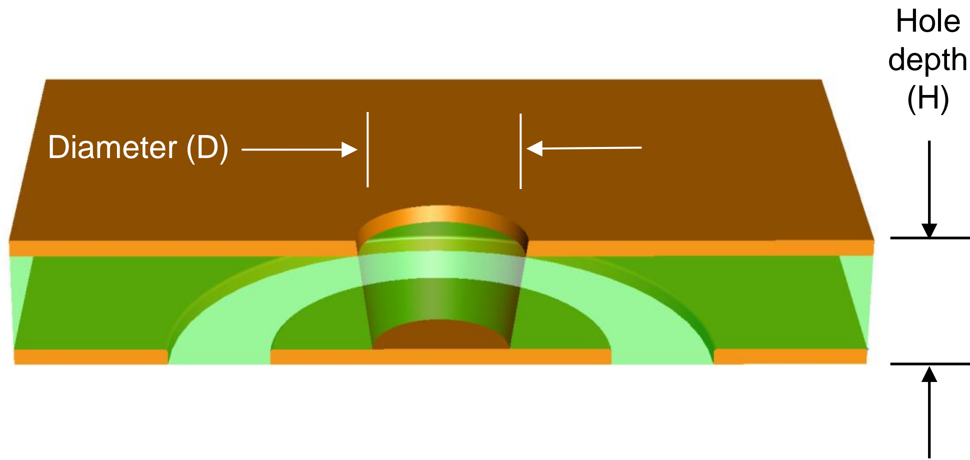
Aspect Ratio: Mechanically Drilled Through Holes



$$\text{Aspect Ratio} = \frac{H}{D}$$

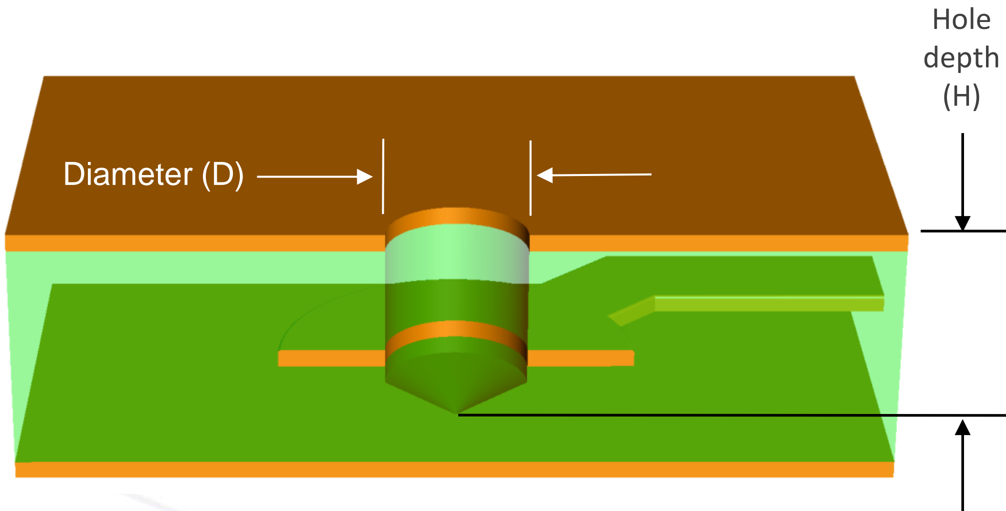
Example 1. Mechanically drilled through hole that will be used to penetrate the entire thickness of the PCB or a through hole that will be used in a mechanically drilled sub-lamination used to form blind or buried via's. In this configuration the depth of the hole is measured from the surface of the external copper layers. In this case if the hole diameter was 0.010" and the depth was 0.093" the Aspect Ratio would be 9.3 to 1

Aspect Ratio: Microvia & Controlled Depth Drilling



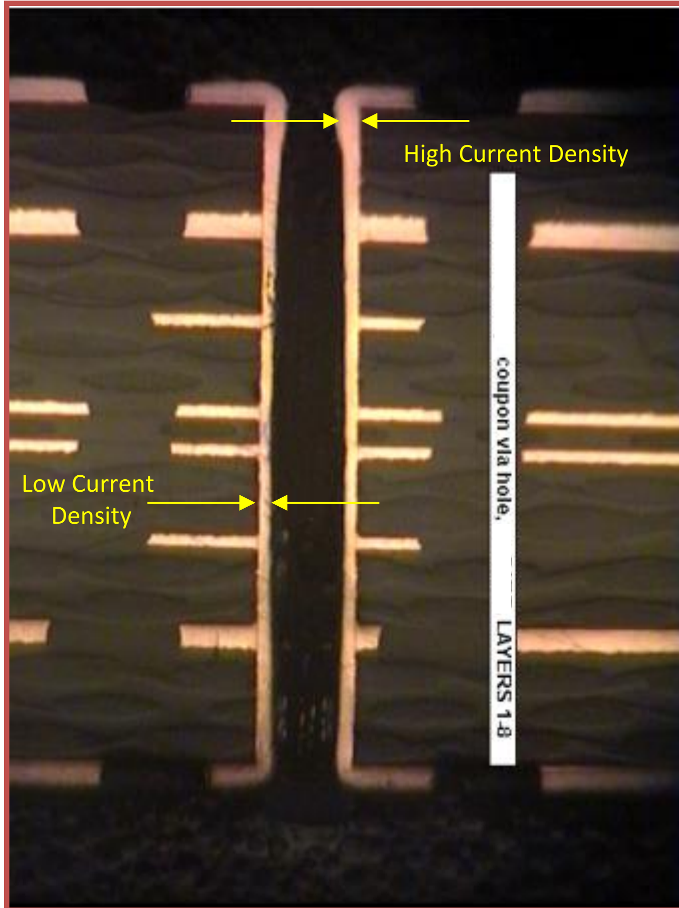
Example 2. Laser drilled microvia's are a controlled depth hole that terminates on a copper layer. As a result the depth of the hole is calculated from the top of the terminating layer to the top of the copper foil layer on the hole entrance. In this case if the hole diameter was 0.006" and the depth was 0.003" the Aspect Ratio would be 0.5 to 1

$$\text{Aspect Ratio} = \frac{H}{D}$$



Example 3. Controlled depth mechanically drilled hole that terminates to an internal copper layer. In this case the mechanically drilled hole must penetrate the internal copper layer in order to make a reliable connection. In order to insure the internal layer penetration, the dielectric thickness and drill depth tolerance must be taken into account and the worst case depth must be used in the calculation. In this case if the hole diameter was 0.025" and the depth was 0.010" the Aspect Ratio would be 0.4 to 1

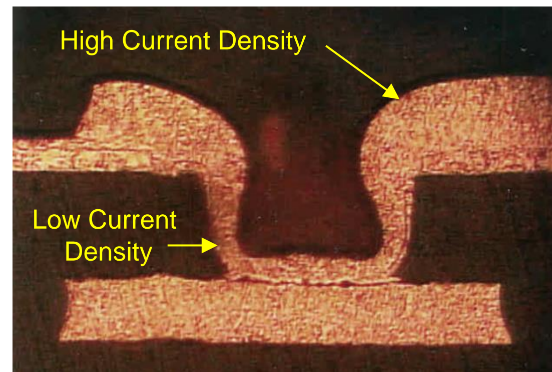
Limitations With Conventional "DC" Copper Electroplating



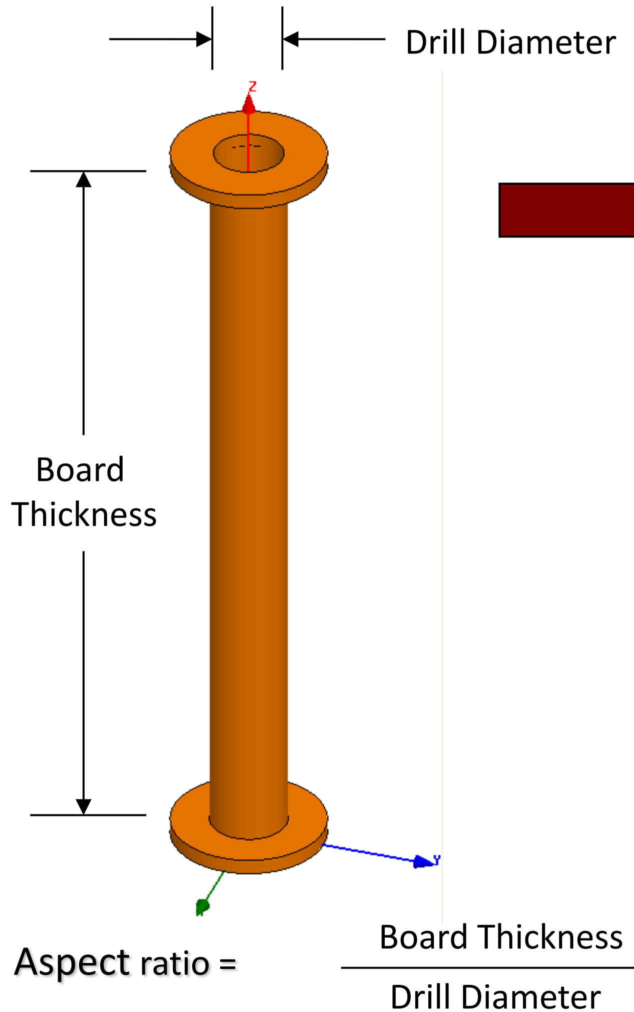
- In conventional DC electroplating, edges of the hole barrel have easy access for copper ions to deposit resulting in higher current density and faster copper deposition

- Regions deep in the hole barrel have a lower current density resulting in a lower deposition rate. The net result on high aspect ratio holes is that copper tends to be thicker at the edge of the hole barrel for a given thickness at the center

- Reducing the overall current density can achieve more uniform plating thickness. However, if the current density is reduced too much the grain structure of the copper can become coarse leading to possible barrel cracking



High Aspect Ratio Copper Pulse Plating



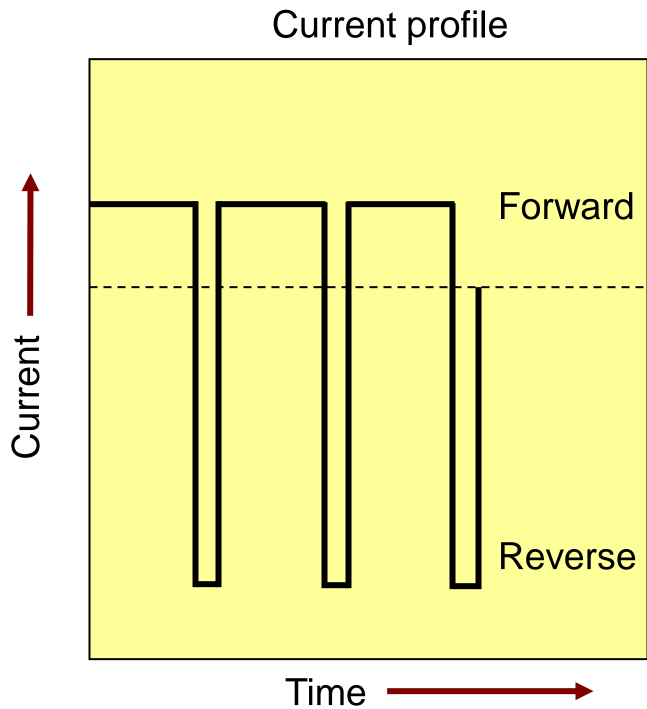
Aspect ratio = $\frac{\text{Board Thickness}}{\text{Drill Diameter}}$

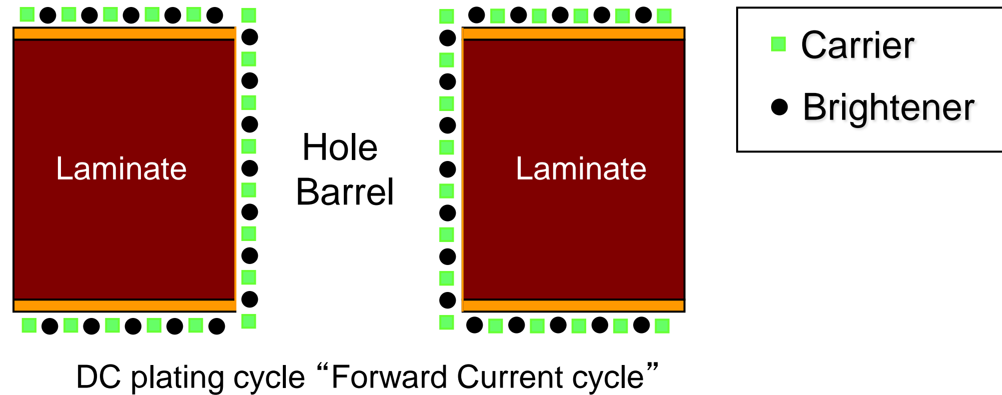
Increasing layer counts and reduced hole diameters are driving Aspect Ratios beyond limits of standard electroplating

Solution: Complex Waveform Pulse Plating

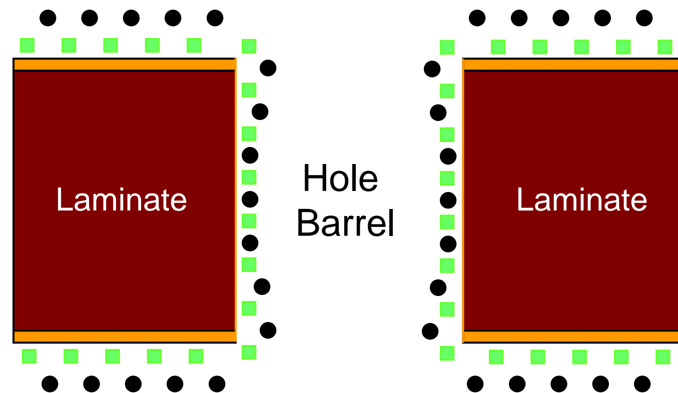
Copper deposition is enhanced by modifying the plating chemistry in the reverse current cycle to reduce copper deposition in high current density areas of the hole barrel, resulting in uniform plating

High Aspect Ratio Reverse Pulse Plating Process





DC plating cycle "Forward Current cycle"

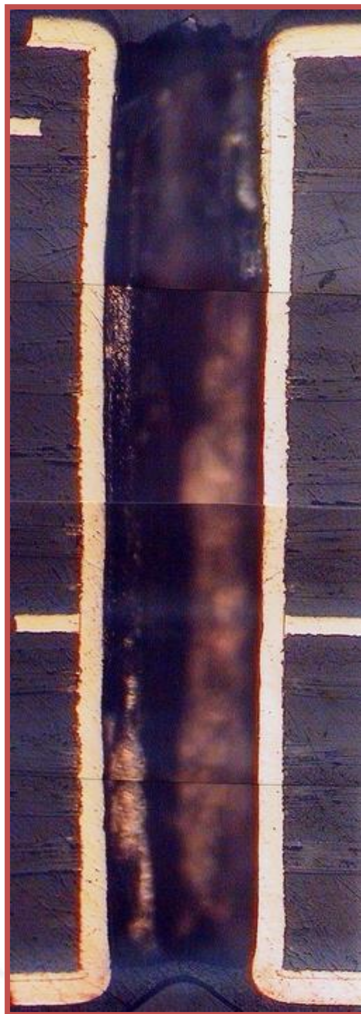


Simplified Overview:

In the forward cycle Cu deposition is greater in high current density areas and lower in the center of the hole barrel. In the reverse cycle the brighteners are de-sorbed from the high current density areas slowing Cu deposition and then slowly return to the surface. This process continues resulting in fast uniform copper deposition.

"Reverse current cycle" brighteners are de-sorbed from the surface in high current density

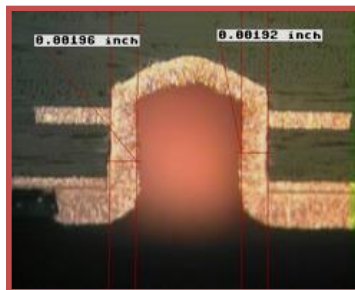
High Aspect Ratio Copper Electroplating Reverse Pulse Plating Process



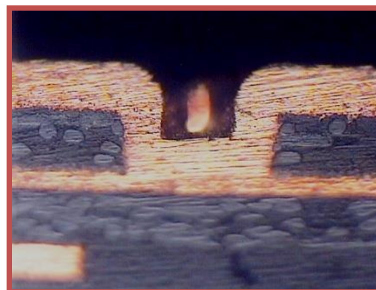
Aspect Ratio = 14:1
Thickness =0.112”
Drill dia. = 0.008”

Aspect Ratio = 16:1
Thickness = 0.216”
Drill dia. = 0.0135”

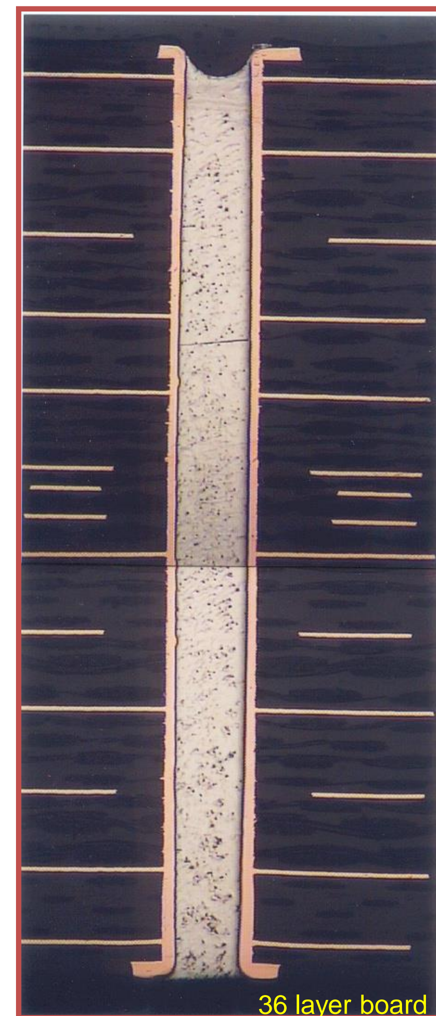
Reverse pulse plating provides uniform copper plating in both high aspect ratio through holes as well as blind laser drilled and mechanical formed blind holes



Controlled depth mechanical drilling



0.005” Laser drilled microvia



TTM Technologies

High Aspect Ratio Copper Electroplating Reverse Pulse Plating Process

Reverse Pulse Plating Capabilities

Description	Aspect ratio	Advanced	Via/Hole Diameter Emerging[1]	Dielectric/ Board Thickness
Microvia	0.6:1	1:1[2]	100 µm (0.004")	100 µm (0.004")
PTH	11:1	14:1	200 µm (0.008")	2.8 mm (0.112")
PTH	14:1	16:1	>337.5 µm >(0.0135")	5.4 mm (0.216")

Reverse Pulse Plating Line

Notes:

1- Always consult engineering with any application where the emerging capabilities are required
2- Requires special process and may not work on all applications
3- Extended flute length drills required, Typical dielectric thickness limit 1.57 mm (0.062")

TTM Technologies

Achieving Higher Densities Using Advanced Via Structures

Engineering Considerations For Via Structures

Standard through hole technology:
Channel density limited by via density, geometry and pitch

Mechanical Solution

Laser Solution

Once you leave through-hole designs, the goal is to find the via combination that maximizes routing channel density at the lowest cost

Controlled Depth Drill:
Still geometry limited
Limited Z axis connectivity

Blind & Buried vias:
Channel density enhanced
Still geometry limited
Limited Z axis connectivity

Microvias:
Channel density enhanced through smaller geometry
Limited Z axis connectivity

Stacked Microvia:
Channel density enhanced through smaller geometry
Unlimited Z axis connectivity

Via Structures: Mechanical Controlled Depth Drill

Controlled Depth Mechanically Drilled Hole

Drilled Through Hole

Prepreg

Core

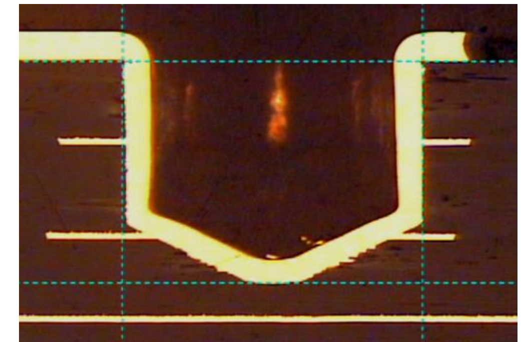
Prepreg

Core

Prepreg

Core

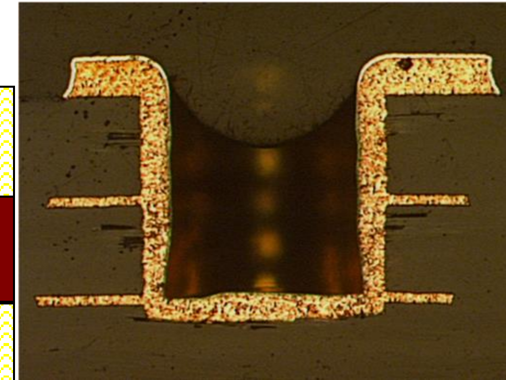
Prepreg



- Increased channel density on layers below the controlled depth drill
- Standard PTH geometry apply, Depth limited by aspect ratio
- No sequential lamination required

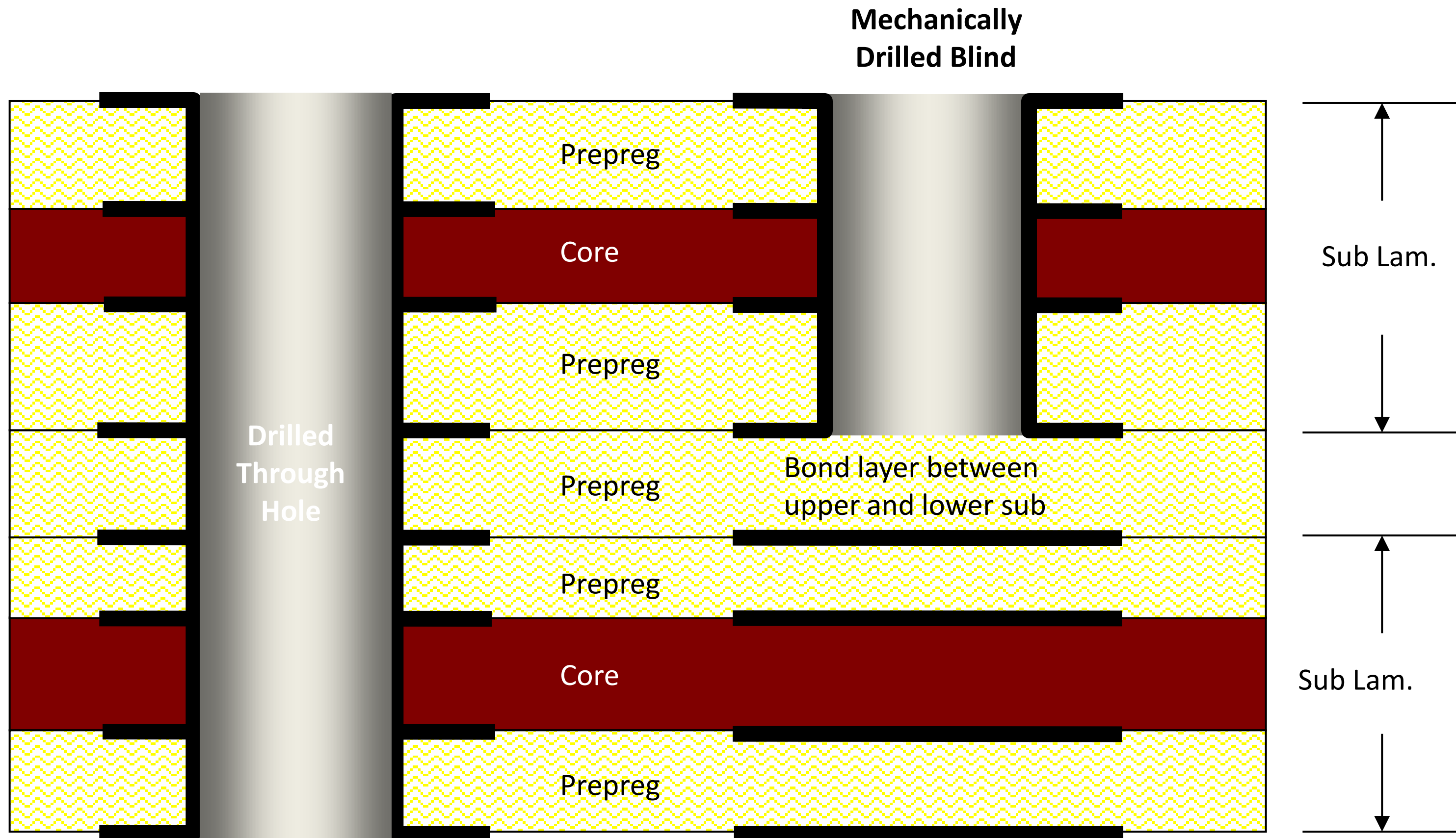
Via Structures: Laser Modified Controlled Depth Drill

Via hole is first mechanically drilled then with a laser the remaining dielectric is removed clearing a path to the copper layer



- Increased channel density on layers below the controlled depth drill
- Allows a connection with no stub
- Standard PTH geometry apply, Depth limited by aspect ratio
- No sequential lamination required

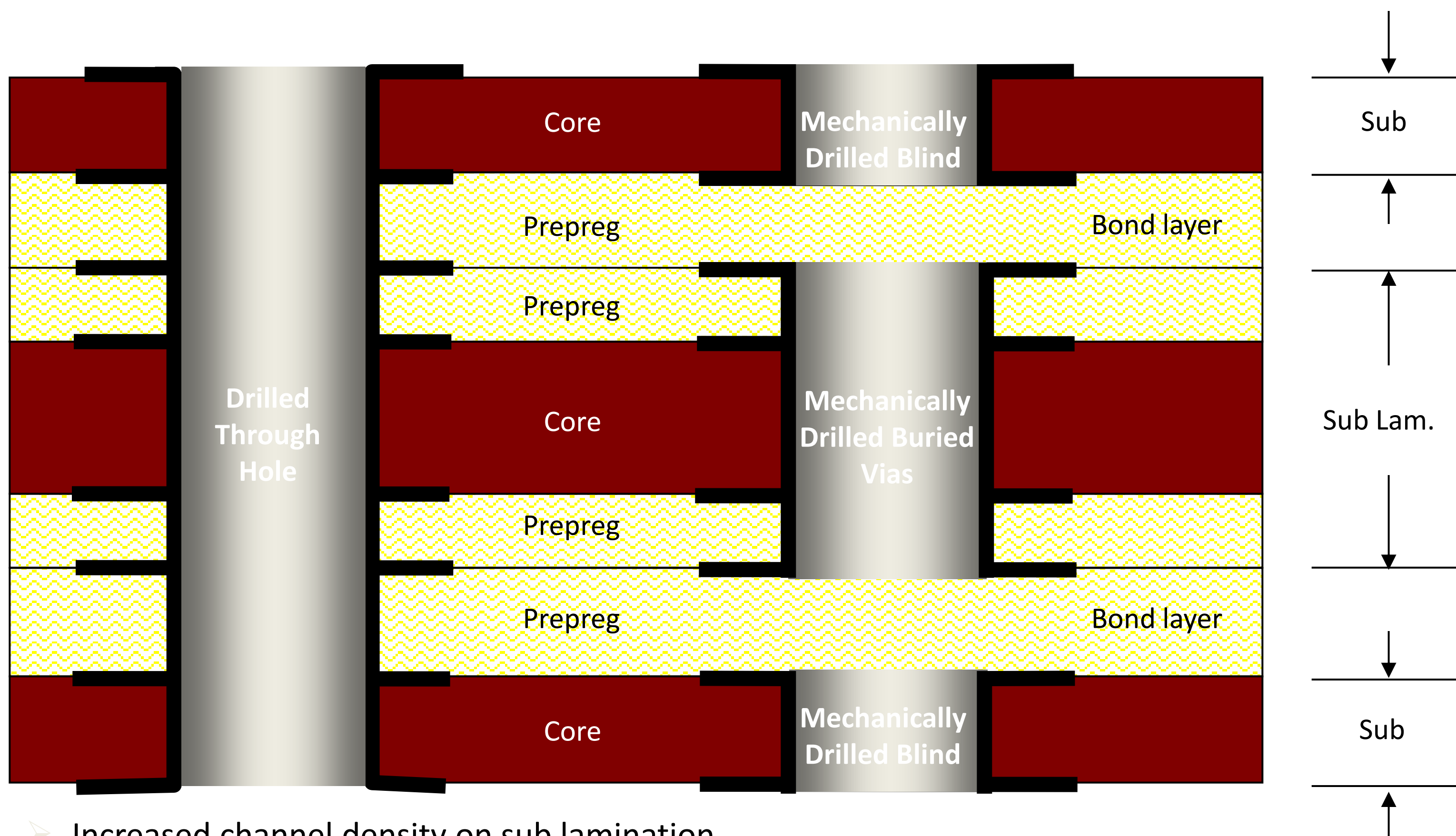
Via Structures: Blind Via



- Increased channel density on lower sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles

TTM Technologies

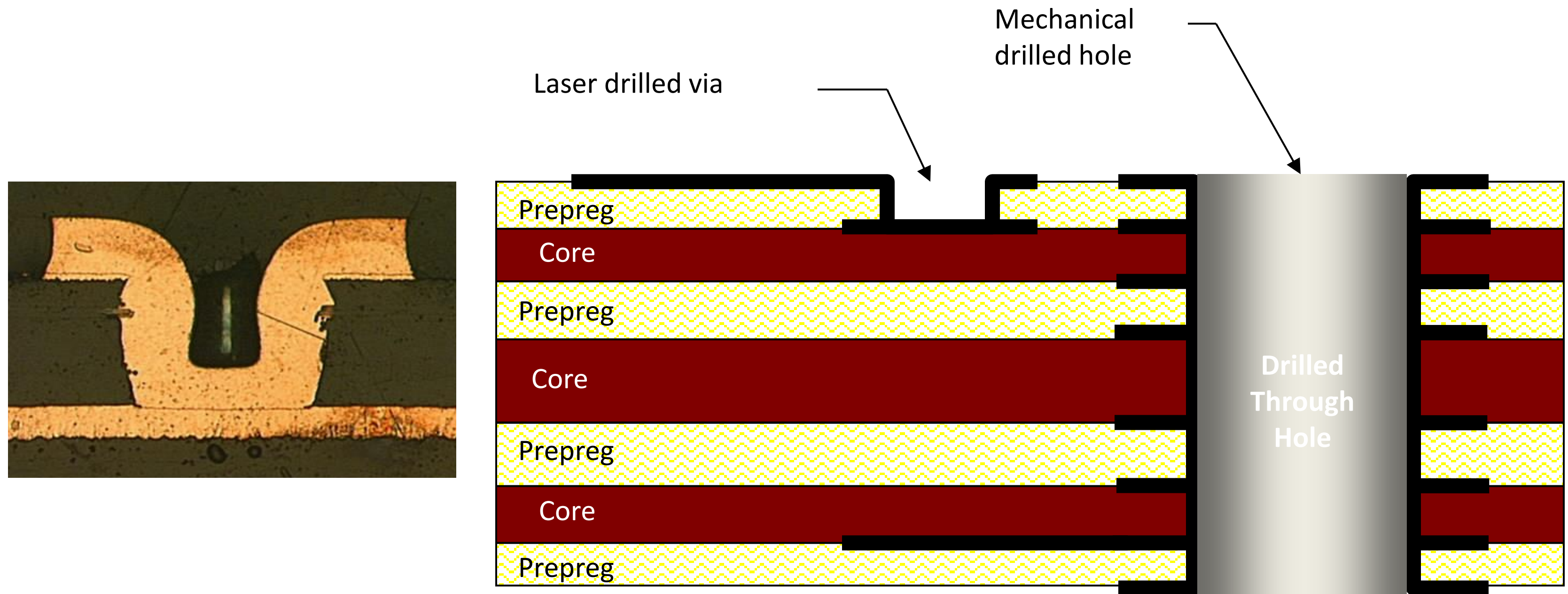
Via Structures: Mechanically Drilled Blind and Buried



- Increased channel density on sub lamination
- Standard PTH geometry apply, reduced aspect ratio on sub drill
- Anti-pad diameter must account for tolerance buildup in multiple laminating cycles
- No Z axis connectivity between adjacent sub-laminations

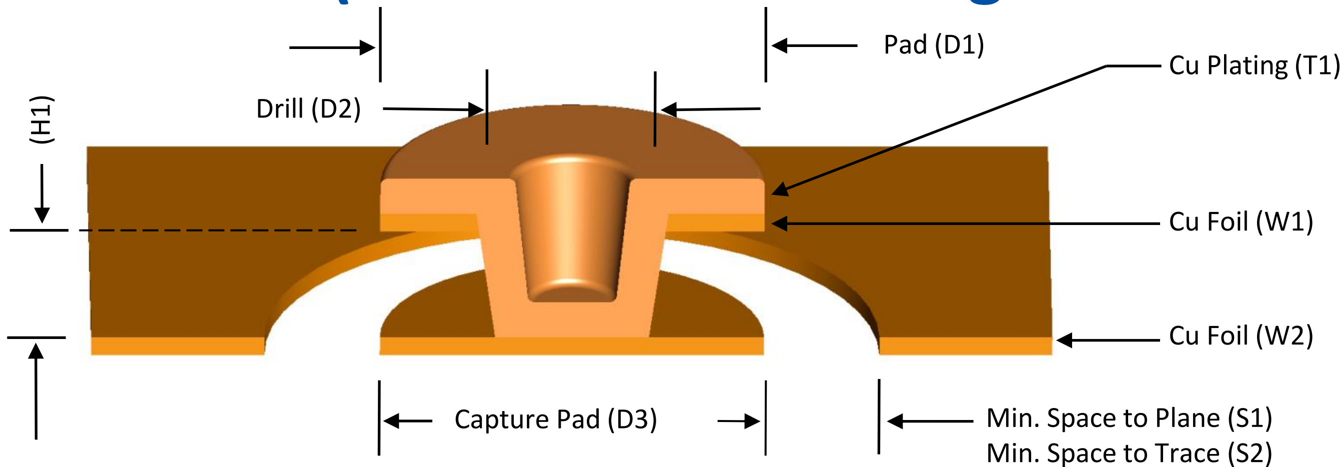
TTM Technologies

Via Structure: Laser Microvia



- Increased channel density on layer 1 and 2 from reduced geometry
- Increased channel density on layers n-1 to n resulting from a blind hole
- Standard PTH geometry apply to mechanical drilled holes
- Dielectric thickness layer 1:2 limited by plating aspect ratio (0.5:1 to 0.6:1)

First Generation Microvia Geometries: (Microvia terminating on a foil layer)



Microvia Feature Variables		Copper Foil Weight			
		1/4 oz	3/8 oz	1/2 oz	1.0 oz
Layer 1 Copper Foil W1 [2]					
Minimum Pad Diameter [1]	D1	0.008"	0.008"	0.010"	N/A
Pad Thickness: W1 + T1		0.0014"	0.0016"	0.0018"	0.0024"
Layer 2 Copper Foil W2 [2]					
Minimum Space to Plane	S1	N/A	0.0035"	0.004"	0.005"
Minimum Space to Trace [4]	S2	N/A	0.003"	0.0035"	0.004"
Minimum Capture Pad Dia. [1,5]	D3	N/A	0.008"	0.010"	0.010"
Foil Thickness	W2	N/A	0.00045"	0.0006"	0.0012"
		Minimum	Maximum		
Laser Drill Diameter [3]	D2	0.004"	0.006"		
Dielectric Thickness	H1	0.0025"	0.003"		
Cu Plating Thickness	T1	0.0012"			

Notes:

1- Recommended minimum pad diameters are drill diameter + 0.006"

2- 3/8 oz and 1/2 oz Cu foil weight are recommended (design permitting)

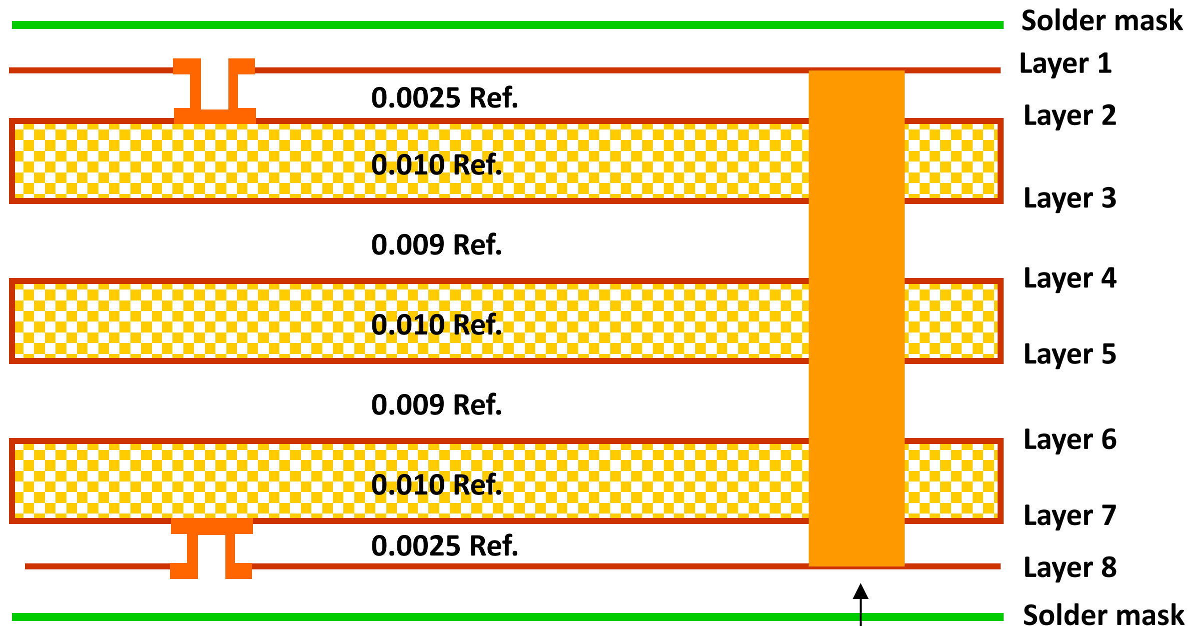
3- Larger hole diameter can be achieved with an increase in lasing and plating time

4- Minimum pad to trace assumes that the trace will pass the pad tangentially

5- 3/8 oz copper foil is not recommended for laser capture pad layers (non-Plated)

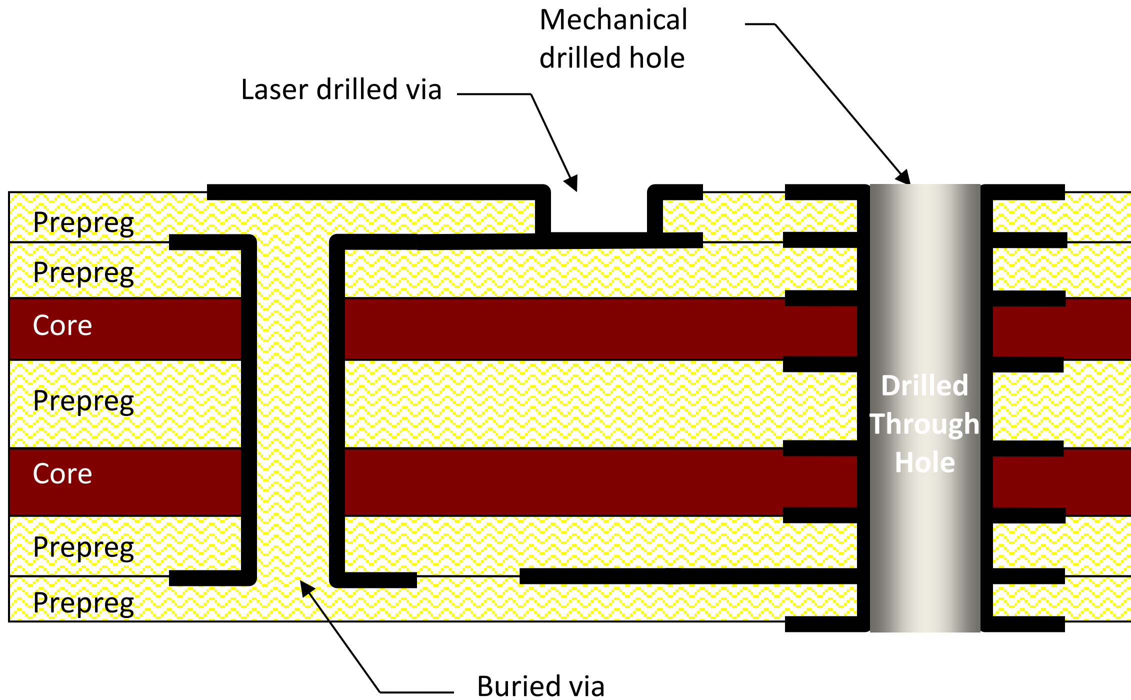
First Generation Microvia Geometries: (Microvia terminating on a foil layer)

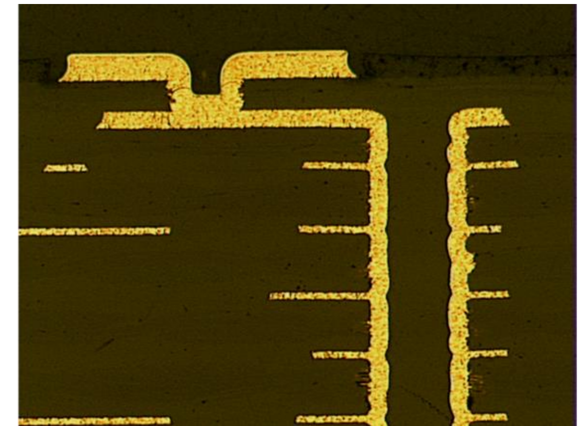
Lowest cost due to one lamination cycle



Finish Thickness = 0.062 +/- 0.006
Material = High Temp FR4

Via Structure: Laser Microvia & Buried Mechanical Sub





- Increased channel density on layer 1 and 2 from reduced geometry
- Increased channel density on layers n-1 to n resulting from a blind hole
- Standard PTH geometry apply to mechanical drilled holes
- Dielectric thickness layer 1:2 limited by plating aspect ratio (0.5:1 to 0.6:1)

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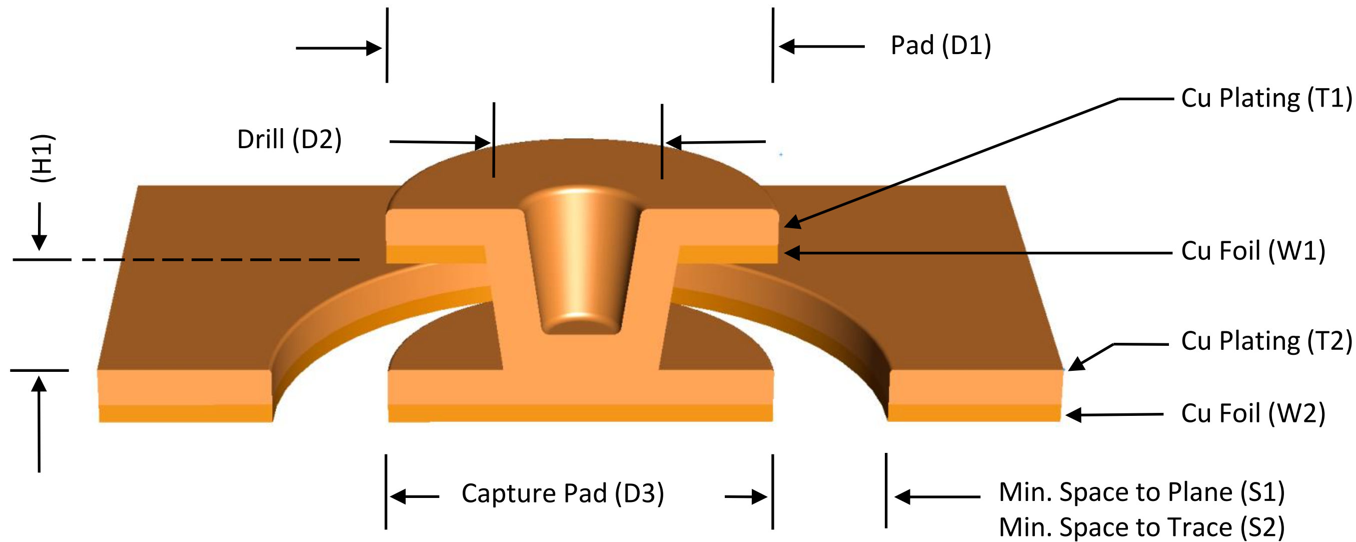
First Generation Microvia Geometries: (Microvia terminating on a plated layer)



Microvia Feature Variables		**Copper Foil Weight**			
		1/4 oz	3/8 oz	1/2 oz	1.0 oz
Layer 1 Copper Foil W1 [2]					
Minimum Pad Diameter [1]	D1	0.008"	0.008"	0.010"	N/A
Pad Thickness: W1 + T1		0.0014"	0.0016"	0.0018"	N/A
Layer 2 Copper Foil W2 [2]					
Minimum Space to Plane [4]	S1	0.005"	0.005"	0.006"	0.008"
Minimum Space to Trace [4, 5]	S2	0.003"	0.003"	0.0035"	0.004"
Minimum Capture Pad Dia. [1]	D3	0.008"	0.008"	0.010"	0.010"
Plated Layer Thickness W2 +T2		0.0013"	0.0014	0.0016	0.0022"
		Minimum	Maximum		
Laser Drill Diameter [3]	D2	0.004"	0.006"		
Dielectric Thickness	H1	0.0025"	0.003"		
Cu Plating Thickness	T1	0.0012"			
Copper Plating Thickness	T2	0.001"			

Notes:

1- Recommended minimum pad diameters are drill diameter + 0.006”

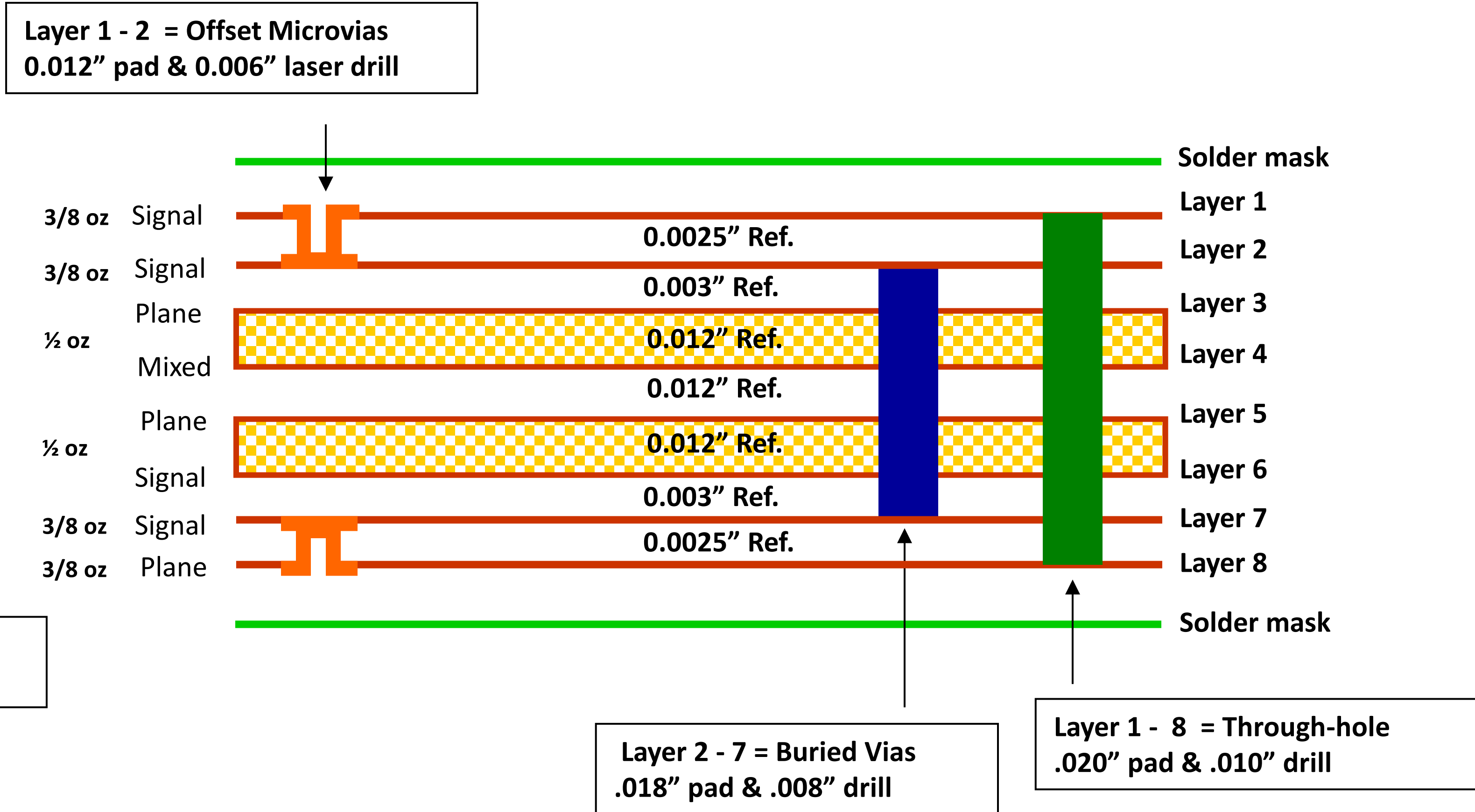
2- 3/8 oz and 1/2 oz Cu foil weight are recommended design permitting

3- Larger hole diameter can be achieved with an increase in lasing and plating time

4- Non-standard increased plating thickness (Wrap plating etc..) will increase minimum space

5- Minimum pad to trace assumes that the trace will pass the pad tangentially

First Generation Microvia Geometries:
("Staircase" Structure)



Finish Thickness = 0.062" +/- 0.006"
Material = High temp FR4

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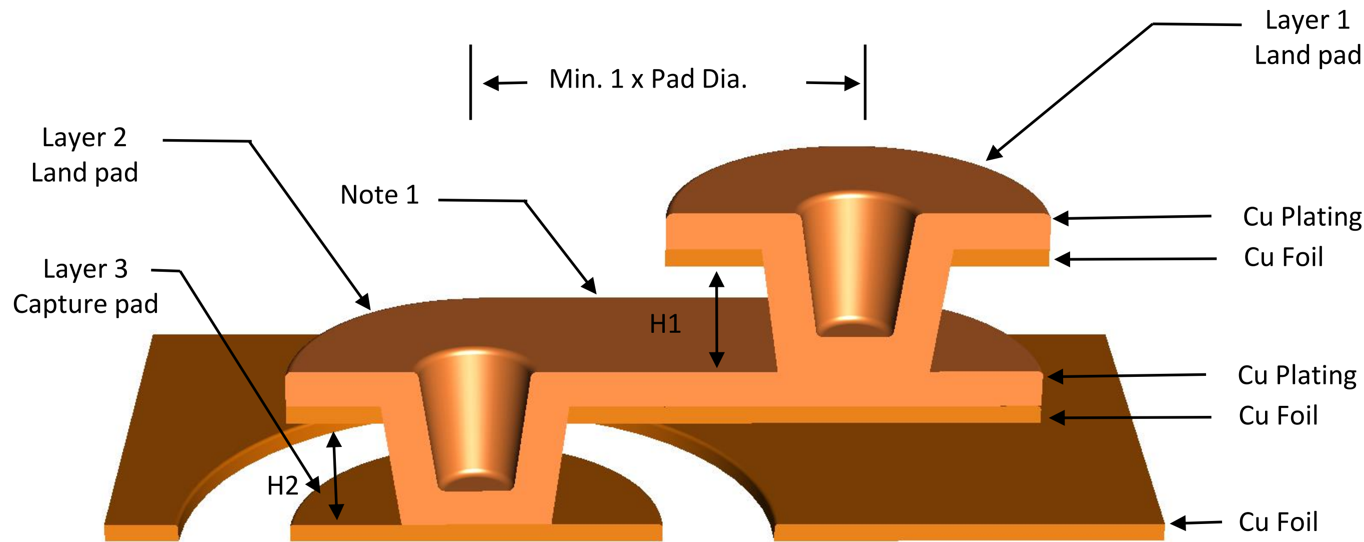
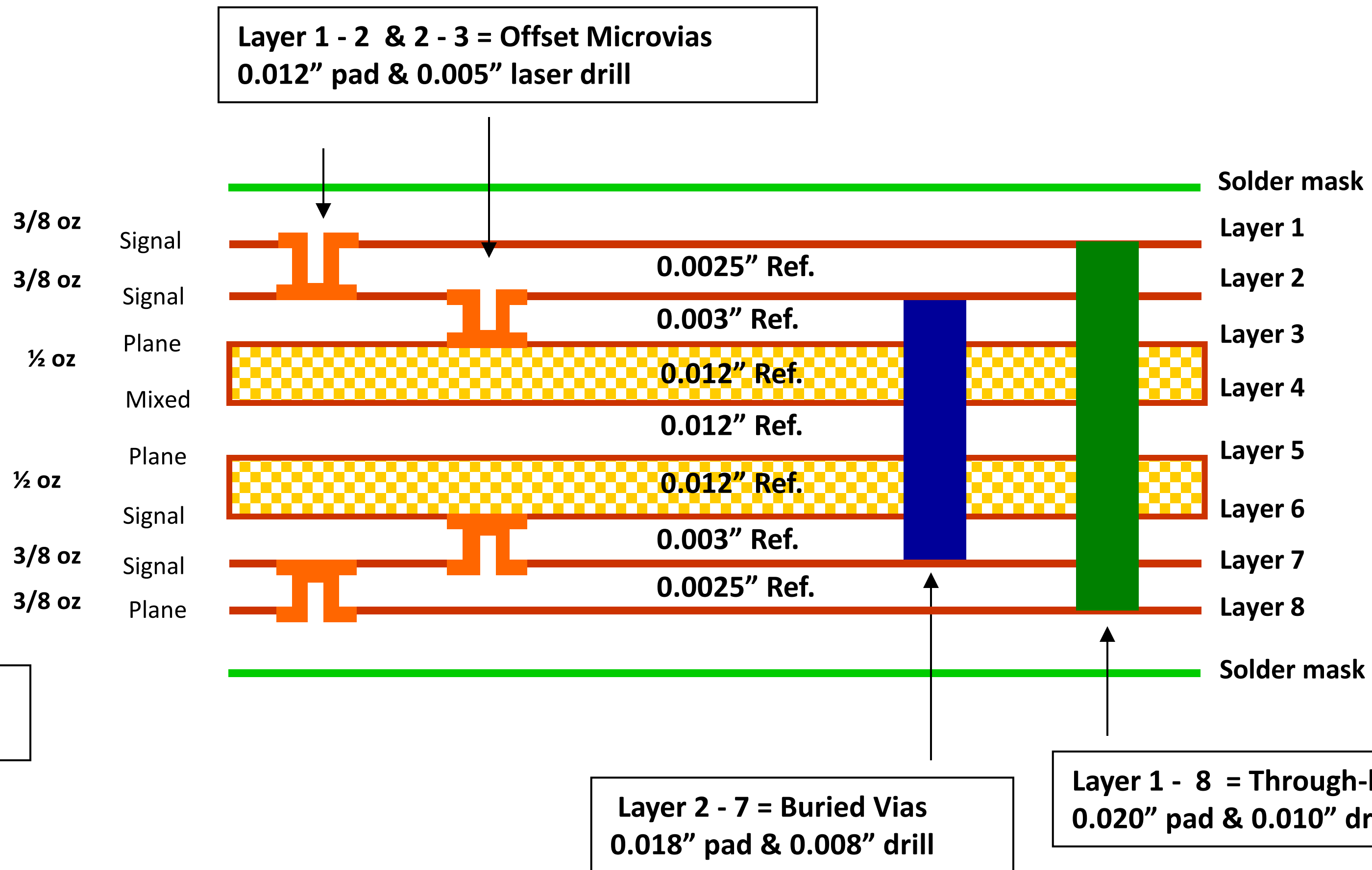
First Generation Microvia Geometries:
(“Staircase” Structure)



Example: Two layer offset “Staircase” microvia structure making a connection from layer 1 to Layer 3. Microvias from layer 2 to 3 does not require a plated copper fill, where as the microvia from layer 1 to 2, copper fill is optional but recommended for via-in-pad. H1 and H2 represent the dielectric thickness between layers and standard design rules apply.

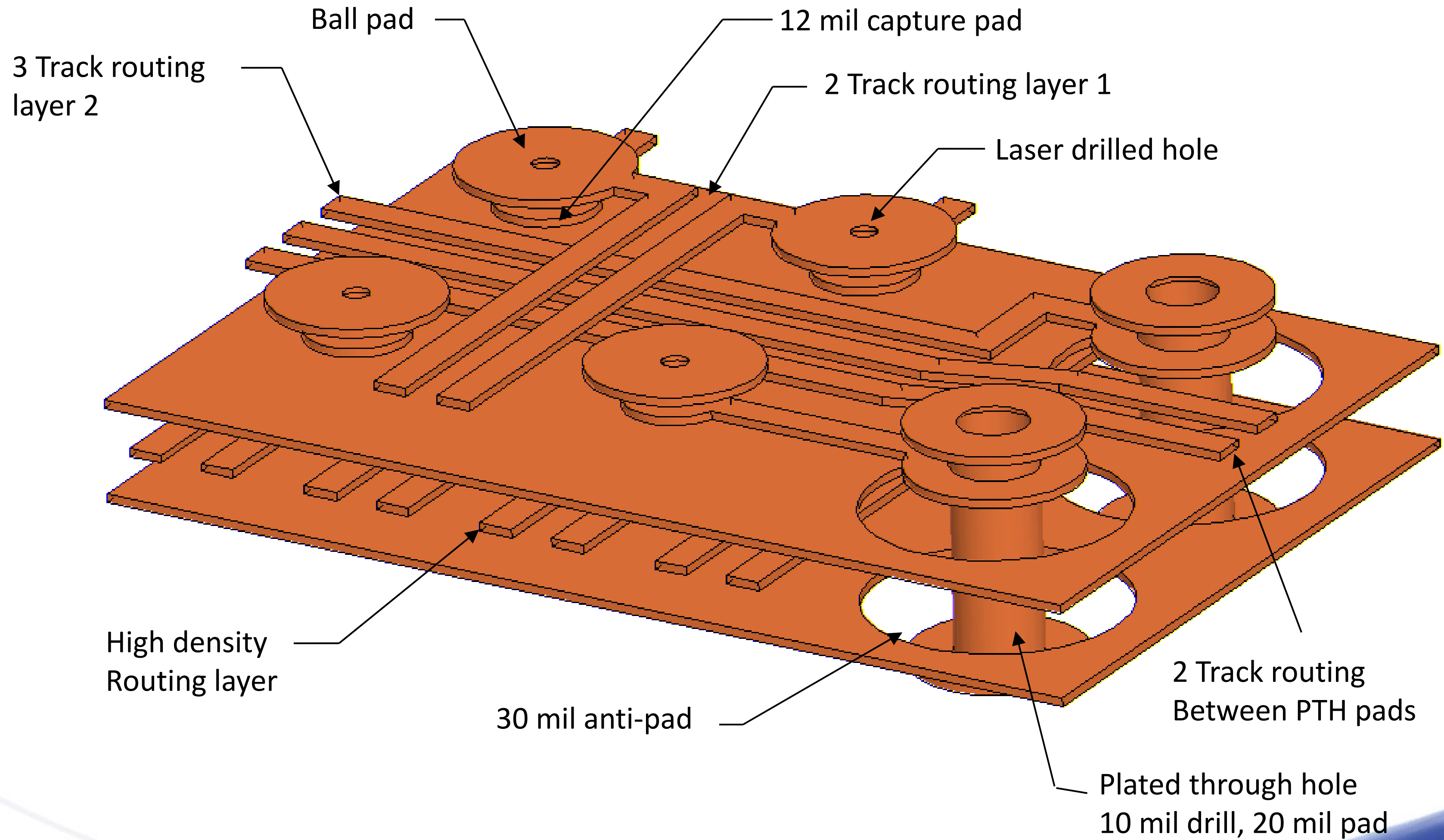
1- Layer two consists of the 1:2 capture pad and the 2:3 land pad positioned tangent to each other. In order to avoid an acute angle between the two round geometries a fillet is required to make an oblong pad.

First Generation Microvia Geometries: ("Staircase" Structure)



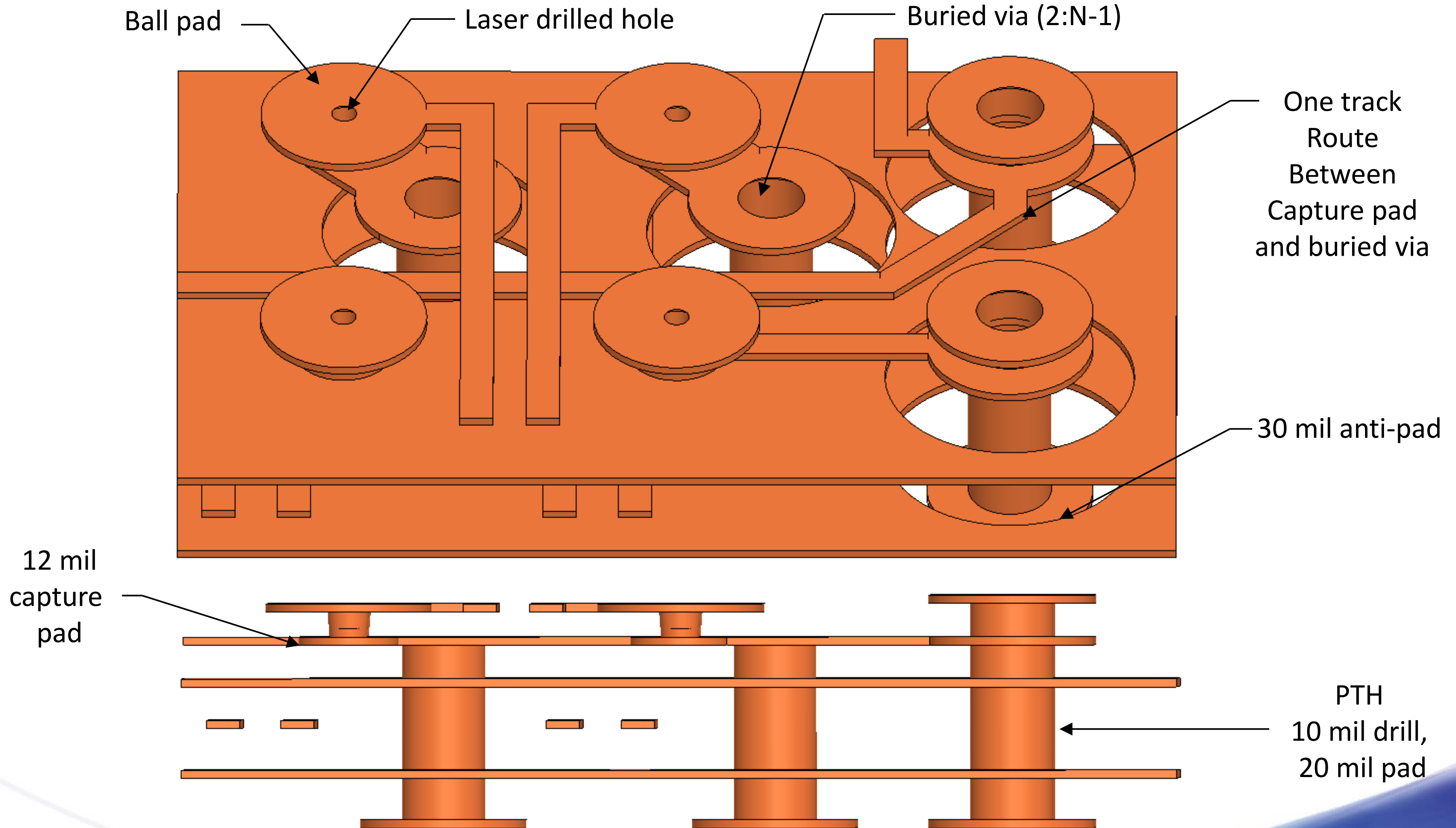
Finish Thickness = 0.062" +/- 0.006"
Material = High temp FR4

First Generation Microvia Examples: Microvia Through Hole Combo 1.0 mm

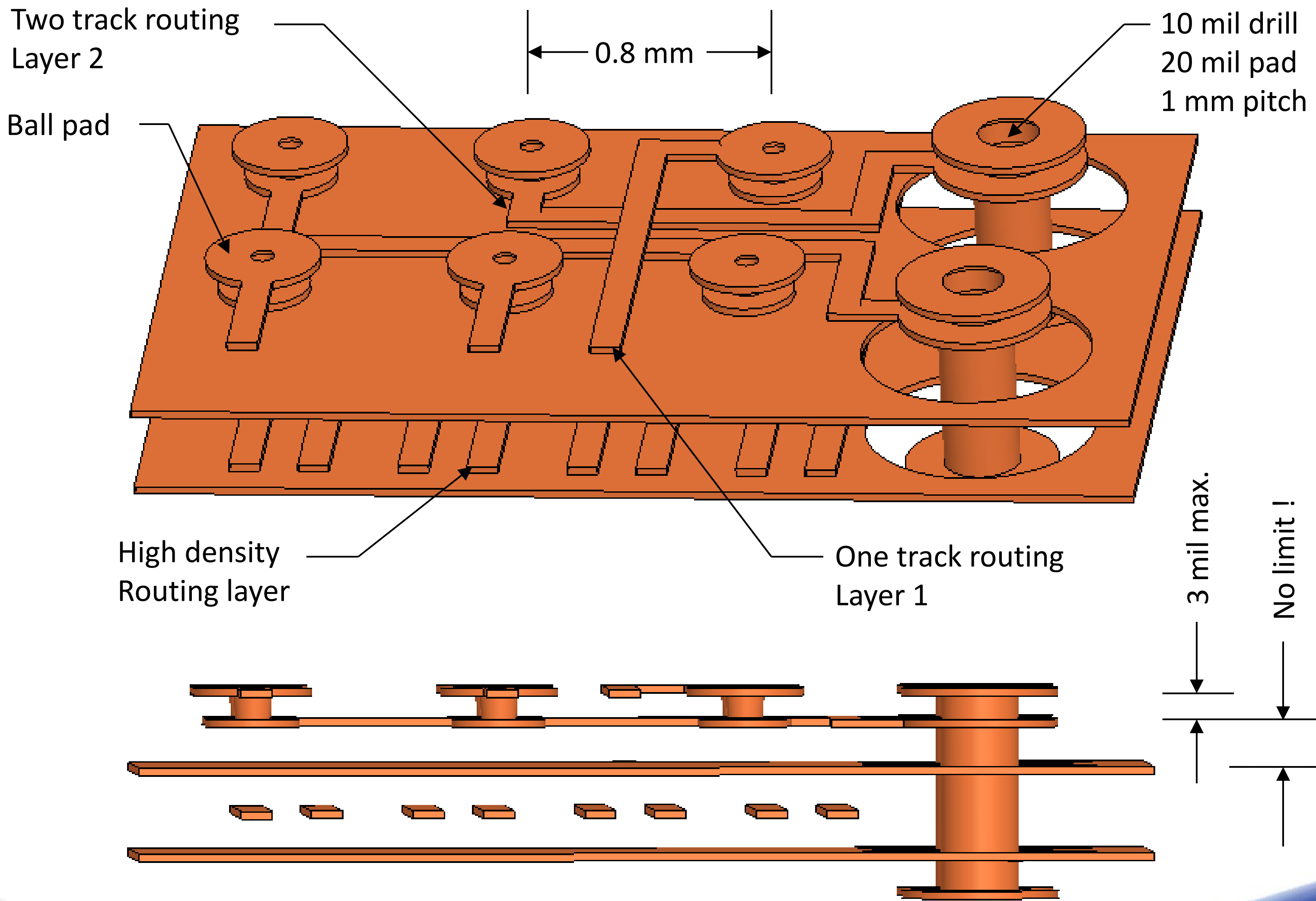


First Generation Microvia Examples:

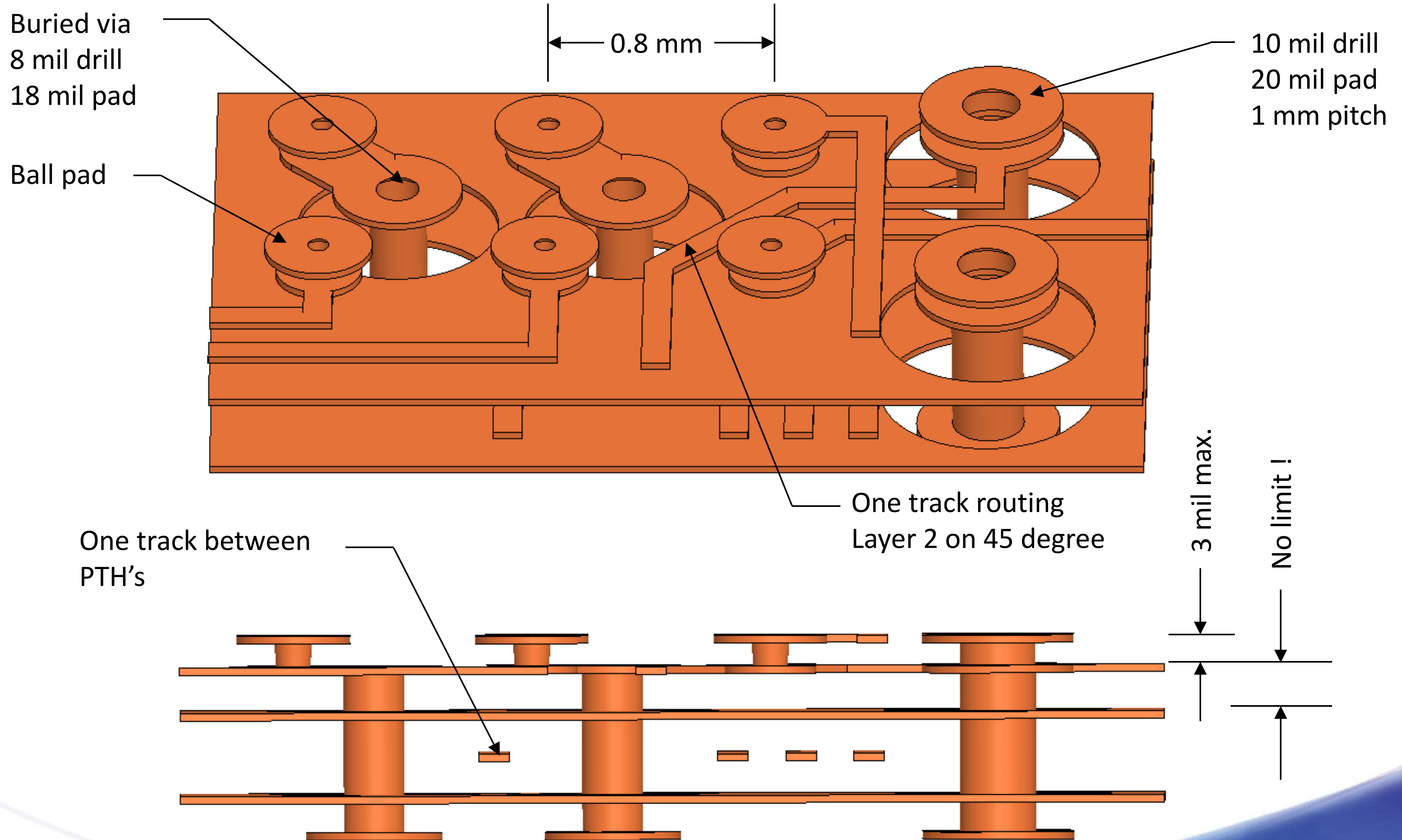
microvia & Buried & PTH Vias 1.0 mm (Min Offset)



First Generation Microvia Examples: Microvia Through Hole Combo 0.8 mm



First Generation Microvia Examples: Microvia Through Hole & Buried Combo 0.8 mm



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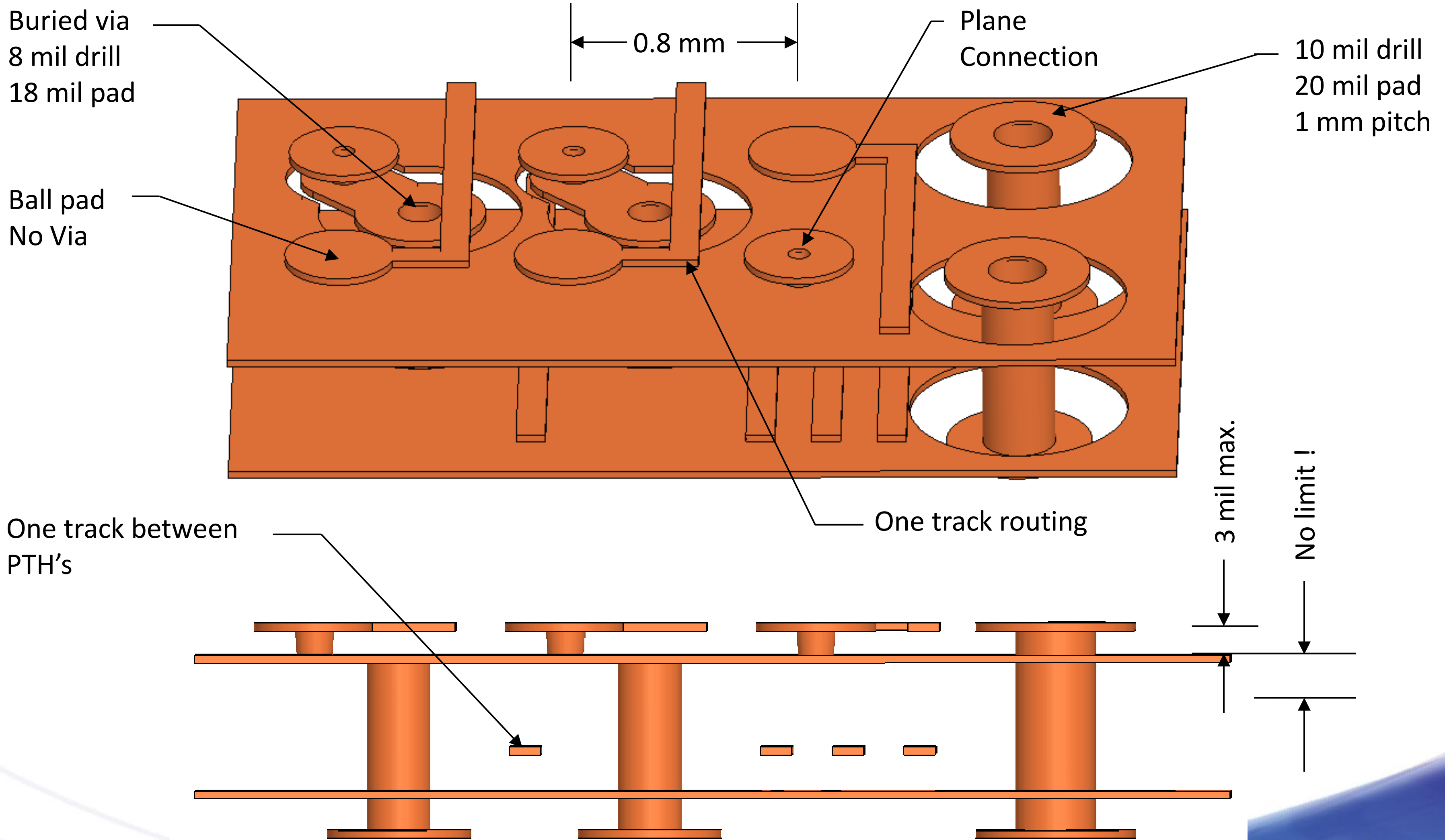
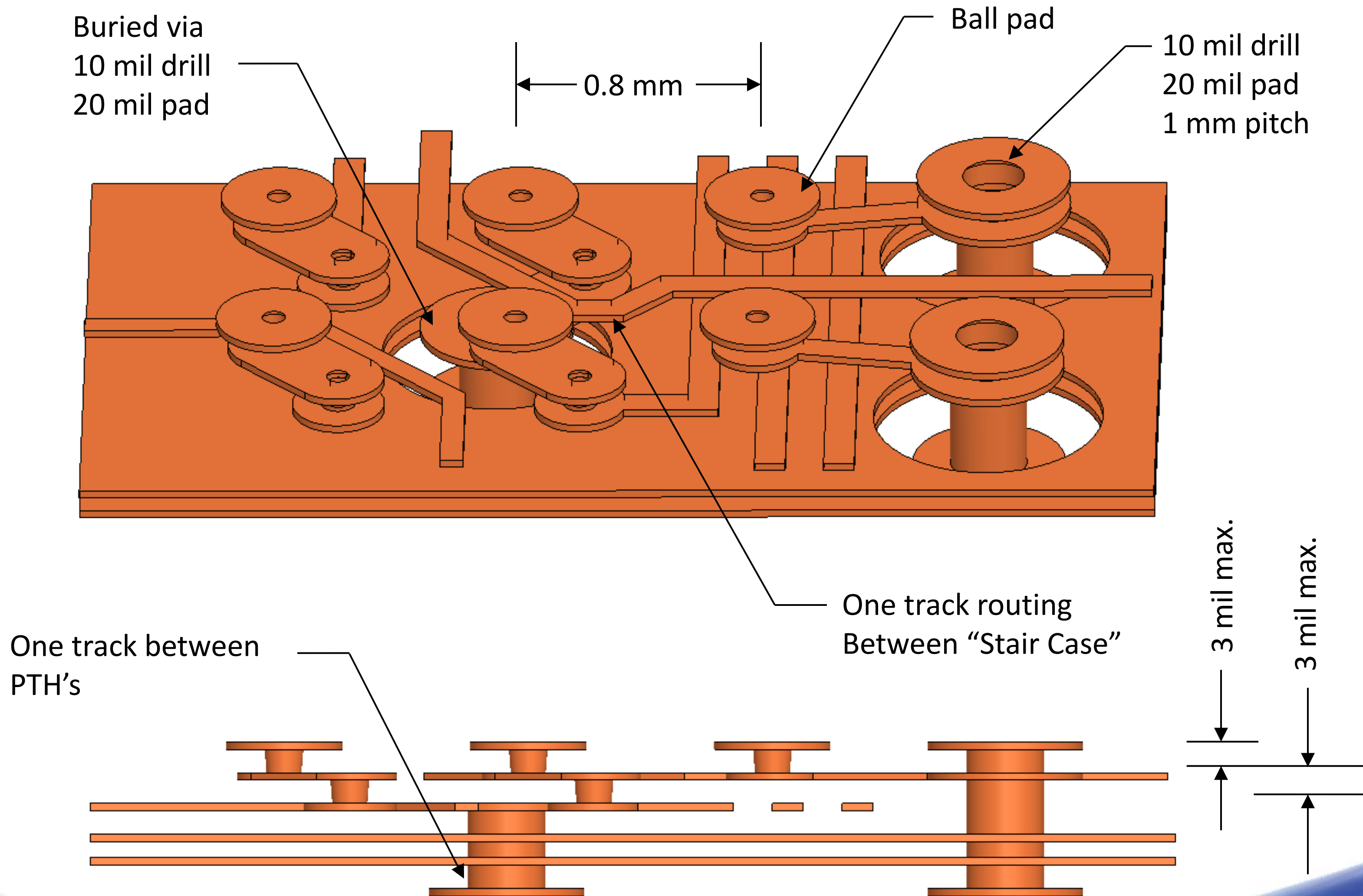
First Generation Microvia Examples: Microvia Through Hole & Buried Combo 0.8 mm



First Generation Microvia Examples: Microvia "Stair Case" & Buried Combo 0.8 mm



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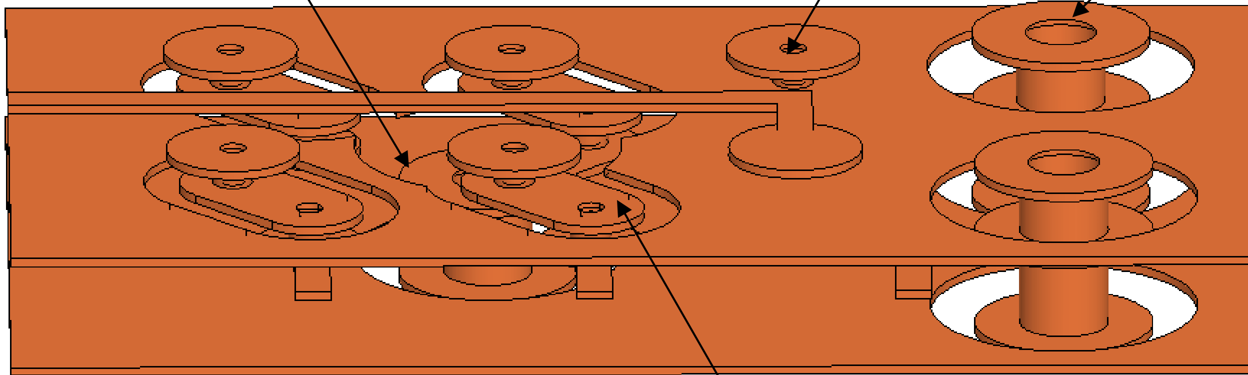
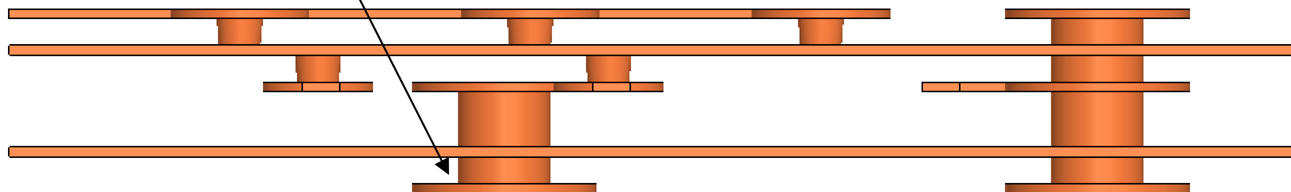
First Generation Microvia Examples: Microvia "Stair Case" & Buried Combo 0.8 mm





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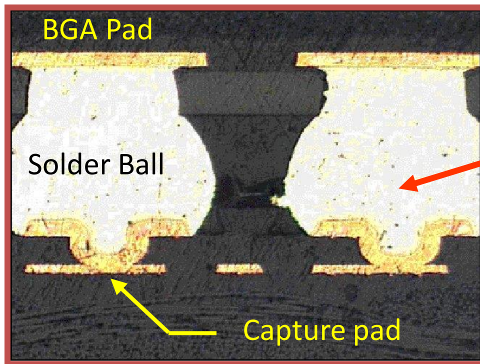
Limitation of first generation microvias

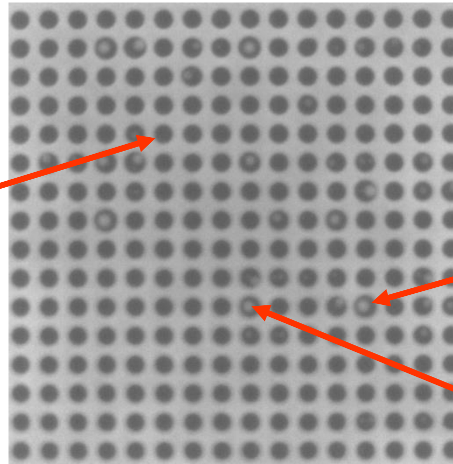
Solder Joint Quality & Reliability…Via-In-Pad Micro Via

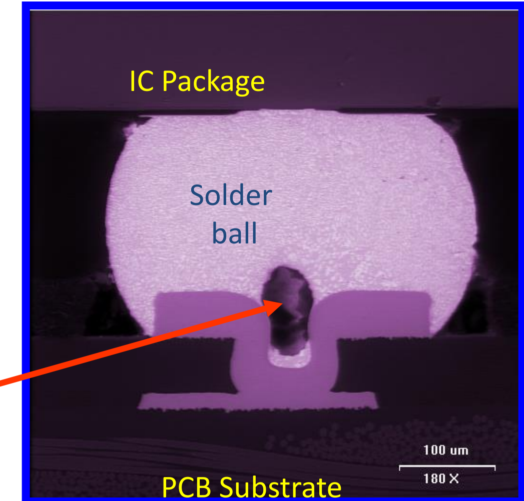
Ideal Solder Joint



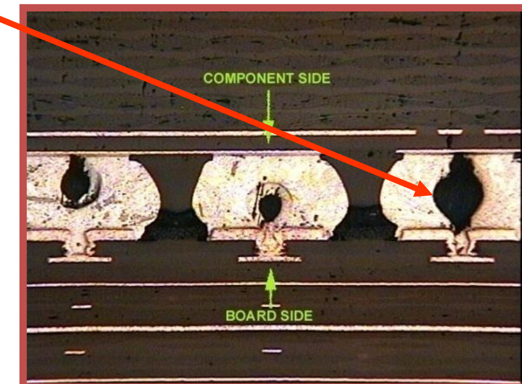
Chip Scale BGA Package with Microvia in Pad

X-Ray of BGA site





Solder void within a solder ball at via-in-pad location



- Microvias vias in pad from layer 1 to 2 must have minimum volume after plating to prevent and or minimize solder voiding due to trapped volatiles
- Even with minimum microvia volume an optimized solder profile is often necessary
- Microvia in excess of 0.005” are too large for via in pad and generally result in solder voiding

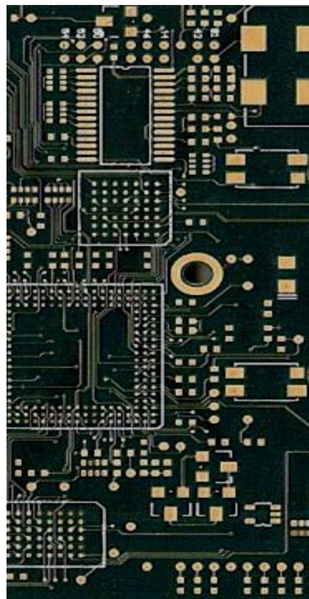
Mechanical Via-In-Pad & Microvia Routing Geometries ?

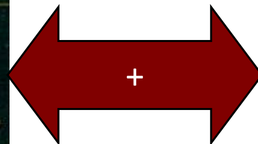
Mechanical via-in-pad requires wrap plating to meet the requirements of IPC 6012. This increases minimum line width and spacing that can be achieved due to increased copper thickness, in general greater than 5 mil line and space. Microvia Designs generally require line width and space less than 5 mils. There is a conflict ?

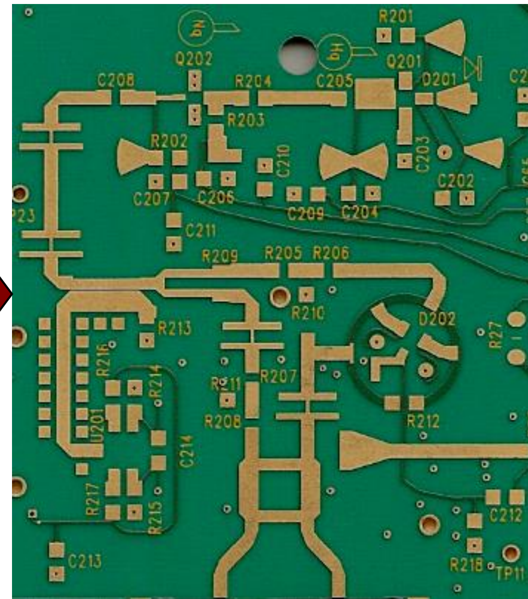
Mixed Signal Design

Chip Scale Digital

- Microvia
- Stacked microvia
- 3 mil line and space







Analog RF/ Microwave

- Via-In-Pad
- Critical line & Space
- Via stub removal
- Mixed depth blind via
- Multiple wrap plating

← Design Conflict ! →

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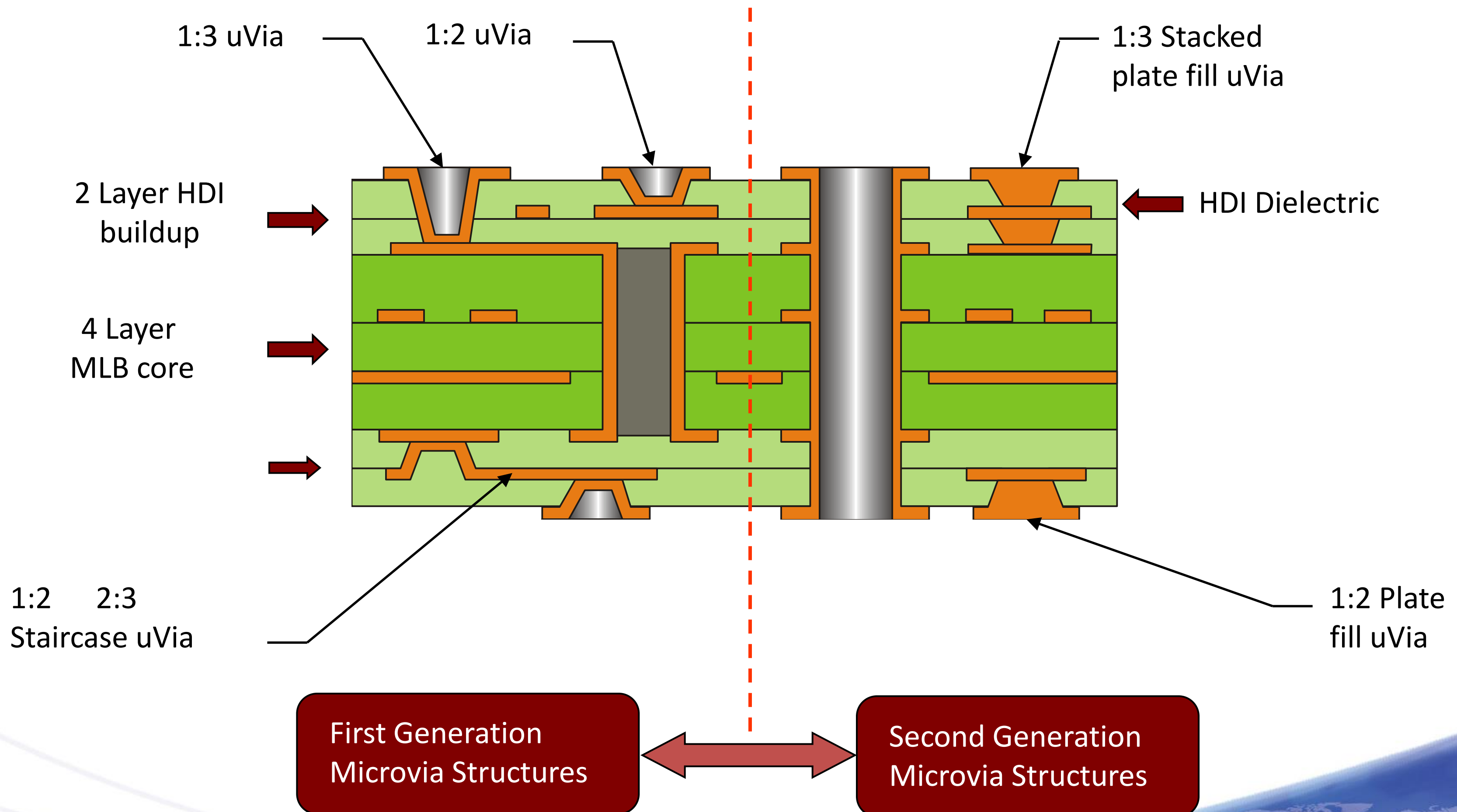
Second Generation Microvias & Applications

First and Second Generation Laser Drilled Microvia Structures



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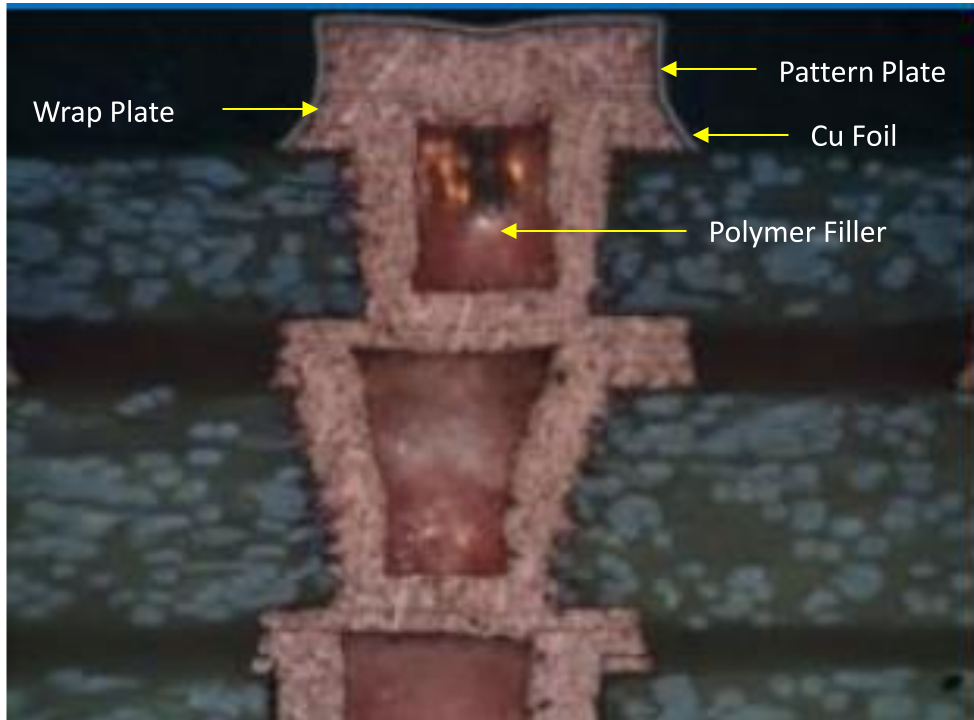
Polymer Filled Microvias

Not Recommended due to Reliability Concerns



Stacked Microvia using polymer fill and copper over-plate

- Basic process for polymer fill
  - Laser drill
  - Electroless copper
  - Electroplate copper
  - Polymer fill
  - Planarize
  - Electroless copper
  - Pattern plate
- Advantages
  - Less capital equipment
  - No special chemistry
- Disadvantages
  - Very difficult to get high percentage fill
  - Wrap plating is required
  - Many process steps

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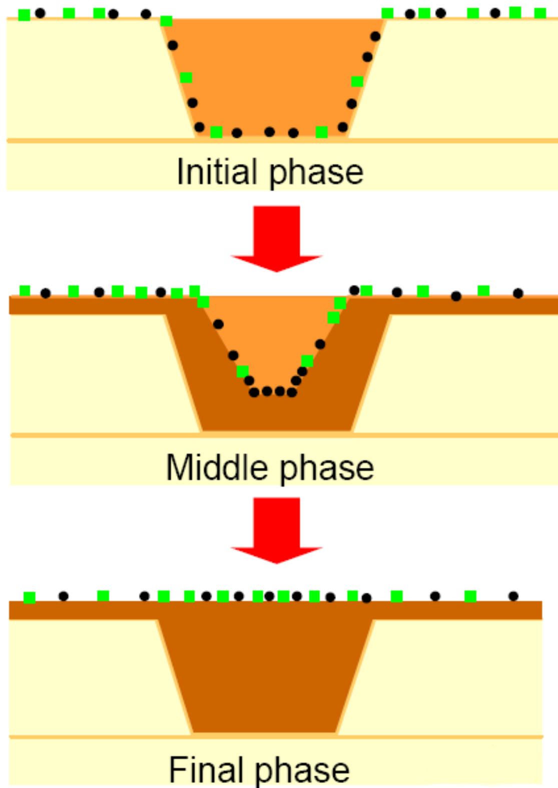
Recommended Fill Method: Solid Copper

Mechanism of copper filling

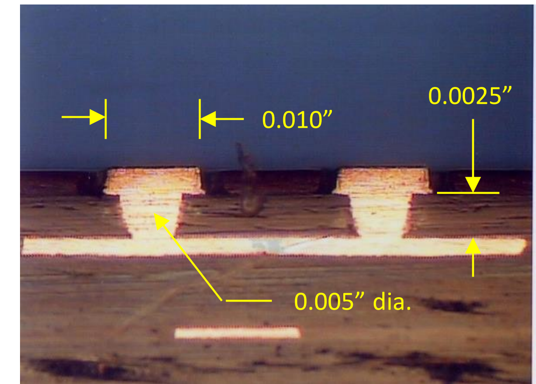


- Bottom-up filling behavior is attributed to the action of organic additives (must be controlled to prescribed limits)
- Suppressor rapidly forms current inhibiting film on Cu surface. Film has little geometric dependence due to high suppressor solution concentration
- Accelerated bottom-up fill behavior is due to a local accumulation of brightener species at the feature base
- As surface area is reduced during deposition, the concentration of brightener species increases, resulting in a non-equilibrium surface concentration. This local concentration of brightener accelerates the plating rate relative to the surface.

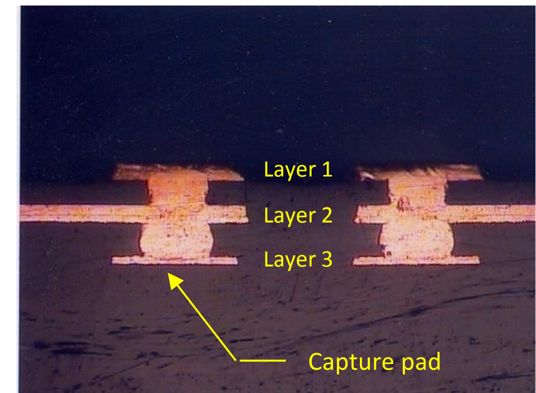
● Brightener

■ Carrier

Planar Microvia



Stacked Microvia



Source: ROHM HAAS ELECTRONIC MATERIALS CIRCUIT BOARD TECHNOLOGIES

Advanced process plating room for solid copper via fill

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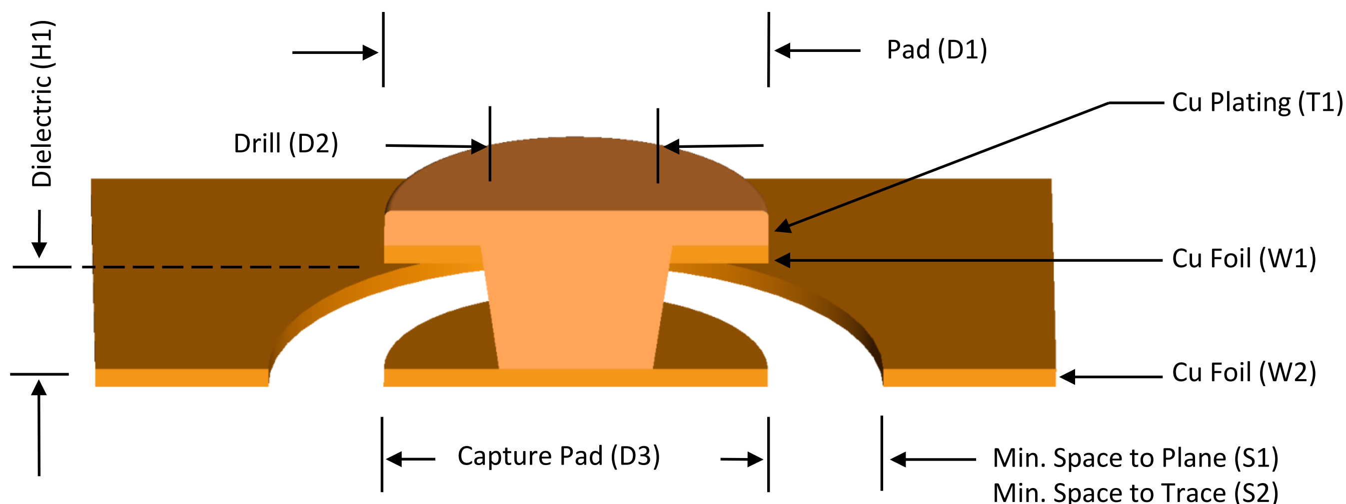
Advanced PCB Structures using Stacked Microvias

- Solid copper microvias can be vertically stacked to gain deeper penetration to internal layers (Design Flexibility)
- In general, laser direct imaging is recommended for proper registration in high density PCB applications
- Stacked microvias require sequential lamination for each additional layer
- The number of vertically stacked layers is limited by the number of lamination cycles that materials are exposed to. In general, most laminates should not be exposed to more than three thermal lamination cycles (4 – 5 Advanced)
- Stacked microvias start with a plating cycle to develop a solid copper filled via, followed by a pattern plate cycle to produce the circuit image. Therefore, the pattern plate thickness must be accounted for in the circuit design

Second Generation Microvia Geometries:

Solid Via Landing on a Non-Plated Layer – Design Guidelines



Microvia Feature Variables		Copper Foil Weight			
		1/4 oz	3/8 oz	1/2 oz	1.0 oz
Layer 1 Copper Foil W1 [2]					
Minimum Pad Diameter [1]	D1	0.008"	0.008"	0.010"	N/A
Pad Thickness: W1 + T1		0.0014"	0.0016"	0.0018"	0.0024"
Layer 2 Copper Foil W2 [2]					
Minimum Space to Plane	S1	N/A	0.0035”	0.004"	0.005"
Minimum Space to Trace [4]	S2	N/A	0.003”	0.0035"	0.004"
Minimum Capture Pad Dia. [1, 5]	D3	N/A	0.008”	0.010"	0.010"
Foil Thickness	W2	N/A	0.00045"	0.0006"	0.0012"
		Minimum	Maximum		
Laser Drill Diameter [3]	D2	0.005"	0.006"		
Dielectric Thickness	H1	0.0025"	0.003"		
Cu Plating Thickness	T1	0.0006"	0.0008”	0.001”	0.001”

Notes:

1- Recommended minimum pad diameters are drill diameter + 0.006”

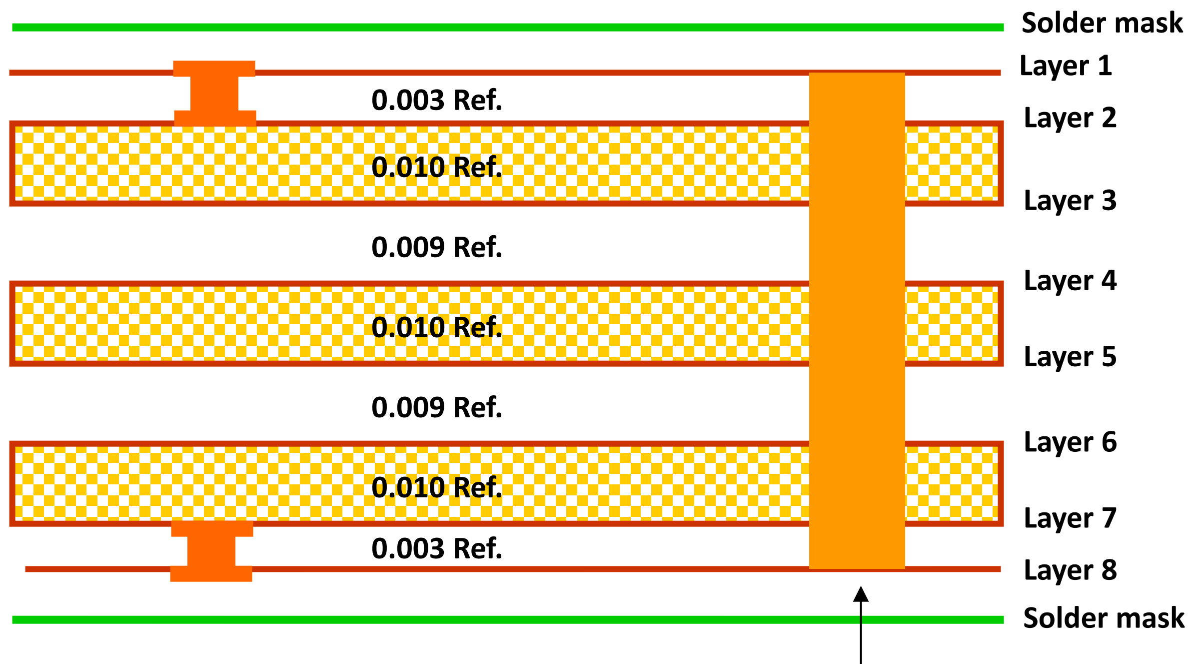
2- 3/8 oz and 1/2 oz Cu foil weight are recommended (design permitting)

3- Larger hole diameter can be achieved with a significant increase in lasing and plating time

4- Minimum pad to trace assumes that the trace will pass the pad tangentially

Second Generation Microvia Geometries:

Solid Via Landing on a Non-Plated Layer



Microvias
Layer 1 - 2
Layer 8 - 7
0.012" pad
0.006" laser drill

Layer 1 – 8 through vias
0.020" pad & 0.010" drill

Finish Thickness = 0.062" +/- 0.006"
Material = High Temp FR4

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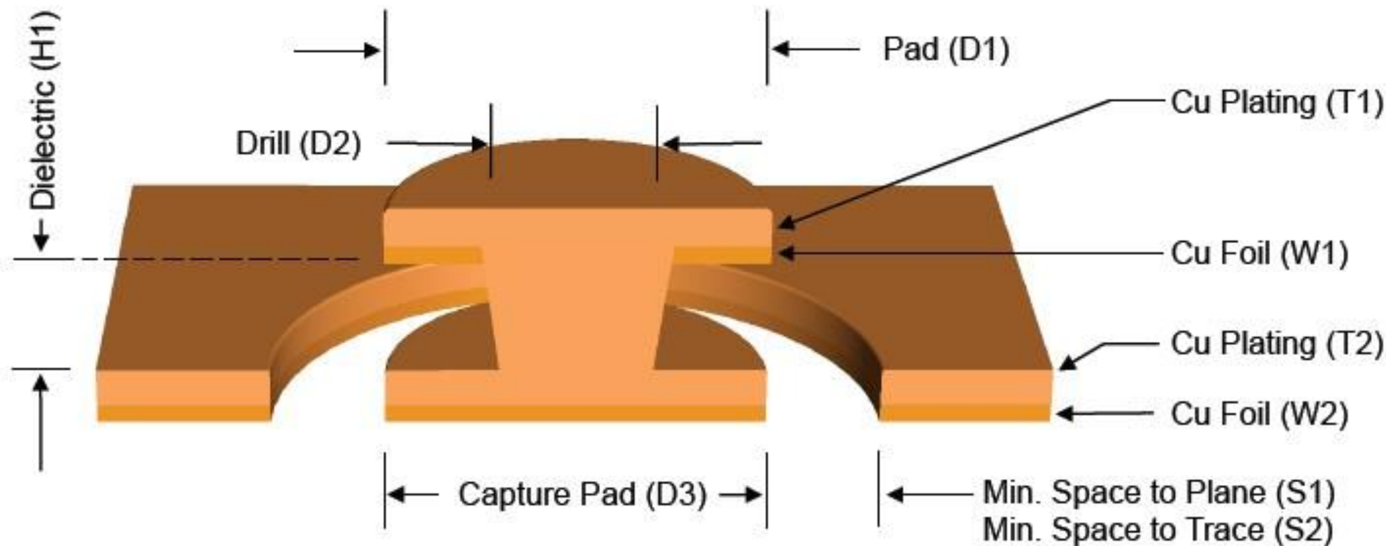
Second Generation Microvia Geometries:

Solid Via Landing on a Plated Layer – Design Guidelines



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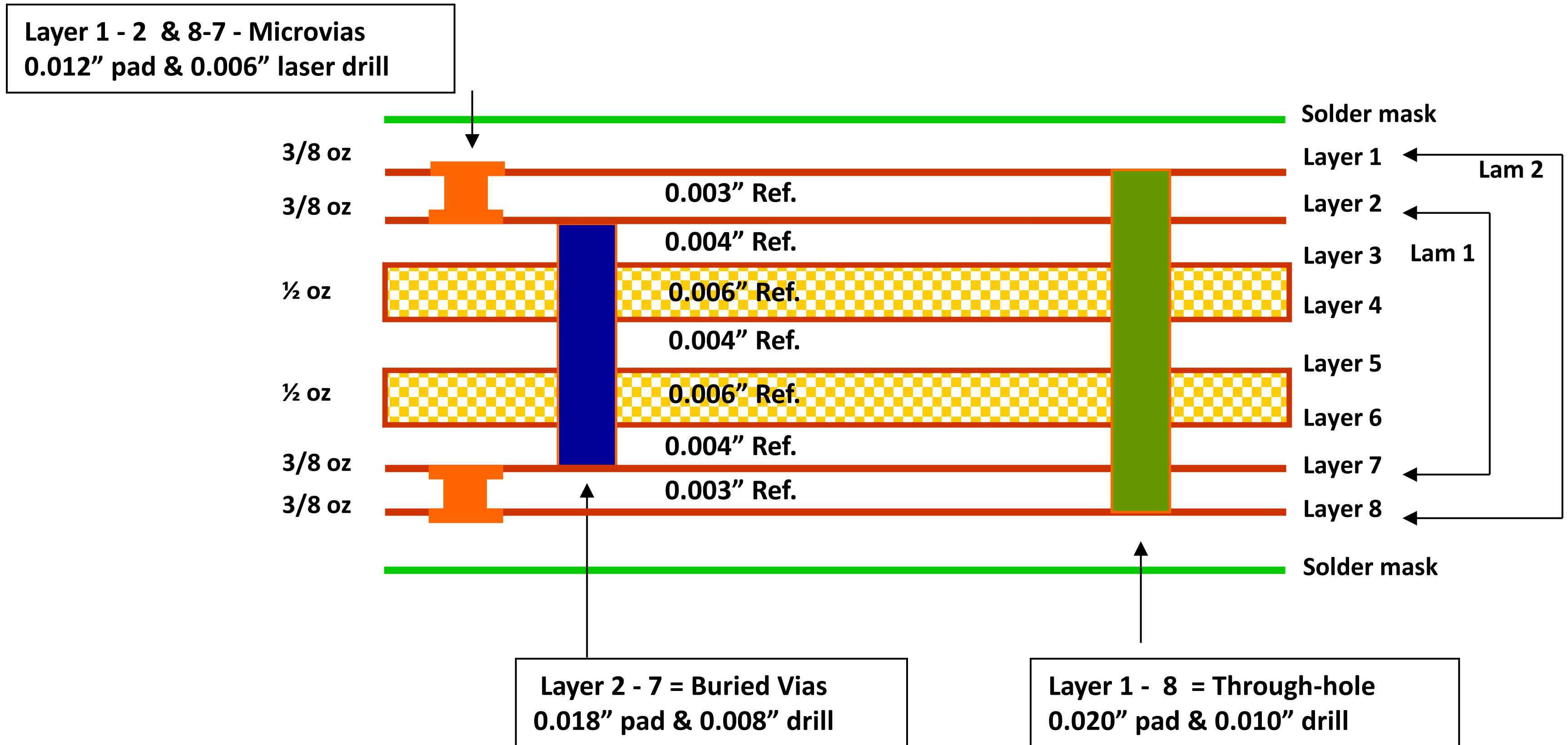
Microvia Feature Variables		**Copper Foil Weight**			
		1/4 oz	3/8 oz	1/2 oz	1.0 oz
Layer 1 Copper Foil W1 [2]					
Minimum Pad Diameter [1]	D1	0.008"	0.008"	0.010"	N/A
Pad Thickness: W1 + T1		0.0014"	0.0016"	0.0018"	N/A
Layer 2 Copper Foil W2 [2]					
Minimum Space to Plane [4]	S1	0.005"	0.005"	0.006"	0.008"
Minimum Space to Trace [4, 5]	S2	0.003"	0.003"	0.0035"	0.004"
Minimum Capture Pad Dia. [1]	D3	0.008"	0.008"	0.010"	0.010"
Plated Layer Thickness W2 +T2		0.0013"	0.0014	0.0016	0.0022"
		Minimum	Maximum		
Laser Drill Diameter [3]	D2	0.004"	0.006"		
Dielectric Thickness	H1	0.0025"	0.003"		
Cu Plating Thickness	T1	0.0012"			
Copper Plating Thickness	T2	0.001"			

Notes:

1- Recommended minimum pad diameters are drill diameter + 0.006"
2- 3/8 oz and 1/2 oz Cu foil weight are recommended design permitting
3- Larger hole diameter can be achieved with a significant increase in lasing and plating time
4- Non-standard increased plating thickness (Wrap plating ect.) will increase minimum space
5- Minimum pad to trace assumes that the trace will pass the pad tangentially

Second Generation Microvia Geometries:

Solid Via Landing on a Plated Layer



Finish Thickness = 0.042” +/- 0.004”

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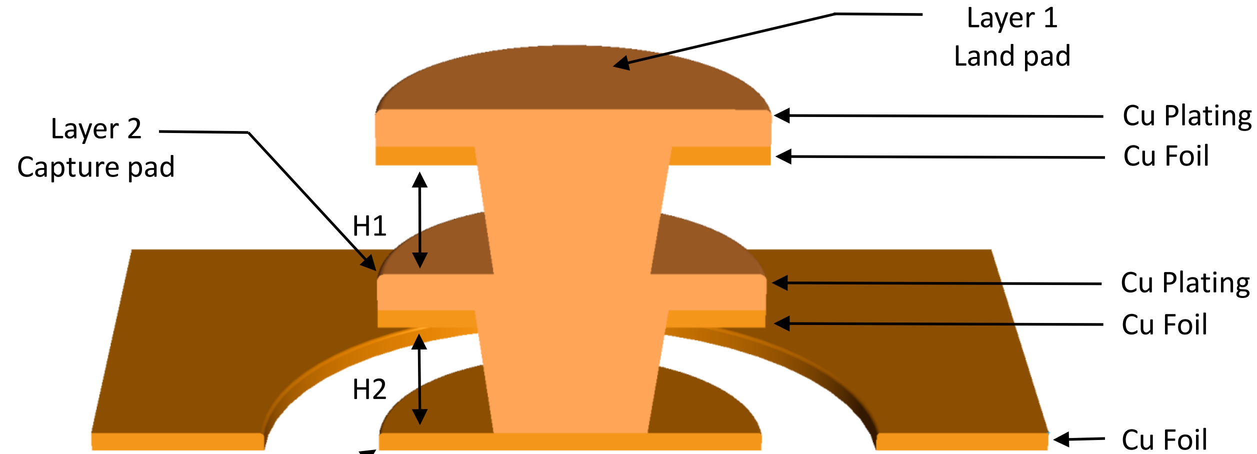
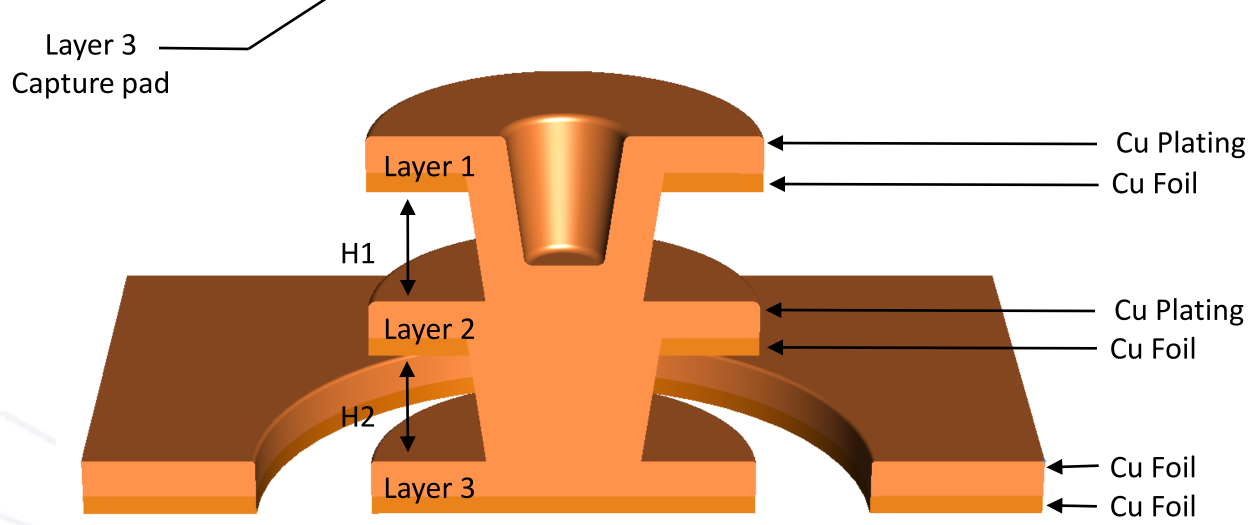
Second Generation Microvia Geometries: Stacked Microvia Examples





Example 1: Two layer stacked microvia (+2) terminating on a copper foil shown with a copper plate-fill on the layer 1 to layer 2 via for via-in-pad application. H1 and H2 represent the dielectric thickness between layers and standard design rules apply.

Example 2: Two layer stacked microvia (+2) terminating on a plated layer. This example illustrates how the internal solid copper vias become the building block for the vias on top until you get to the layer 1 to 2 via. The final 1 to 2 via has the option to be filled with copper (recommended for via-in-pad) or they can be left as a standard via with a divot if used as an interstitial via. H1 and H2 represent the dielectric thickness between the layers where standard microvia rules apply.

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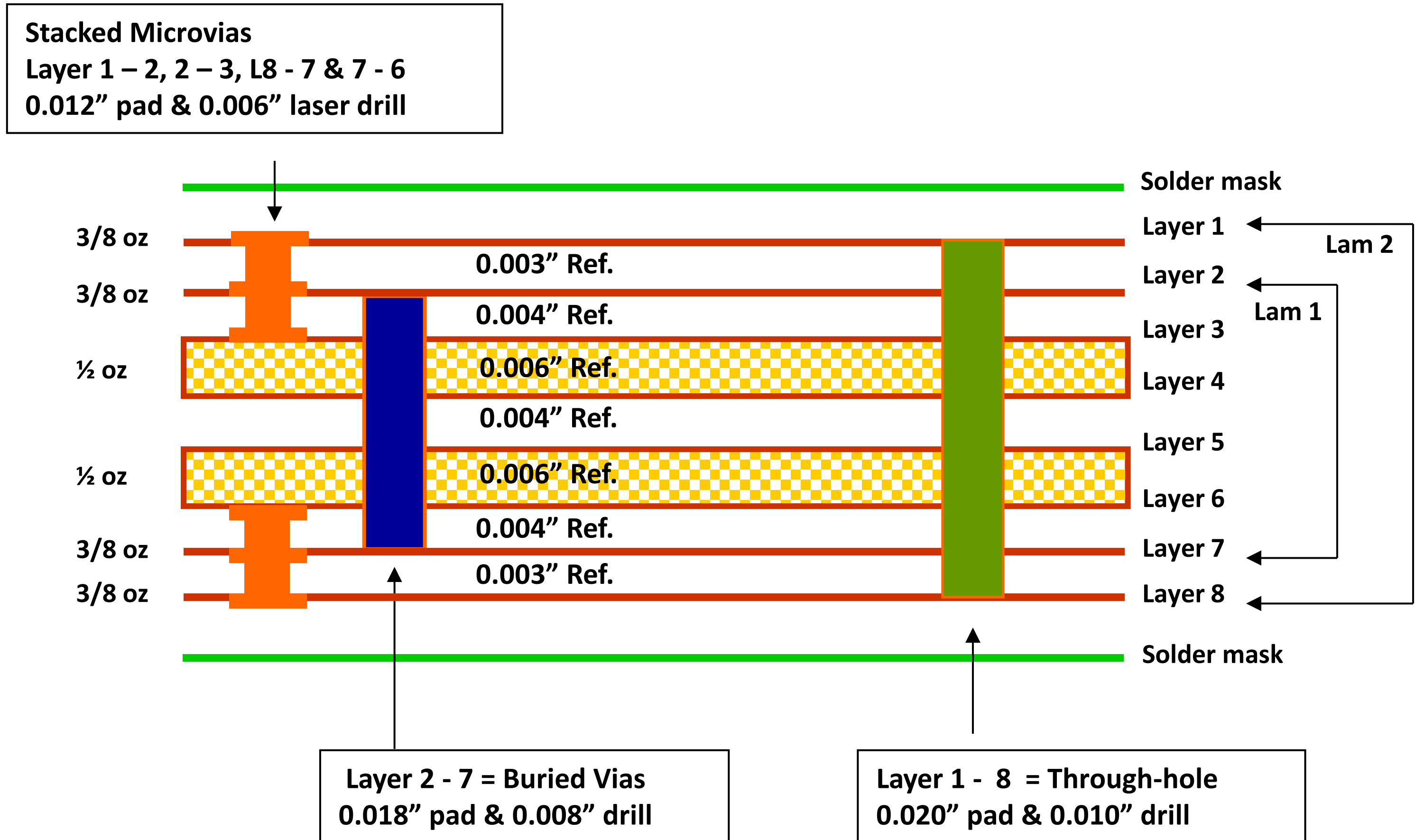
Second Generation Microvia Geometries:

Solid Via Landing on a Non-Plated Layer



Finish Thickness = 0.042” +/- 0.005”

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Second Generation Microvia Geometries:

Solid Via Landing on a Non-Plated Layer

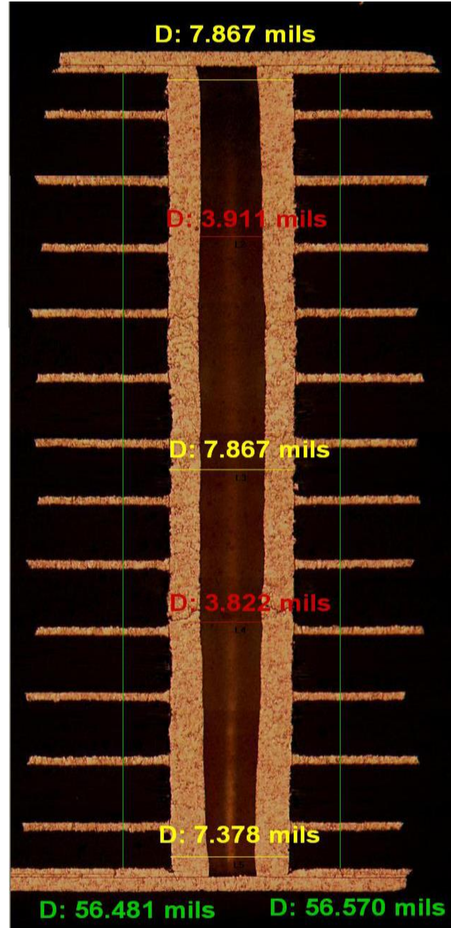
Microsection After Buried Via (*FLAT-WRAP™)* Cycled To Failure
# of HATS cycles passed = 0.008" – 2,604 & 0.010" – 3,278

Lyr# Type:	Lam Cycles:	Description:	Copper:	Laminate / PrePreg:	Base Material:
	21				
1 Sig		Foil (T oz)	.00045		
		Preg(1x1080-HRC)		.0026 +/- 0.0005	Polyclad FR370 HR
		Sub Plating	.00100		
2 Sig		Foil (T oz)	.00045		
		Preg(1x1080)		.0026 +/- 0.0005	Polyclad FR370 HR
3 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
4 Mix			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
5 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
6 Sig			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
7 Mix		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
8 Sig			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
9 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
10 Mix			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
11 Sig		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
12 Sig			.00060		
		Preg(2x106)		.0040 +/- 0.0005	Polyclad FR370 HR
13 Mix		Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
14 Sig			.00060		
		Preg(1x1080)		.0026 +/- 0.0005	Polyclad FR370 HR
15 Sig		Foil (T oz)	.00045		
		Sub Plating	.00100		
		Preg(1x1080-HRC)		.0026 +/- 0.0005	Polyclad FR370 HR
16 Sig		Foil (T oz)	.00045		
	21				

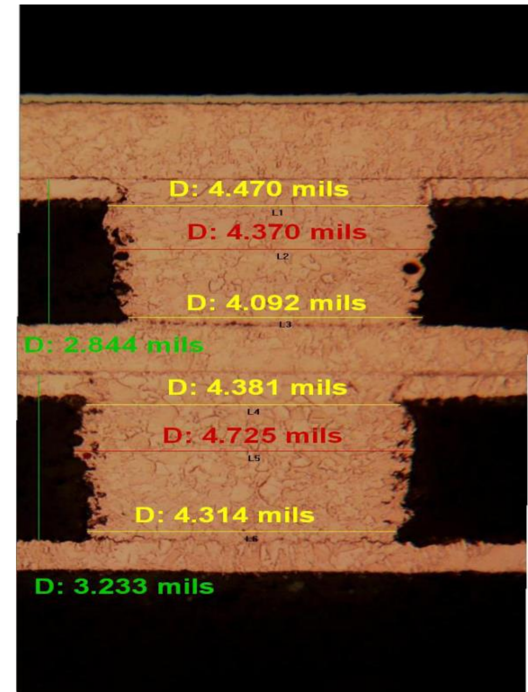
Drill: Plated / CondFill / NonCond — Laser: Plated / SMV — Impedance Layers

Impedance Requirements: L# / Impedance Type	Original Line	Finish Line	1st Ref. Pln.	2nd Ref. Pln.	Z-Ohms (Calc'd)	Z Ohms & Tolerances (+/-%) (Required)	Diff Center to Center	Coplanar Spacing (Original)	Coplanar Spacing (Finished)

Controlled Impedance Notes:	Stackup Notes:
	- CAUTION: MIN. DIELECTRICS BETWEEN 1-2, 2-3, 14-15 & 15-16 ARE .0019.



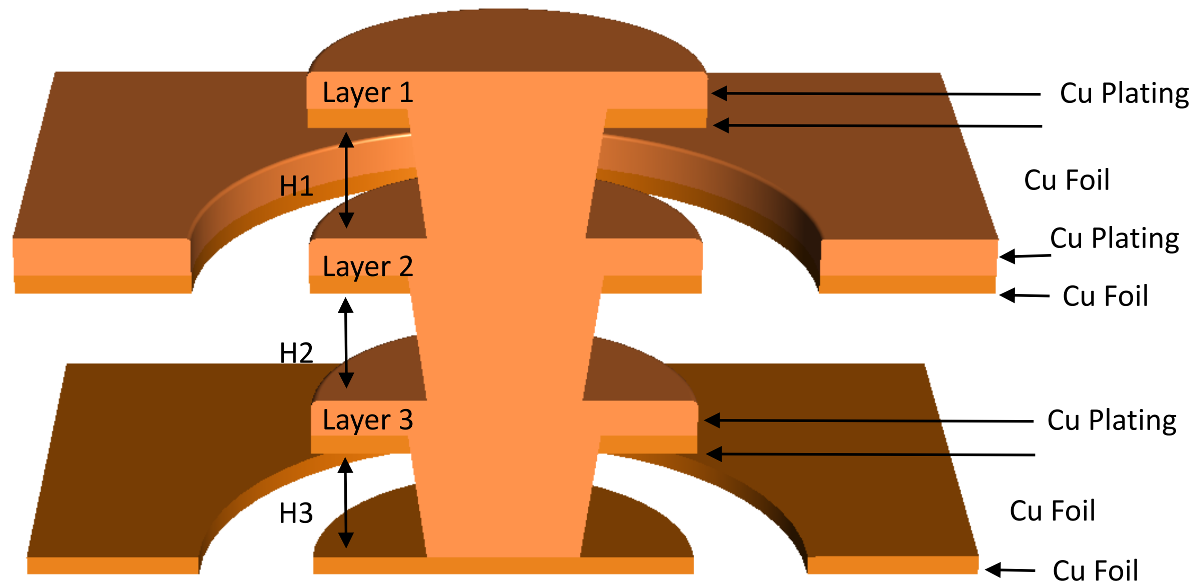
SMV™ - L1-L2/L2-L3
0.004" & 0.005" vias
Passed 5,000 HATS cycle



16 Layer, 2+N+2, Stacked Microvia / Staggered Buried Via
PCB Thickness 0.072" +/- 10%

Second Generation Microvia Geometries:

Stacked MicroVia Landing on a Non-Plated Layer



Example 3: Three layer stacked microvia (+3) terminating on a Cu foil layer. In this example Stacked vias are making a connection from layer 1 to layer 4 where layer 4 is the second layer of the primary sub lamination thereby terminating on a foil layer. Vias from layer 2 to 3 and 1 to 2 both require sequential lamination and as a result become plated layers adding additional thickness. In Addition, layers 2 and 4 are shown as plane layers however, they could just as easy be signal layers, the important point to note, is that copper thickness is dependant on specific stack-up requirements since build-up layers do require copper plating.

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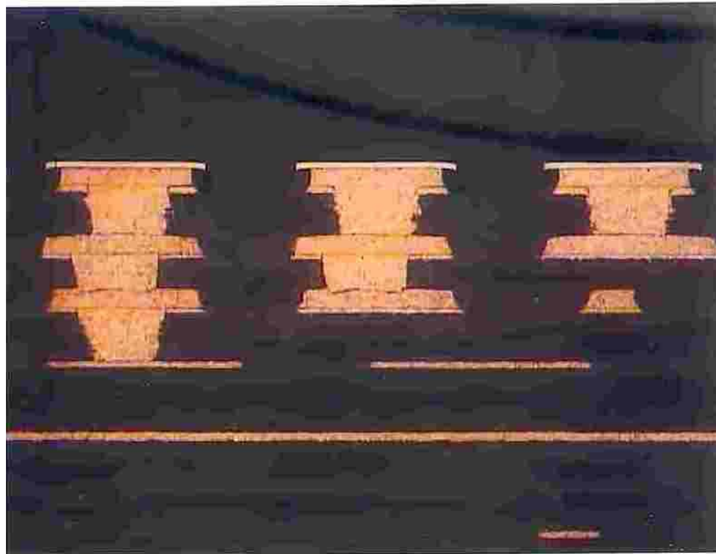
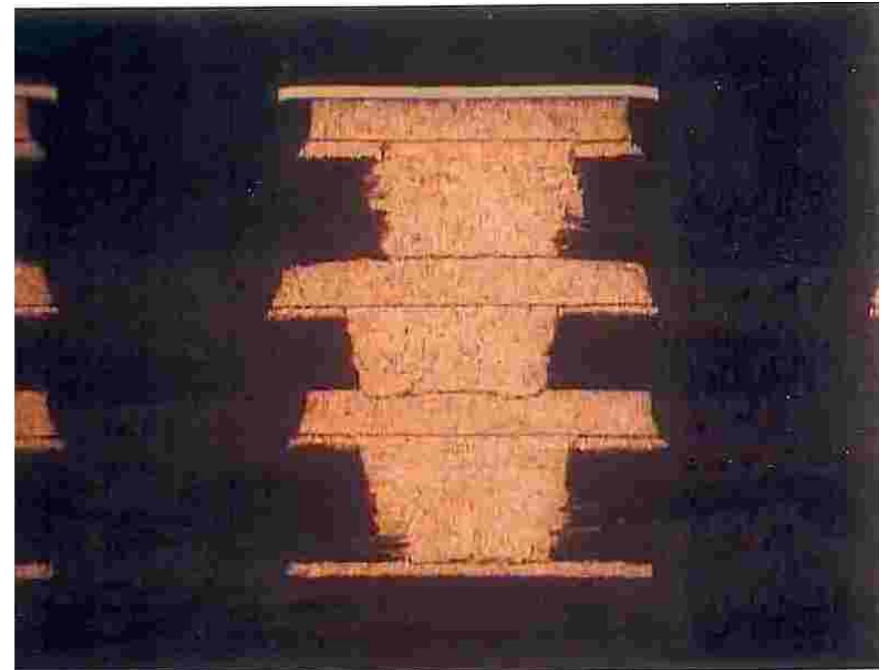
Second Generation Microvia Geometries:

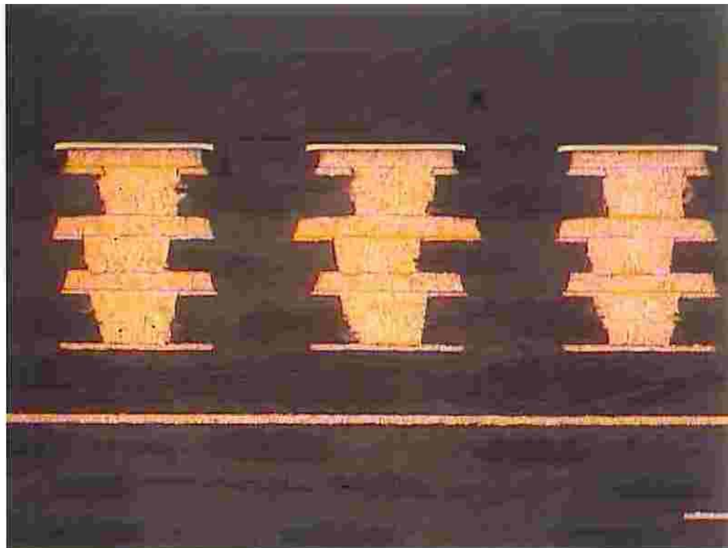
Stacked MicroVia Landing on a Non-Plated Layer



Stacked MicroVia (*SMV®*)

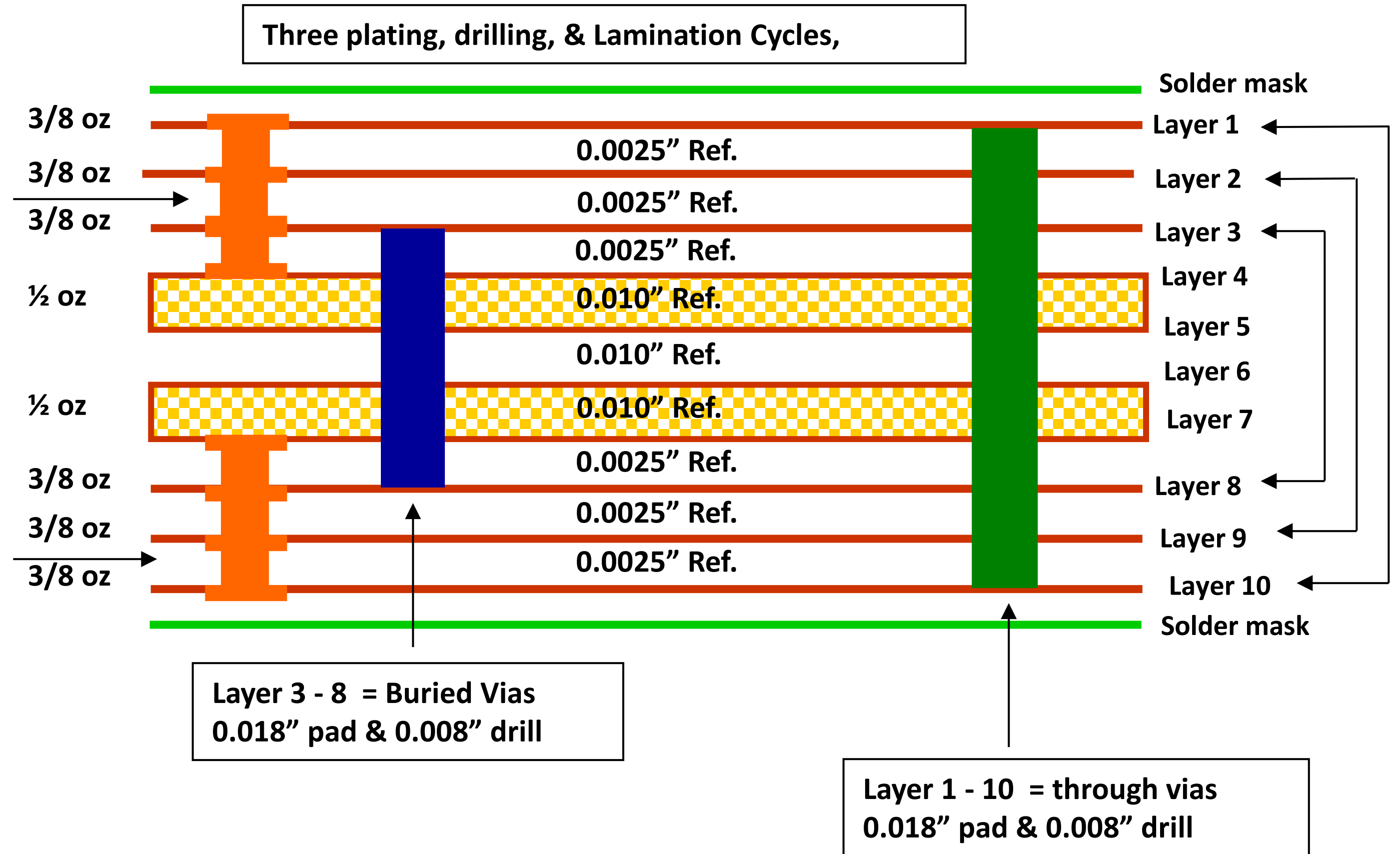
L1-L2, L1-L3 & L1-L4





Second Generation Microvia Geometries: Stacked Microvia Examples

Microvias
Layer 1 - 2
Layer 2 - 3
Layer 3 - 4
0.009” pad external
0.011” pad internal
0.005” laser drill
Solid copper plate



Microvias
Layer 10 – 9
Layer 9 – 8
Layer 8 – 7
0.009” pad external
0.011” pad internal
0.005” laser drill
Solid copper plate

This construction is for Reference only
dielectrics will be fine tuned by factory

Finish Thickness = 0.062” +/- 0.007”
Material = High Temperature FR4

Second Generation Microvia Geometries

Solution for sub 0.5 mm pitch arrays

Microsection After Buried Via (*FLAT-WRAP™)* Cycled To Failure

# of HATS cycles passed = 0.25 mm – 1,337 & 0.3 mm – 1,716

Lyr # Type	Lam Cycles	Drill: Plated / CondFill / NonCond	Laser: Plated / SMV	Description: (Impedance Layers)	Thickness and Tolerances: Copper:	Laminate / PrePreg:	Base Material:
1 Sig	21			Foil (T oz)	.00045		
				Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
				Sub Plating	.00100		
2 Sig				Foil (T oz)	.00045		
				Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
				Sub Plating	.00100		
3 Sig				Foil (T oz)	.00045		
				Preg(1x1080)		.0025 +/- 0.0005	Polyclad FR370 HR
4 Sig				Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
5 Pln					.00060		
				Preg(1x106)		.0050 +/- 0.0005	Polyclad FR370 HR
				Preg(1x1080-HRC)			
6 Sig				Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
7 Sig					.00060		
				Preg(1x106)		.0050 +/- 0.0005	Polyclad FR370 HR
				Preg(1x1080-HRC)			
8 Mix				Core 0.0050 H/H	.00060	.0050 +/- 0.0005	Polyclad FR370 HR
9 Sig					.00060		
				Preg(1x106)		.0050 +/- 0.0005	Polyclad FR370 HR
				Preg(1x1080-HRC)			
10 Sig				Core 0.0050 H/H	.00060	.0050 +/- 0.0005	Polyclad FR370 HR
11 Pln					.00060		
				Preg(1x1080-HRC)		.0050 +/- 0.0005	Polyclad FR370 HR
				Preg(1x106)			
12 Sig				Core 0.0050 H/H	.00060	.0050 +/- 0.0005	Polyclad FR370 HR
13 Mix					.00060		
				Preg(1x1080-HRC)		.0050 +/- 0.0005	Polyclad FR370 HR
				Preg(1x106)			
14 Sig				Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
15 Sig					.00060		
				Preg(1x1080-HRC)		.0050 +/- 0.0005	Polyclad FR370 HR
				Preg(1x106)			
16 Pln				Core 0.0040 H/H	.00060	.0040 +/- 0.0005	Polyclad FR370 HR
17 Sig					.00060		
				Preg(1x1080)		.0025 +/- 0.0005	Polyclad FR370 HR
18 Sig				Foil (T oz)	.00045		
				Sub Plating	.00100		
				Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
19 Sig				Foil (T oz)	.00045		
				Sub Plating	.00100		
				Preg(1x1080-HRC)		.0025 +/- 0.0005	Polyclad FR370 HR
20 Sig	21			Foil (T oz)	.00045		

Impedance Requirements: L#	Impedance Type	Original Line	Finish Line	1st Ref. Pln.	2nd Ref. Pln.	Z-Ohms (Calc'd)	Z Ohms & Tolerances (+/-%) (Required)	Diff Center to Center	Coplanar Spacing (Original)	Coplanar Spacing (Finished)

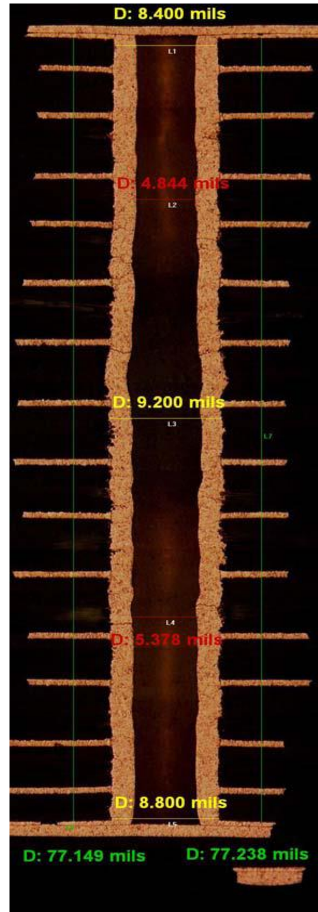
Controlled Impedance Notes:

Stackup Notes:

- CAUTION: MIN. DIELECTRICS BETWEEN LAYERS 1-2, 2-3, 3-4, 17-18, 18-19 & 19-20 ARE .0019

20 Layer, 3+N+3, Stacked Microvia / Staggered Buried Via

PCB Thickness 2.46 mm +/- 10%

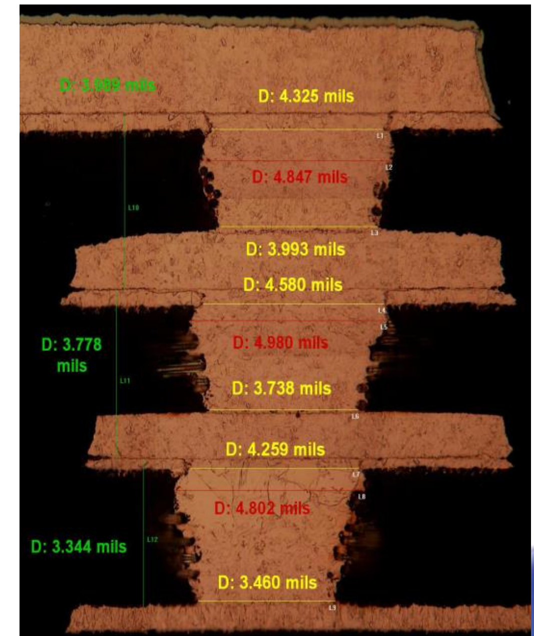


SMV® - L1-L2/L2-L3/L3-L4

# of HATS cycle passed

0.1 mm vias – 3,513

0.127 mm vias – 5,000



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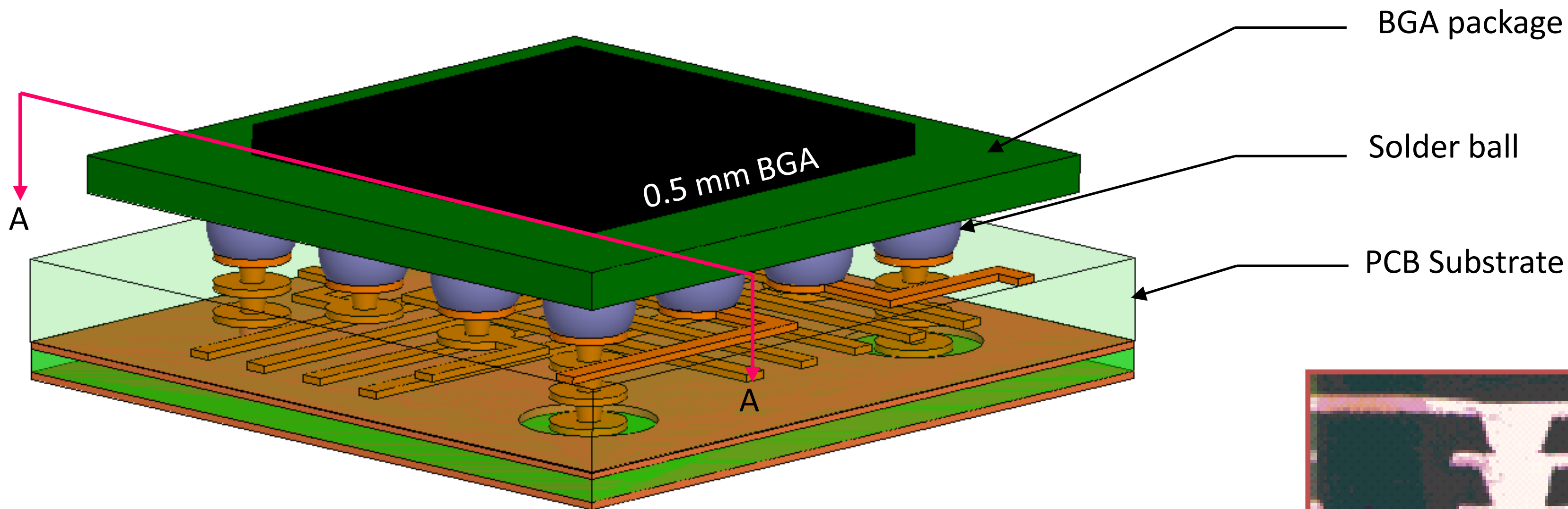
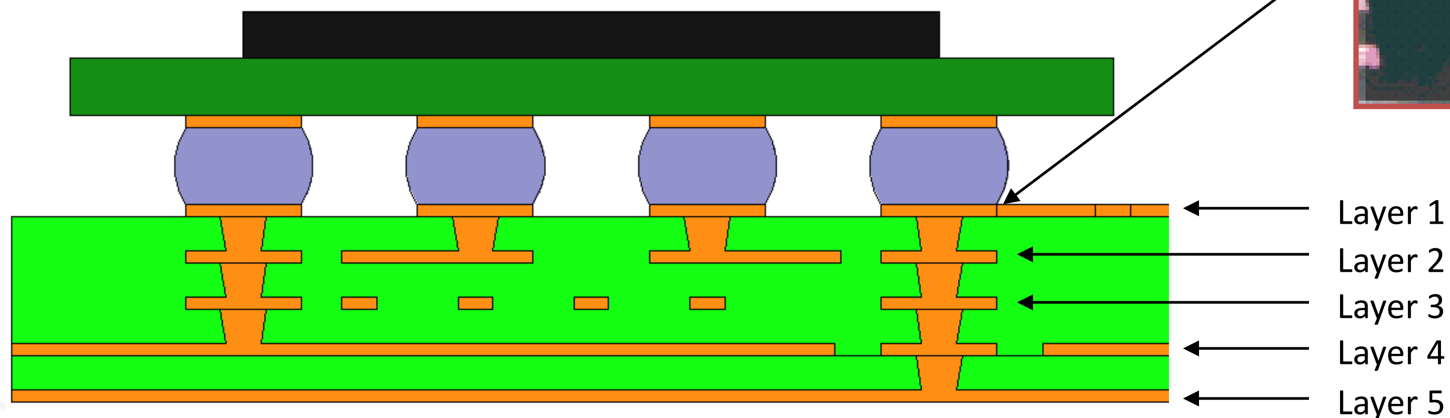
Chip Scale BGA Escape using Stacked Microvias





Section A-A: 4 layer stacked microvia structure*

Only top 5 layers of the board are shown

TTM Technologies

Microvia Sub-lamination Interface Techniques

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Advanced PCB Structures using Stacked Microvias

- Solid copper microvias can be vertically stacked to gain deeper penetration to internal layers (Design Flexibility)

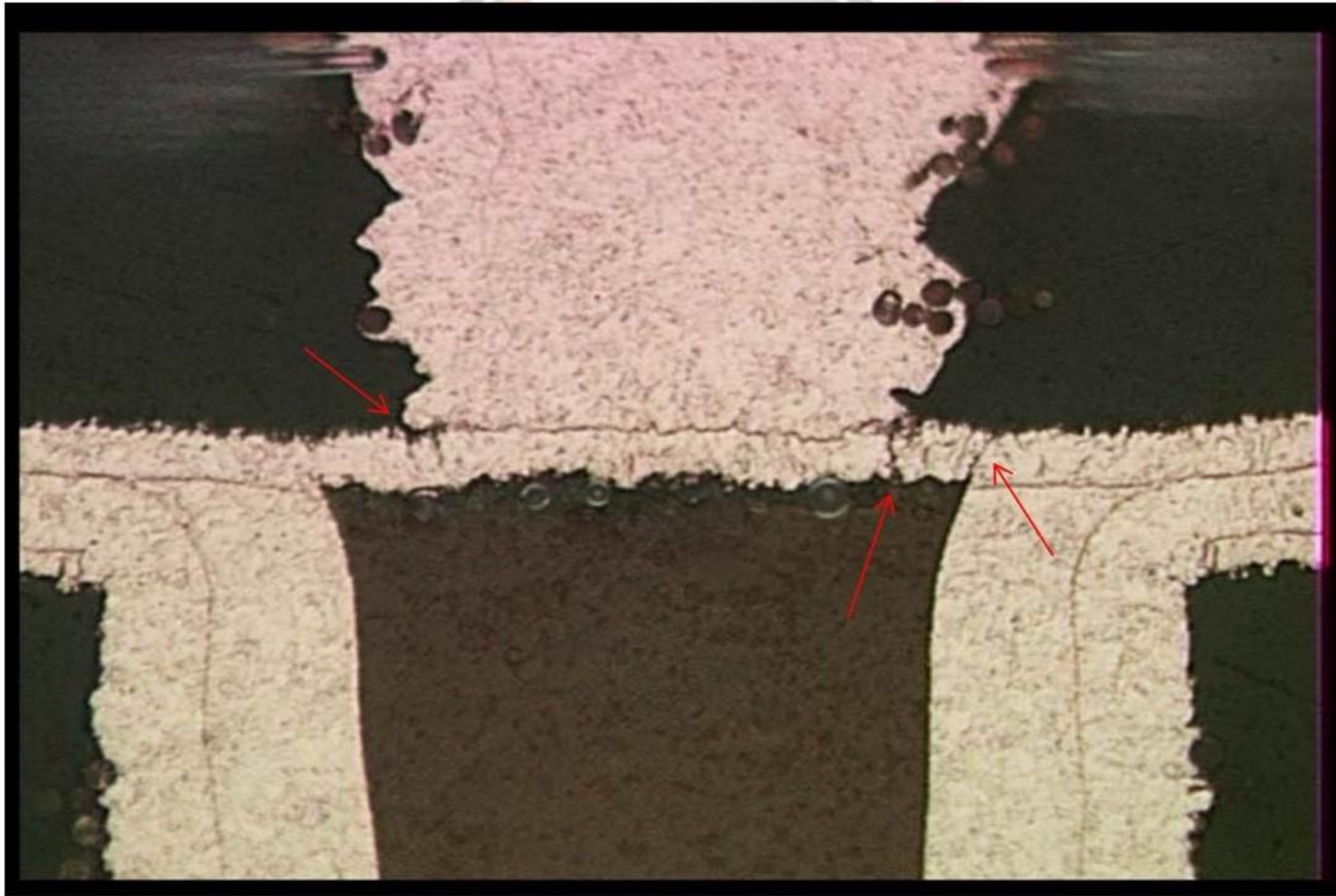
- In general, laser direct imaging is recommended for proper registration in high density PCB applications

- Stacked microvias require sequential lamination for each additional layer

- The number of vertically stacked layers is limited by the number of lamination cycles that materials are exposed to. In general, most laminates should not be exposed to more than three thermal lamination cycles (4 – 5 Advanced)

- Stacked microvias start with a plating cycle to develop a solid copper filled via, followed by a pattern plate cycle to produce the circuit image. Therefore, the pattern plate thickness must be accounted for in the circuit design

Microvia stacked on Epoxy-filled Mechanical Via – NO!



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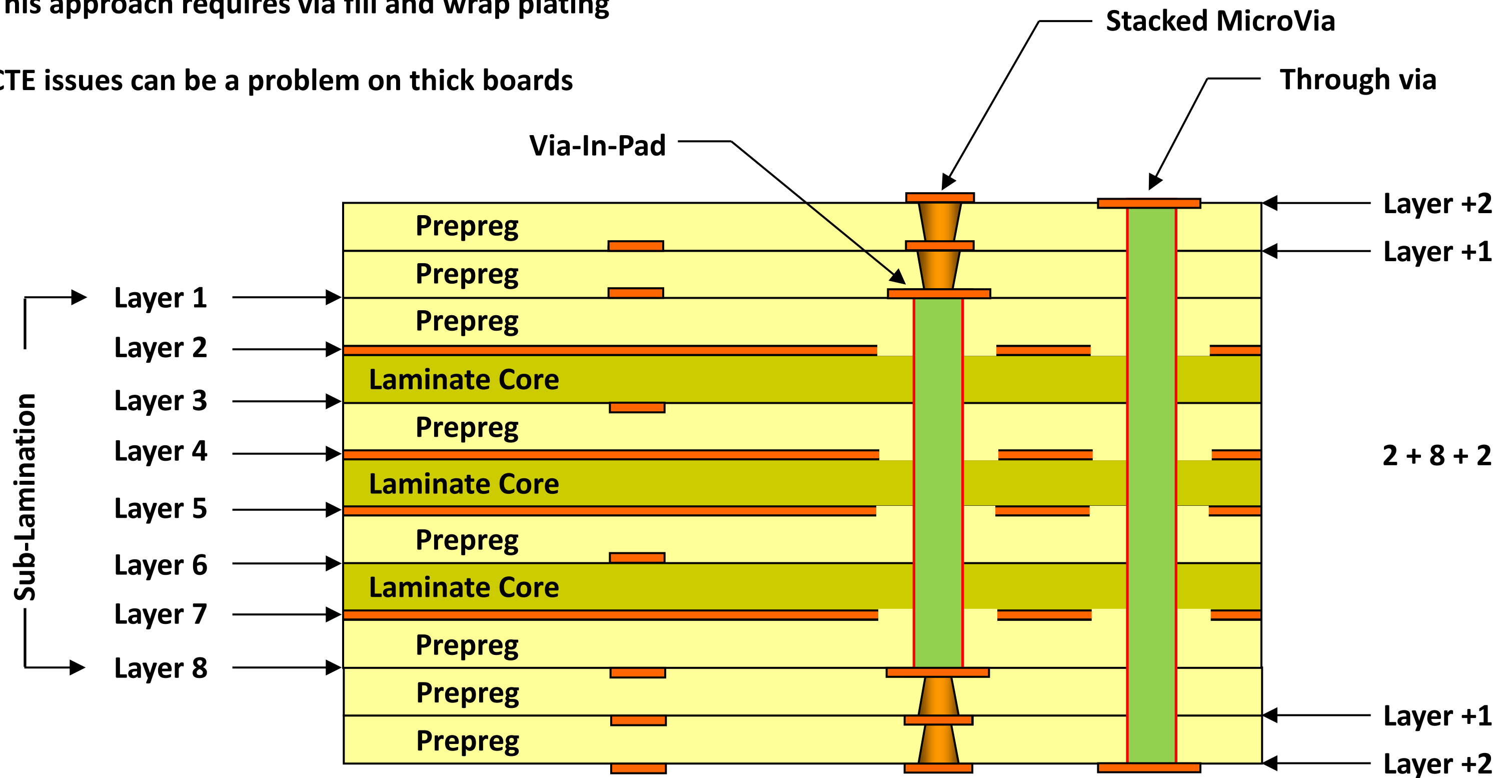
Microvia Sub-Lamination Interface: Stacked On Sub-Via

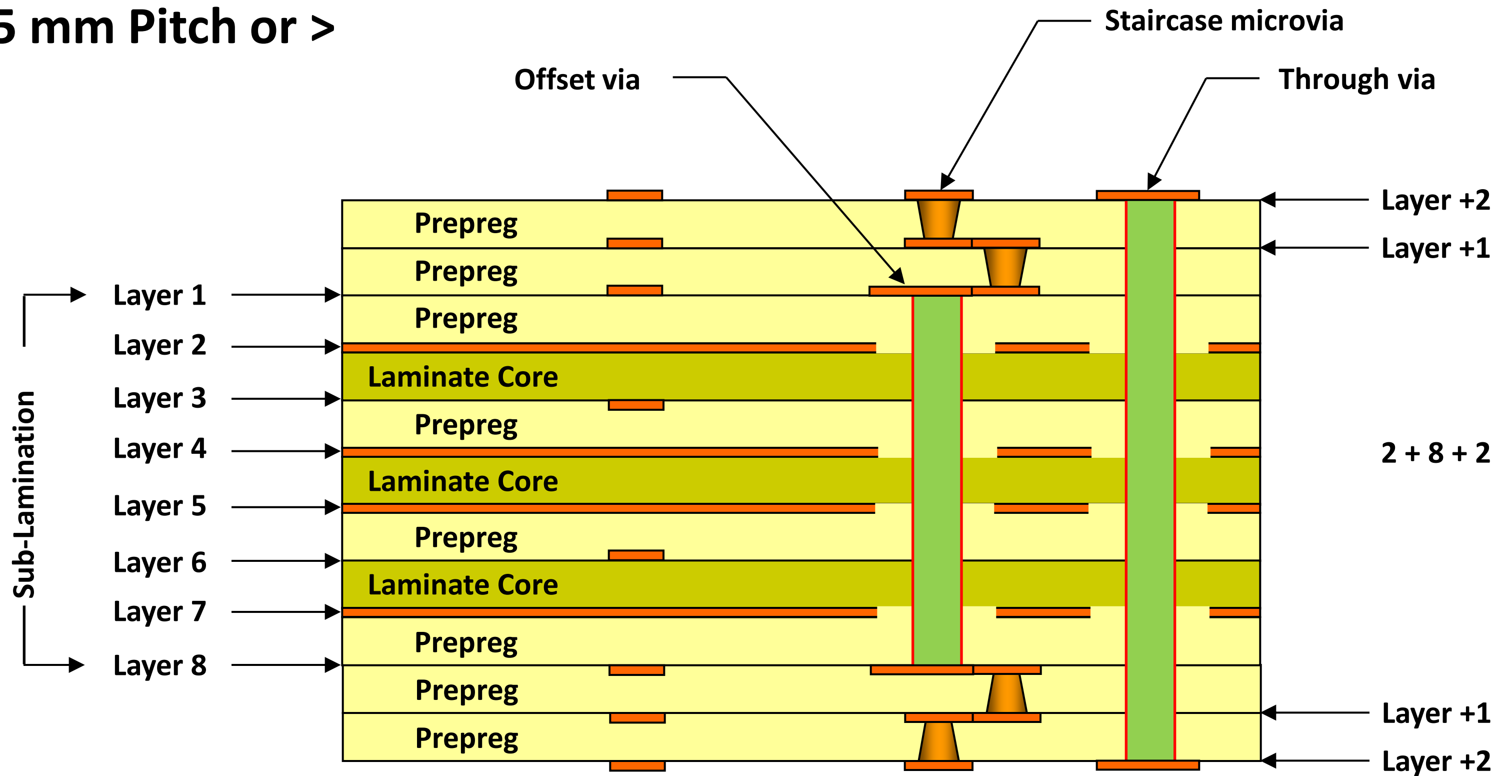
- This approach requires via fill and wrap plating
- CTE issues can be a problem on thick boards



Not Recommended on all designs: Contact engineering

Microvia Sub-Lamination Interface: Offset Via

0.5 mm Pitch or >



Preferred Construction

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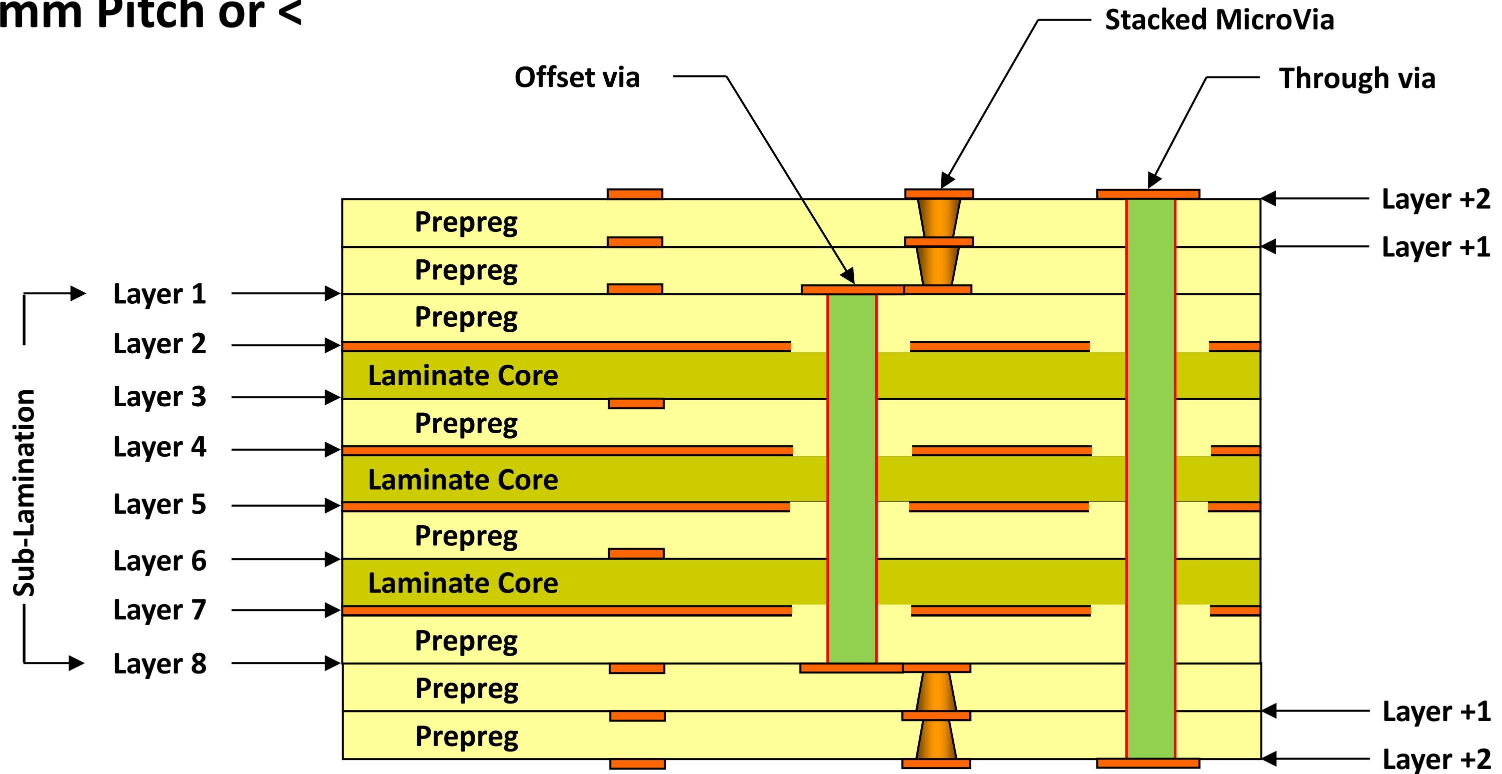
Microvia Sub-Lamination Interface: Offset Via Stacked

0.4 mm Pitch or <



Preferred Construction

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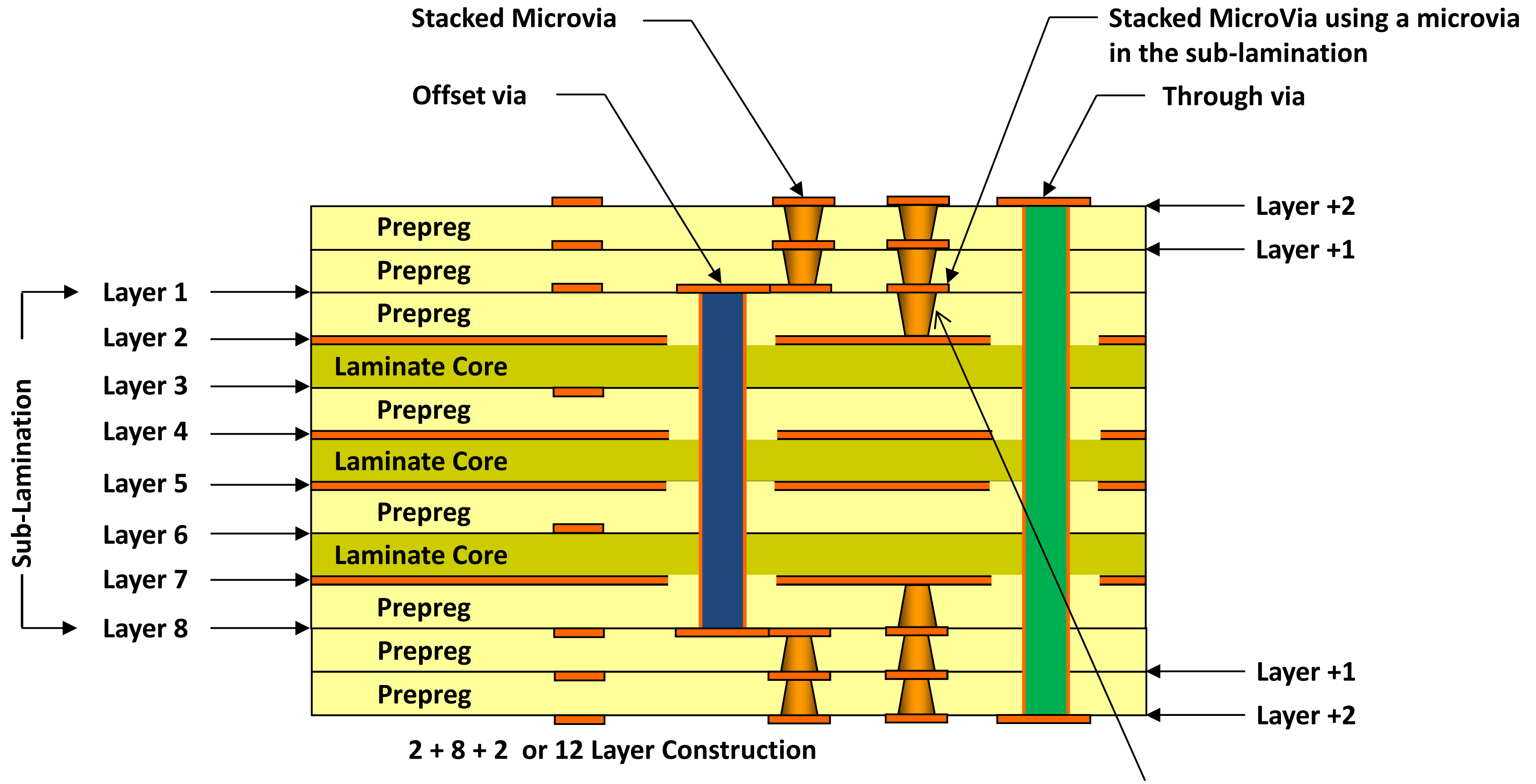
Microvia Sub-Lamination Interface: Sub-Lam Microvia



Preferred Construction with additional low cost Microvia to layer 4

TTM Technologies

Next Generation - *SMV™* Technology

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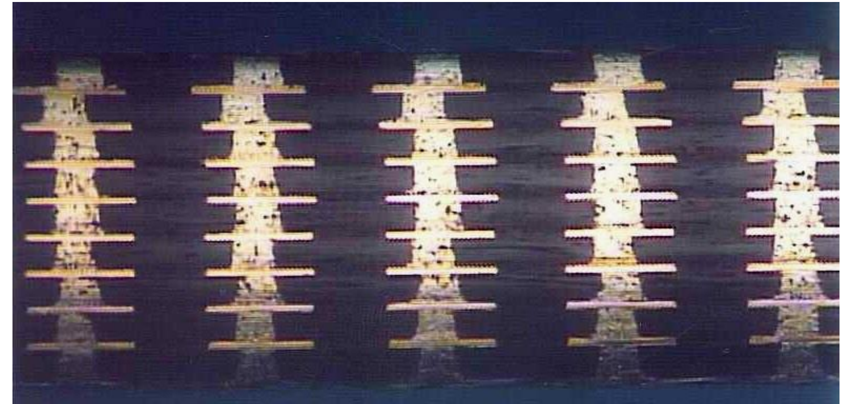
Next Generation - *SMV™* Technology

We're constantly working to enable new technologies to meet the needs of high-technology customer demands with small, feature-rich products (ex. mobile phones, PDA, cameras, and other such products).



- ***NextGen - SMV™*** Technology:
  - Requires one to two lamination cycle (based on design constraint), reducing fabrication time
  - Eliminates plating cycle of inner layers
  - Improves inner layer characteristics, signal integrity and electrical characteristics
  - Reduces demand on plating and lamination, improving facility capacity utilization
  - Allows for thinner finished product
  - Initial customer builds have been encouraging with significant early interest
  - This is a Viasystems patented technology

NextGen Technology

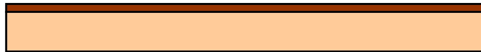
Examples of three concepts that have been developed

- *NextGen-SMV®* is a full build-up technology that is a single lamination parallel process (SLPP™) with conductive paste joints in the z-axis, provides Z-axis connectivity from, and to any layer
- HDI-Link™ is focused towards minimizing lamination cycles on designs such as 3+N+3 or 4+N+4 or …where 'N' is a conventional buried via and 3+ or 4+ build-up cores utilize *NextGen-SMV* technology to make the connection in the Z-axis with conductive paste
- Sub-Link™ is solution for high aspect ratio PCB's (> 40:1) where we build sub-section of a PCB and connect the subs with conductive paste in the Z-axis

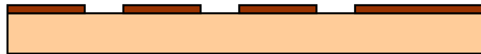
NextGen-SMV™ Mass Terminated Microvia

We continue to drive technology enhancements in the ***SMV™*** arena:

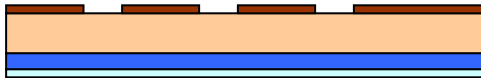
– Requires one to two lamination cycle (based on design constraint), reducing fabrication time
– Eliminates plating cycle of inner layers
– Improves inner layer characteristics, signal integrity and electrical characteristics
– Reduces demand on plating and lamination, improving facility capacity utilization
– Allows for thinner finished product



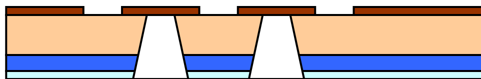
Step 1. Single sided core



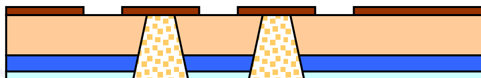
Step 2. Single sided etched core



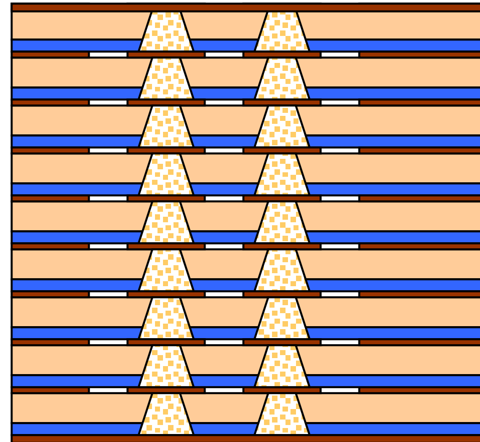
Step 3. Adhesive and single sided etched core

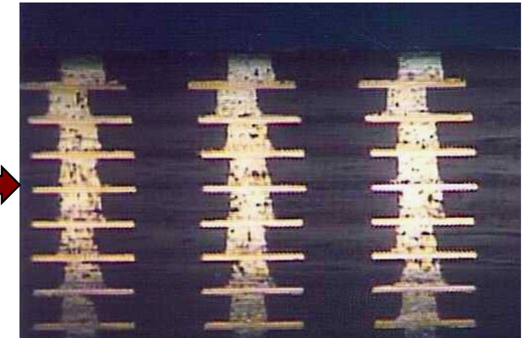


Step 4. Laser drilled micro vias



Step 5. Filled micro vias





Step 6. After single lamination

Laminate

Protective film

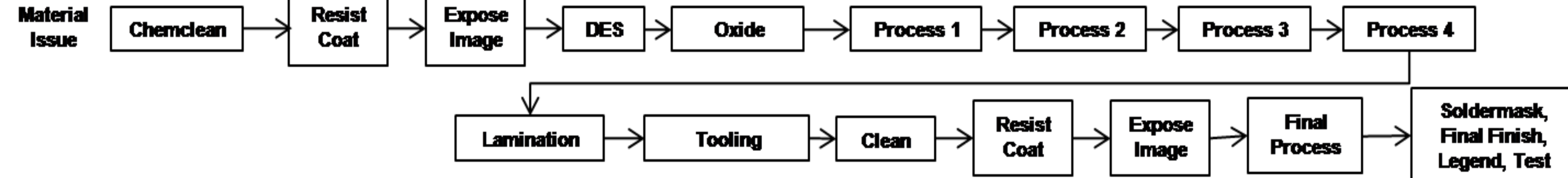
Metallic paste filler

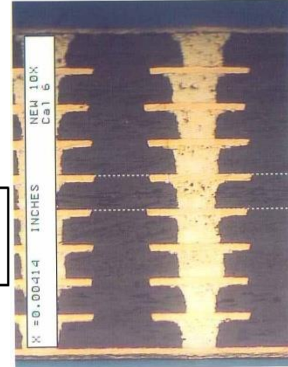
Copper foil

Film adhesive

Single Lam vs. Sequential Build-up Process Comparison of 10L PCB

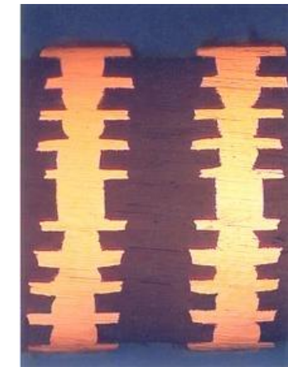
Single Lamination Parallel Process
Stacked MicroVia





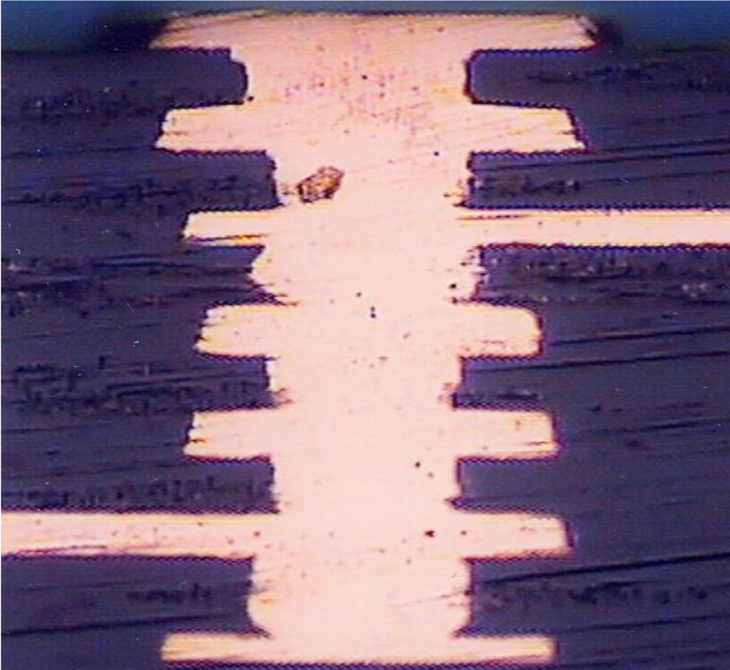
Industry Standard - Sequential Lamination
Stacked MicroVia

Material Issue
Tooling
Process A
Clean
Metallization
Resist Coat
Expose Image
Develop
Oxide
Layup and Lamination
Soldermask, Final Finish, Legend, Test
Print Image
Develop
Process D
Resist Strip
Clean
Metallization
Resist Coat
Process D
Process D
Resist Strip
Etch
Clean
Repeat for sub 4 to 7
Repeat for sub 3 to 6
Repeat for sub 2 to 8
Repeat for final 1 to 10

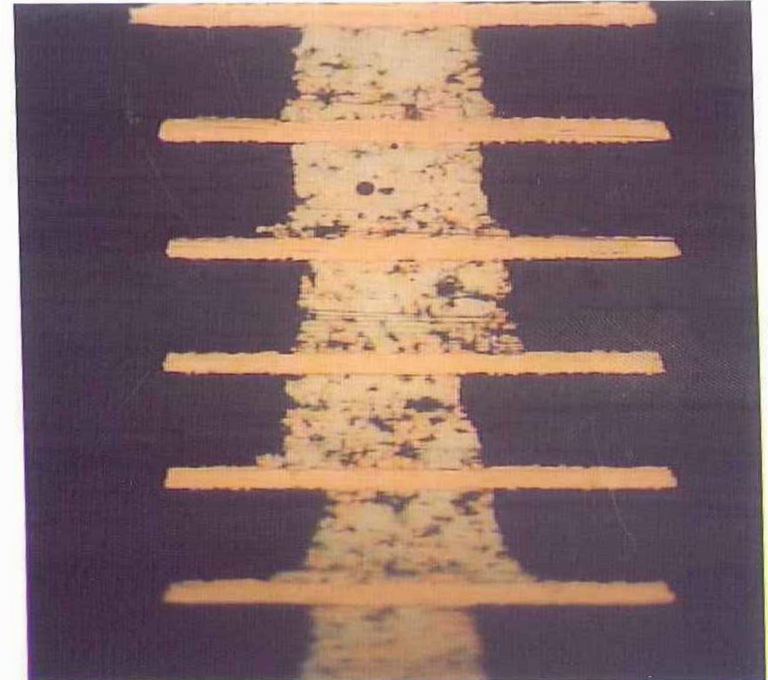


Copper vs. Conductive Paste

SMV – Solid Copper Plate

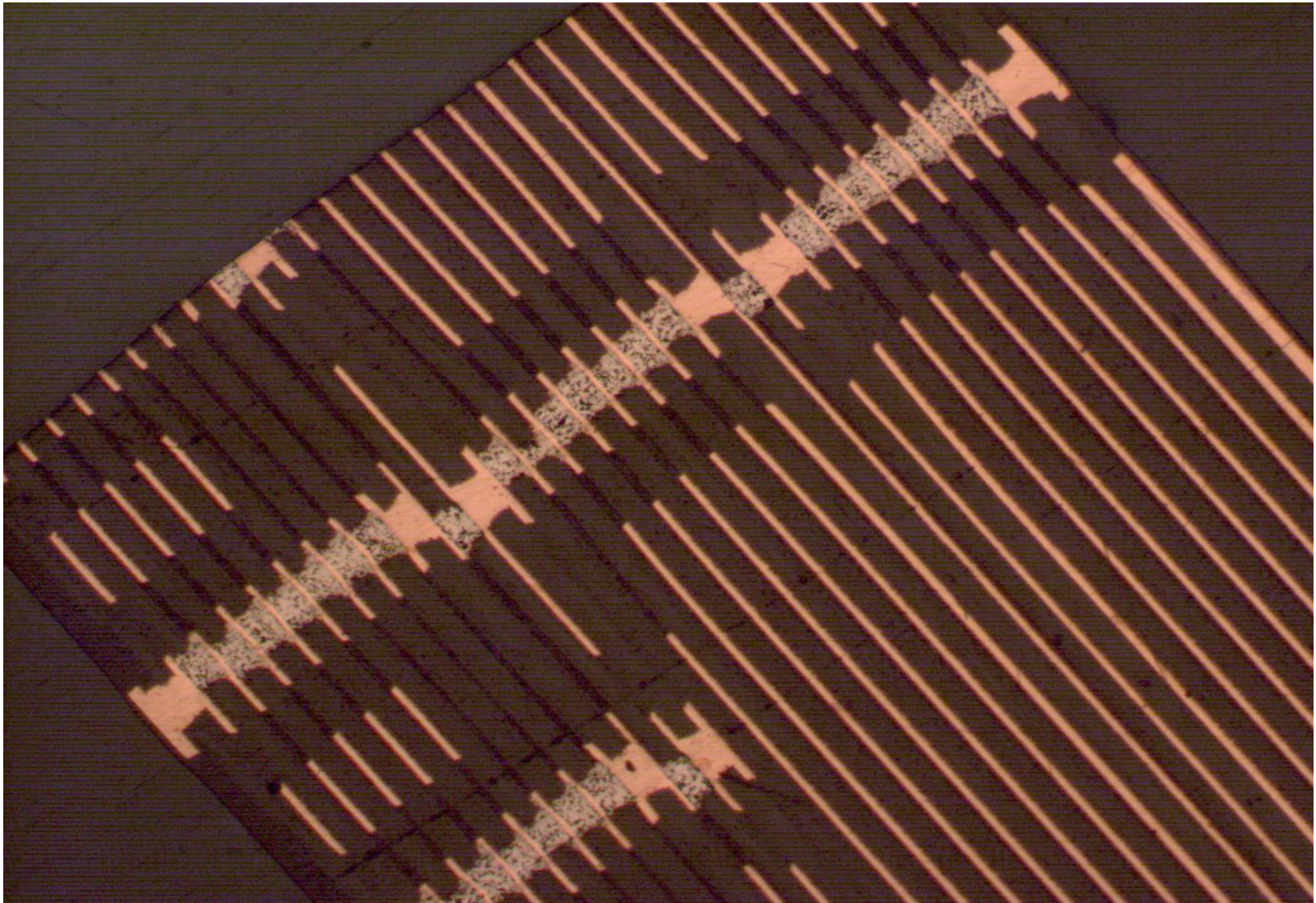


NextGen-SMV® - Conductive Paste



- Inner layers are plated vs. print and etch = contrasting thickness of copper
- Differing thermal conductivity; Copper (385 W/mK) vs. Paste (25 to 40 W/mK)
- Bulk Resistivity; Copper (1.7 micro ohm cm vs. 50 micro ohm cm)

NextGen capability
30 layer any layer via connectivity

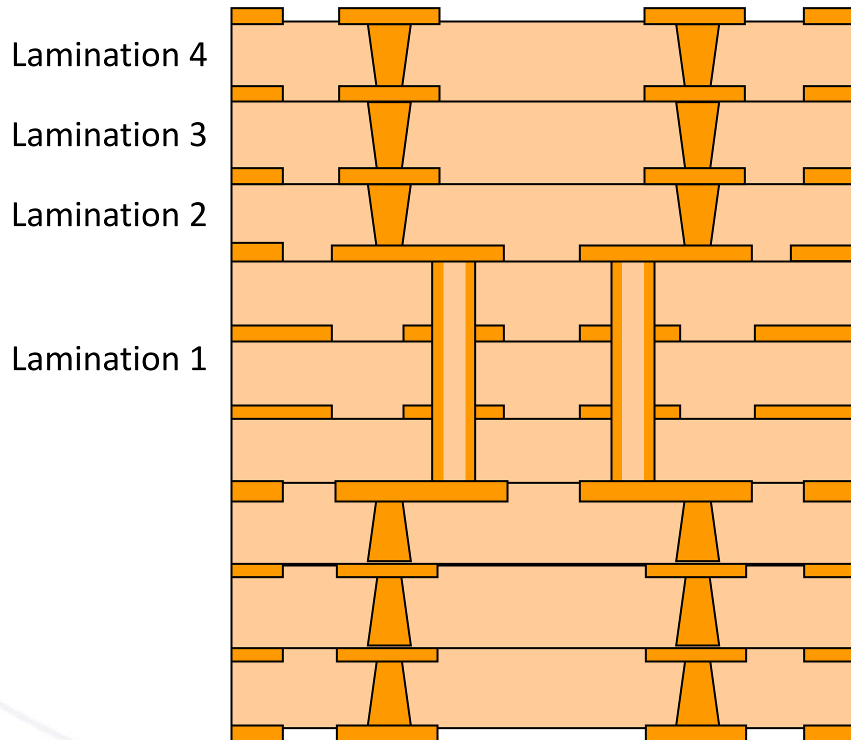


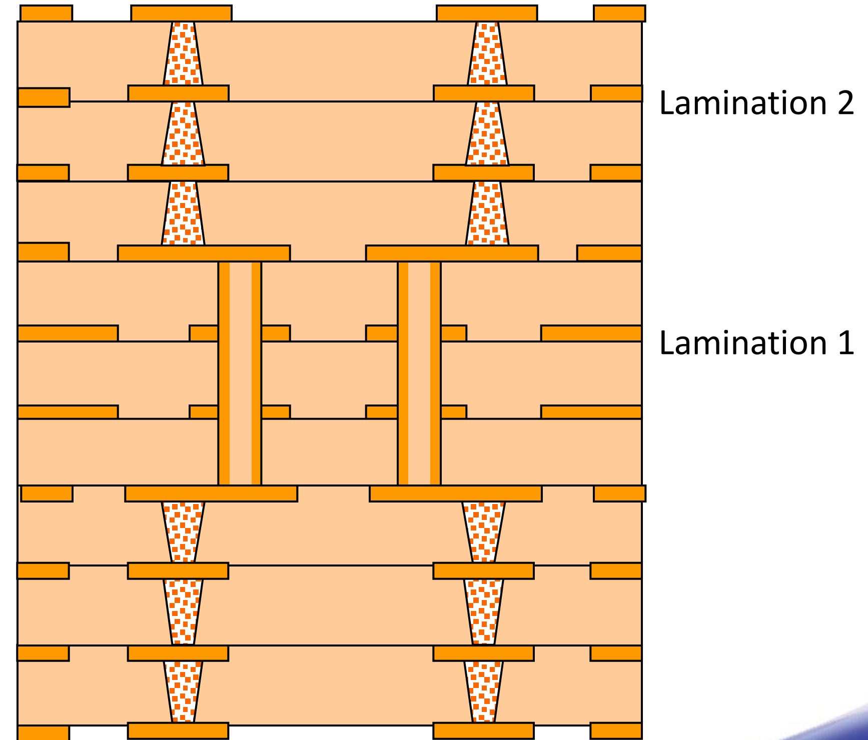
DDi Patent

Guidelines for single shot lamination
8 to 12 layer PCB

Single lamination full build-up PCB			
	Standard	Advanced	Future
Lead Time	**7 days**	**5 days**	**3 days**
Layer Count	**up to 10**	**12 to 14**	**up to 18**
Dielectric Thickness	**0.081mm**	**0.081 & 0.094mm**	**0.069 & 0.107mm**
Via Diameter	**0.152mm**	**0.127 & 0.152mm**	**0.1mm**
Pad Diameter	**0.279mm**	**0.25 & 0.279mm**	**0.23mm**
Board Thickness	**1.0mm**	**1.2 & 1.32mm**	**1.55 & 2.0mm**
Impedance	**10 %**	**8 %**	**5 %**
Copper Weight	**18 µm**	**18 µm**	**12 to 18 µm**
Material Type	**High Temp FR4, Halogen Free**	**Low Loss Epoxy, BT, Halogen Free**	**High Speed**

DDi HDI-Link™, Sub-to-core attach





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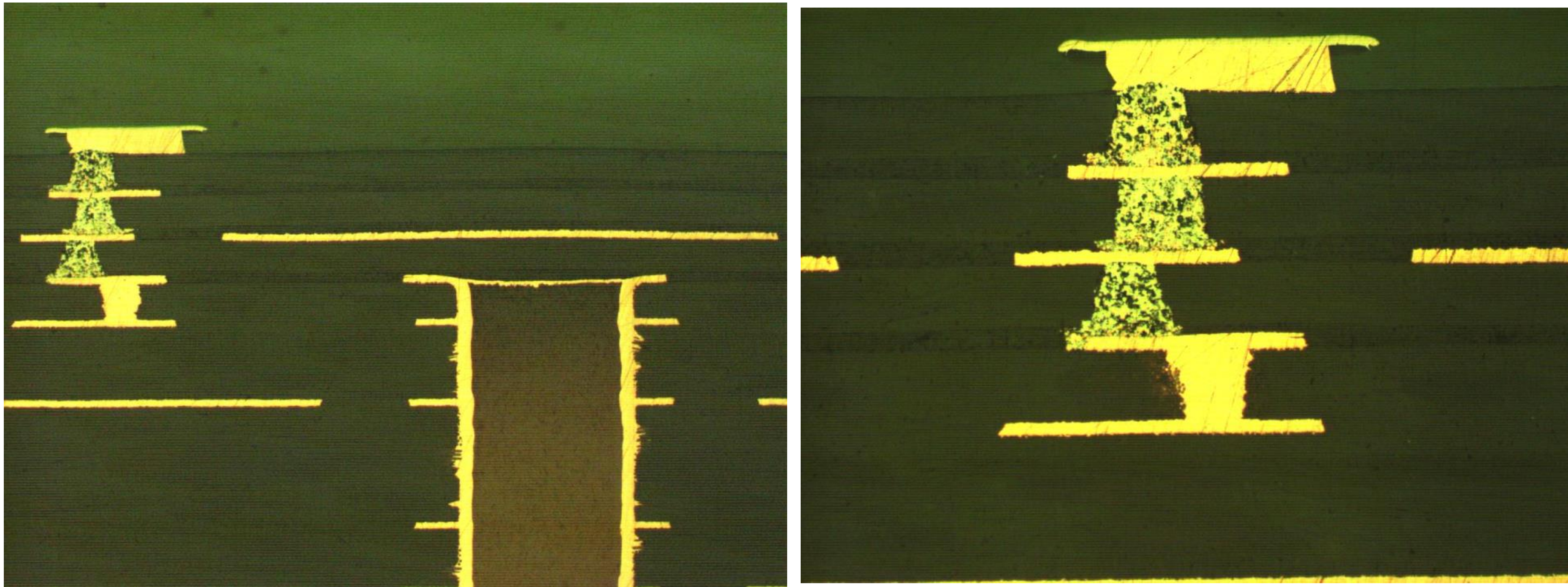
Example of HDI-Link™
20 layer PCB with 3+N+3 construction

Sub-to-Core Attach



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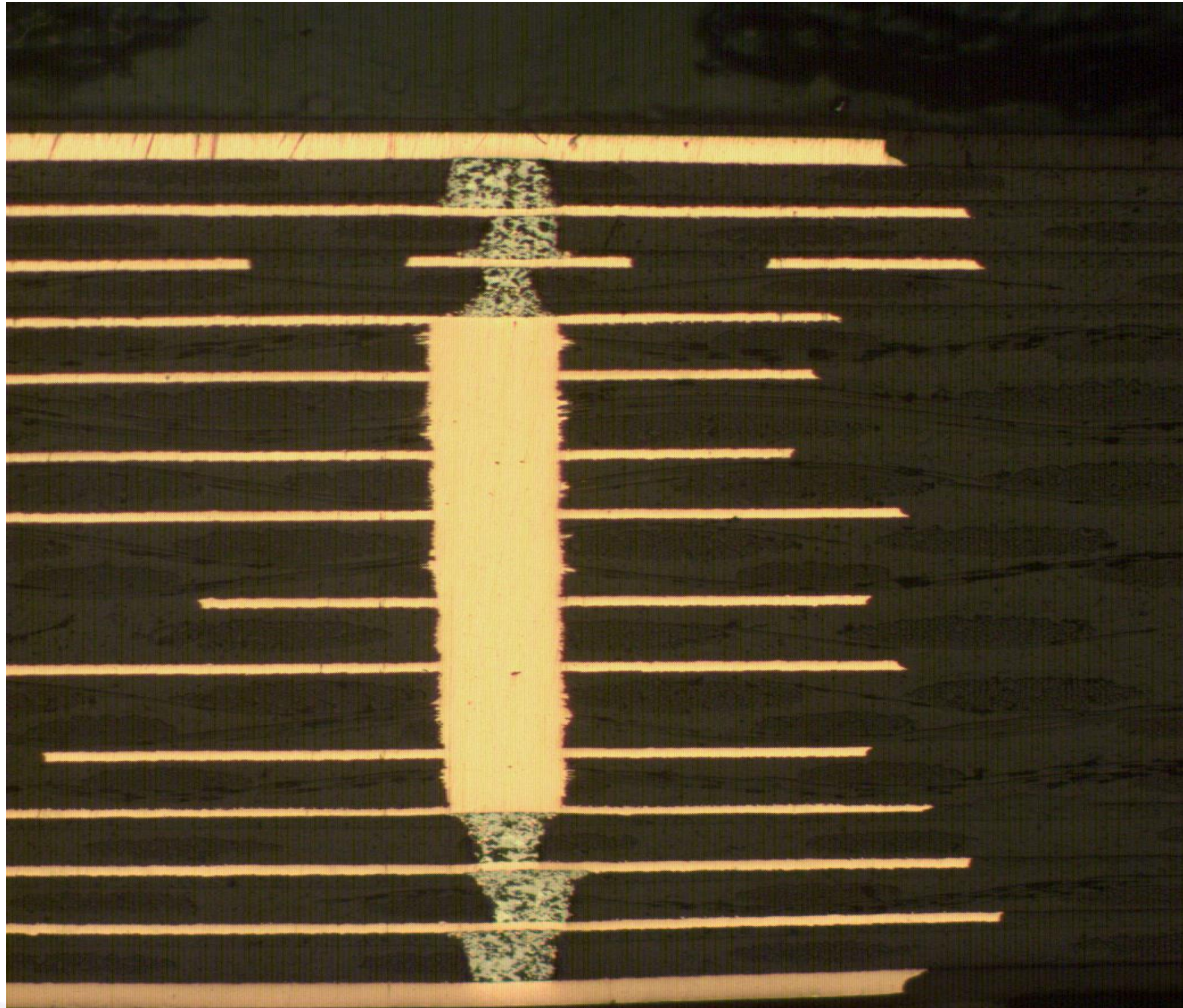
Example of HDI-Link™ 14 layer PCB

3+N+3 (buried via = solid copper plate)



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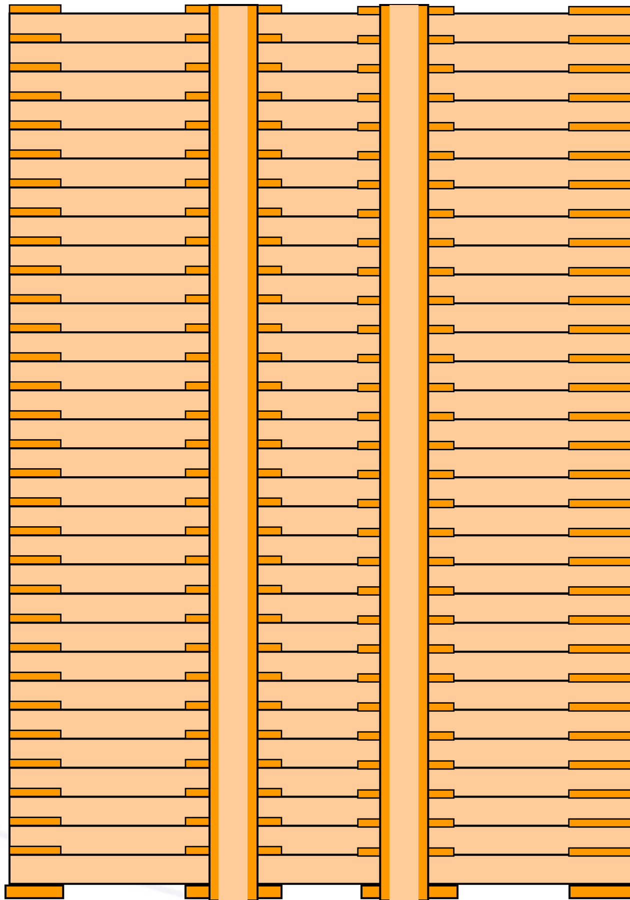
2 lamination cycle PCB build
Conventional buried via (N) + NextGen layers

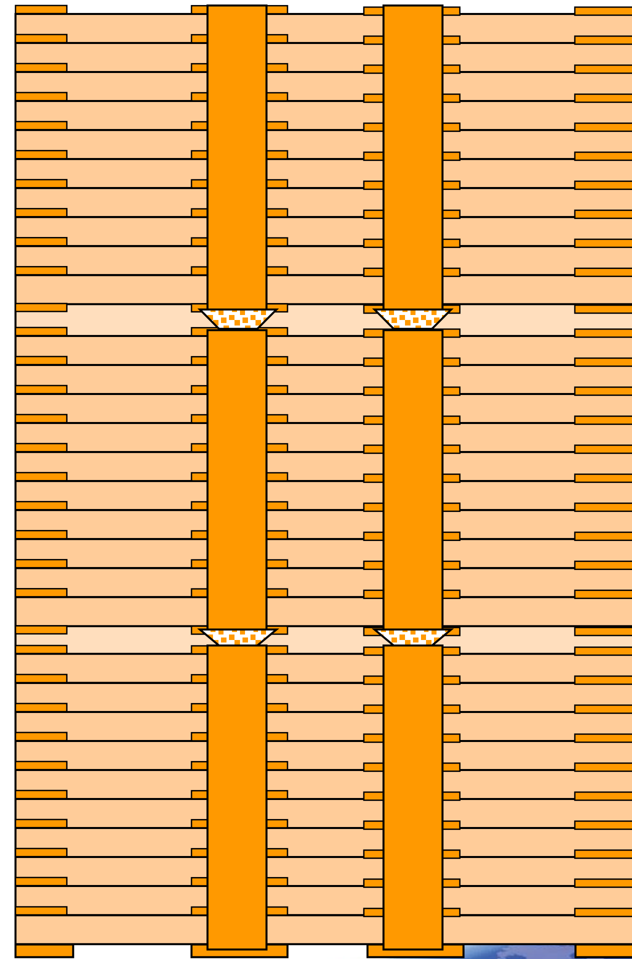
2 lamination cycle build; conventional buried via + NextGen layers			
	Standard	Advanced	Future
Lead Time	**10 days**	**7 days**	**5 days**
Layer Count	**3+N+3**	**4+N+4**	**5+N+5**
Dielectric Thickness	**0.081**	**0.081 & 0.094mm**	**0.069 & 0.107mm**
Via Diameter	**0.152mm**	**0.127 & 0.152mm**	**0.1mm**
Pad Diameter	**0.279mm**	**0.25 & 0.279mm**	**0.23mm**
Board Thickness	**1.5mm**	**3.0mm**	**5.0mm**
Impedance	**10 %**	**8 %**	**5 %**
Copper Weight	**18 µm**	**18 µm**	**12 & 18 µm**
Material Type	**High Temp FR4, Halogen Free**	**Low Loss Epoxy, BT, Halogen Free**	**High Speed**

DDi Sub-Link™, Sub-to-Sub Attach

Conventional High Aspect Ratio PCB
30 + Layers Build PCB



DDi Sub-Link™ High Aspect Ratio PCB
30 + Layers

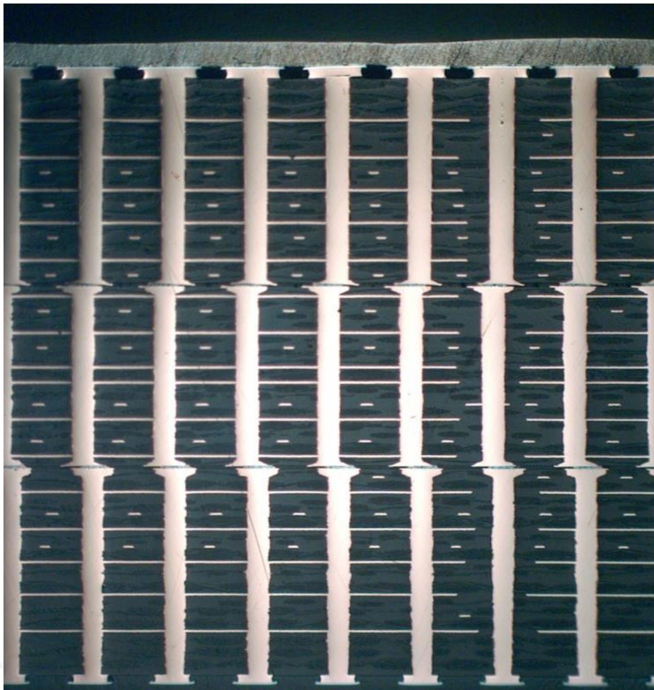


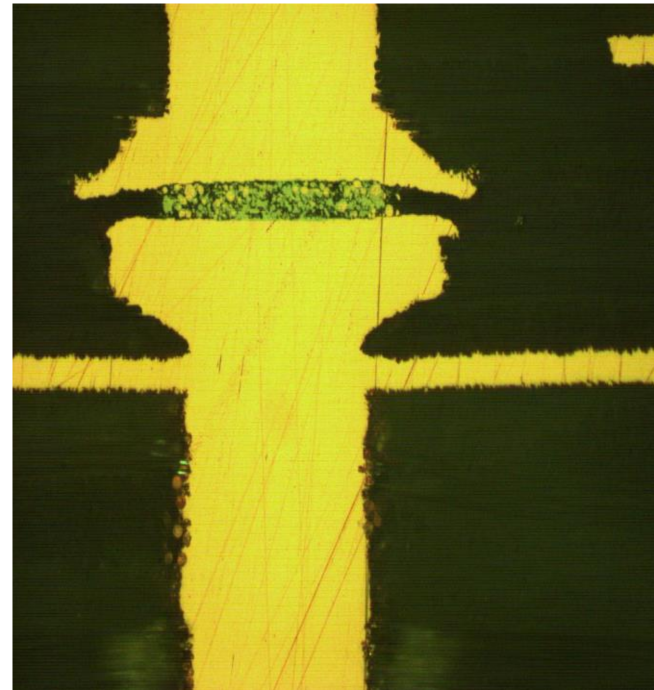
TTM Technologies

DDi Sub-Link™ - Solution for high aspect ratio PCBs
Example of 32 layer Load Board; 11+10+11

Sub-to-Sub Attach

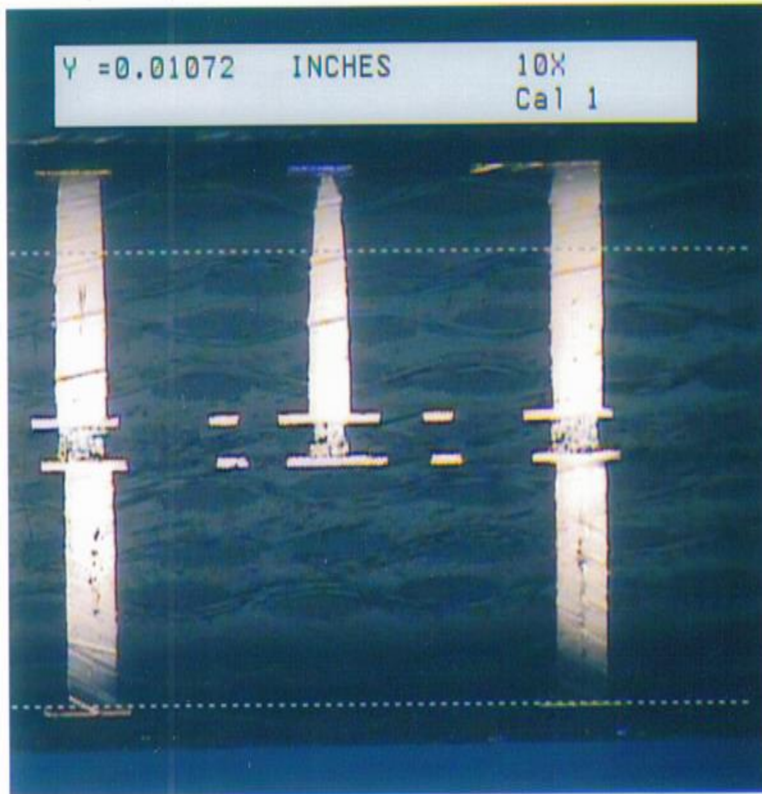
- Sub-Link™ (sub-to-sub attach)
  - Three subs (about 0.060” thick) were used as proof-of-concept
  - Developed a new concept for sub connectivity with conductive paste
  - Solid copper vias in subs with 0.006” mechanical drilled holes
  - PCB pass IPC standard electrical test requirement

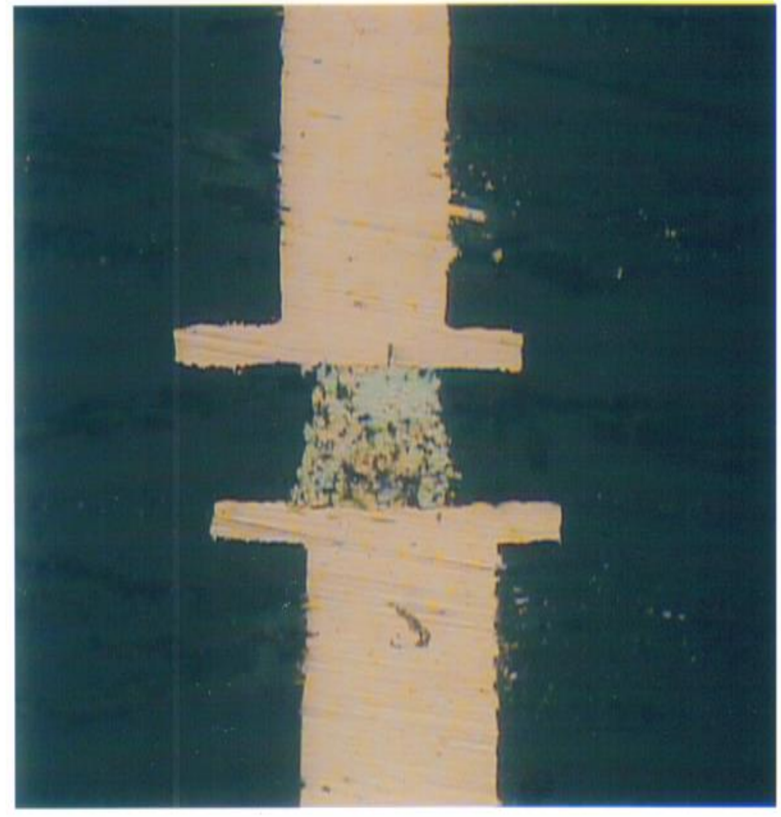




DDi Sub-Link, Sub-to-Sub Attach

Sub-Link - Sub-to-Sub Attach
Solution for High Aspect Ratio PCB





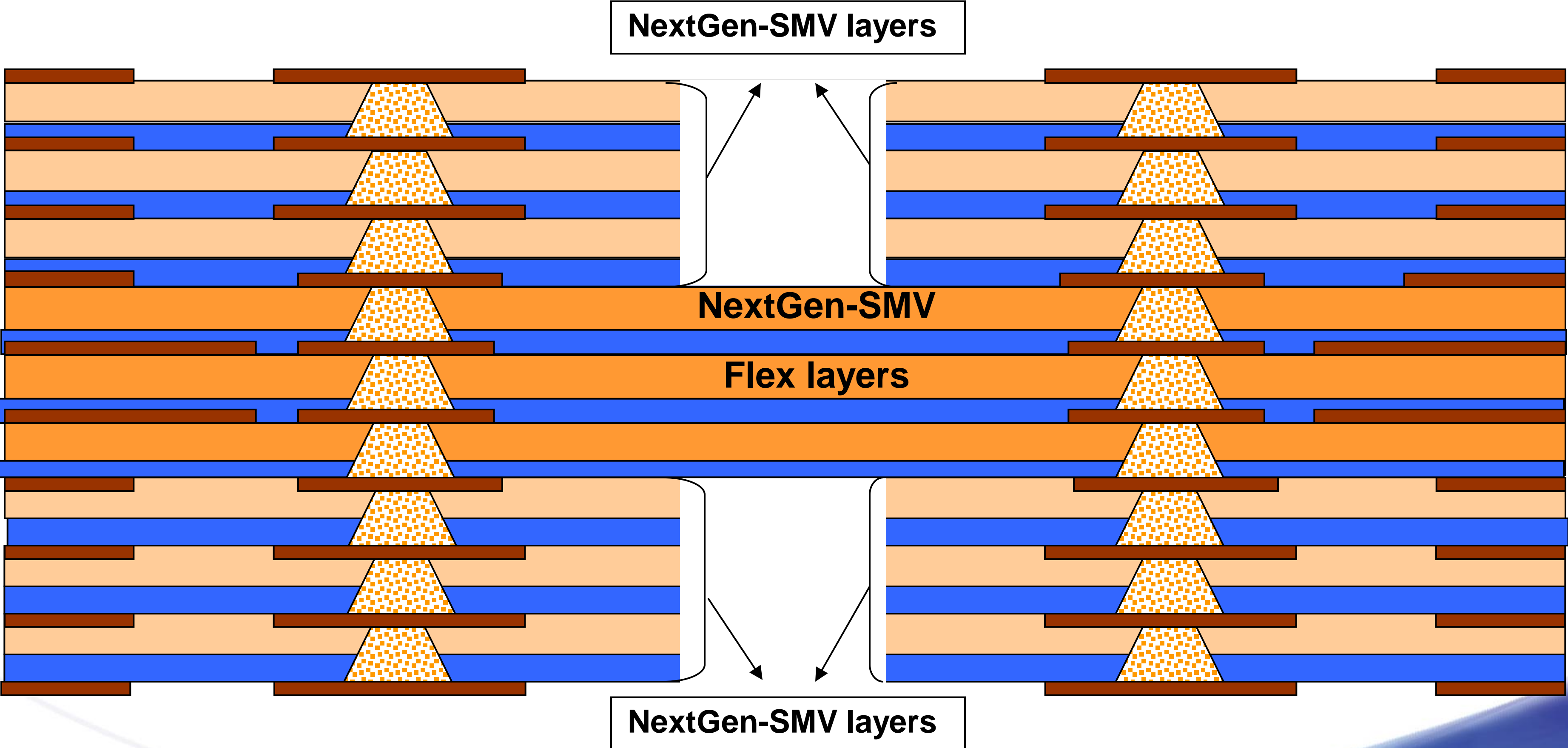
TTM Technologies

NextGen Sub-Link™ Design Guidelines

DDi Sub-Link™ BOARD CHARACTERISTICS			
	Standard	Advanced	Future
Lead Time	**15 days**	**12 days**	**7 days**
Layer Count	**3 Subs**	**4 Subs**	**5 Subs**
Dielectric Thickness	**Standard core and prepreg thickness**	**Standard core and prepreg thickness**	**Standard core and prepreg thickness**
Via Diameter	**0.152mm**	**0.127mm**	**0.1mm**
Pad Diameter	**0.279mm**	**0.25mm**	**0.23mm**
Board Thickness	**4.6mm**	**6.0mm**	**7.62mm**
Impedance	**10 %**	**8 %**	**5 %**
Aspect Ratio	**30:1**	**40:1**	**50:1**
Material Type	**High Temp FR4, Halogen Free**	**Low Loss Epoxy, BT, Halogen Free**	**High Speed**

NextGen Extension
Enable HDI in Rigid-Flex PCBs

Rigid-Flex PCB with DDi NextGen-SMV®
PPSL™ - Parallel Process Single lamination (all paste connectivity in the z-axis)



TTM Technologies

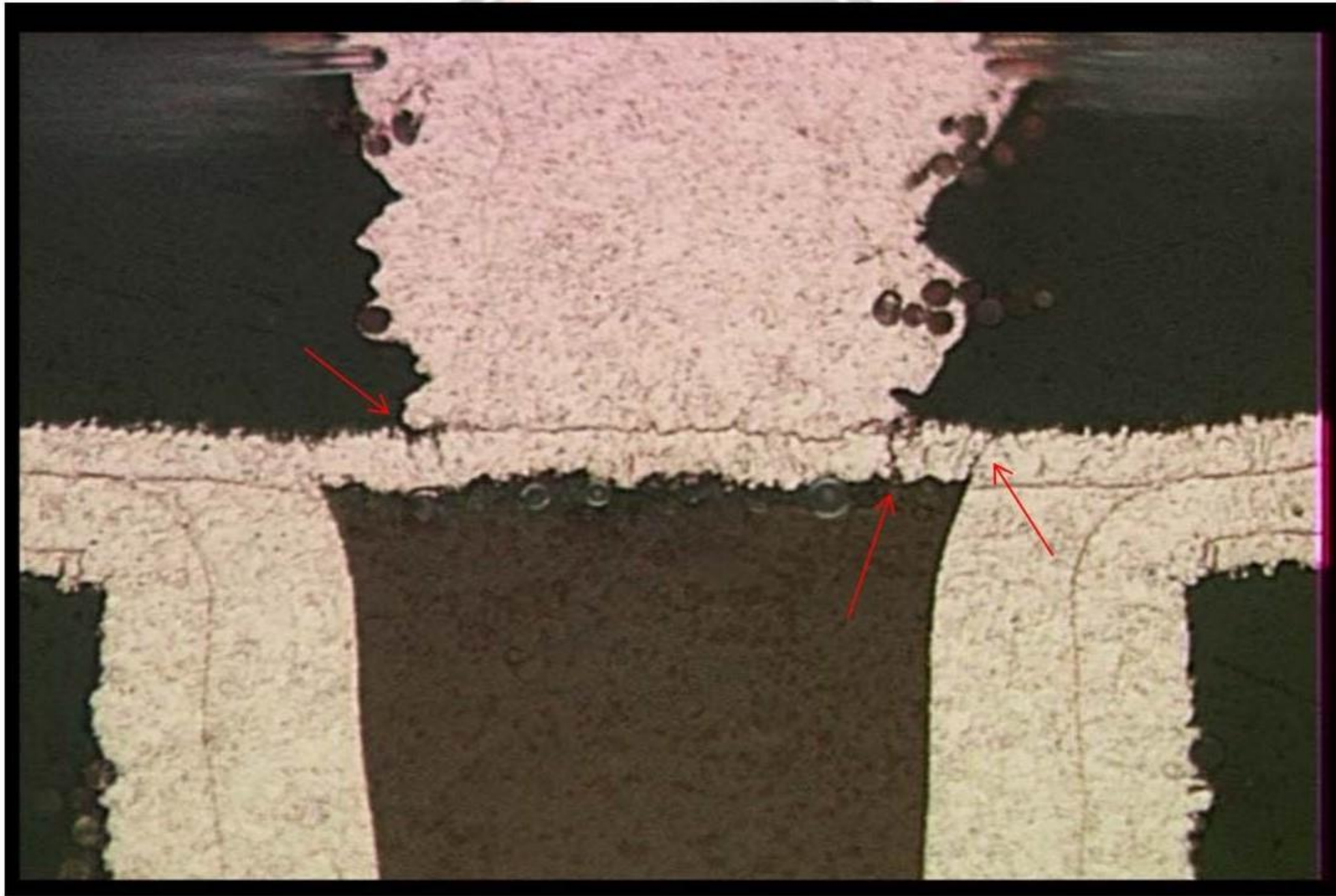
Microvia Sub-lamination Interface Techniques

Microvia: Sub-Lamination Interface

Basic design rules for Microvia build-up layers

- Build-up dielectric layers must be balanced on either side of the sub-lamination
- Build-up dielectric layers are generally 0.0025” (64µm) to 0.003” (75µm) thick
- The recommended total number of lamination cycles that any one part of the structure should experience is 3 and 4 – 5 for advanced structures
- Microvias stacked on buried mechanical vias should be avoided due to wrap plating requirements and excessive stress on thicker substrates
- Solid copper mechanically drilled vias can be used on thin sub-lamination cores in place of wrap plating

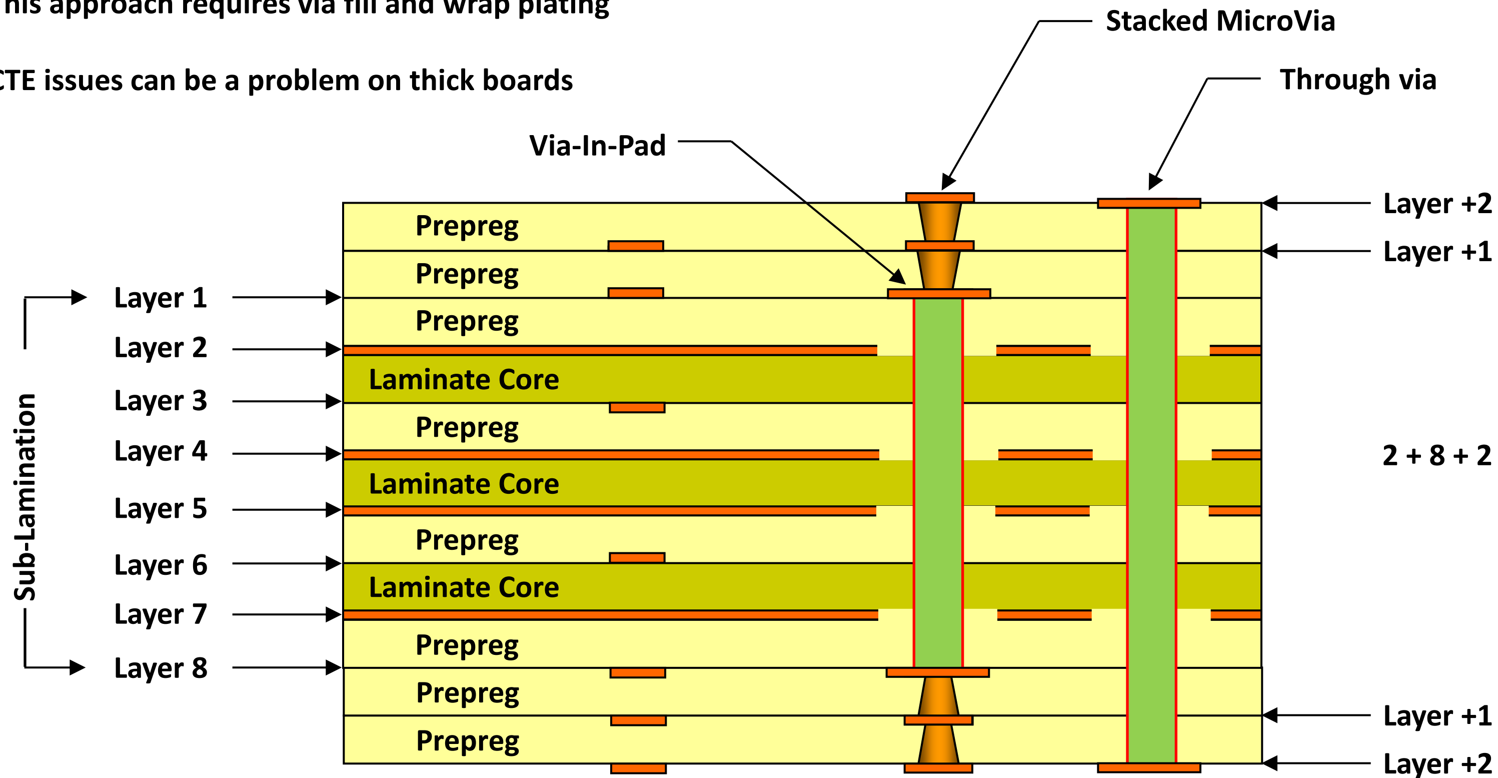
Microvia stacked on Epoxy-filled Mechanical Via – NO!



TTM Technologies

Microvia Sub-Lamination Interface: Stacked On Sub-Via

- This approach requires via fill and wrap plating
- CTE issues can be a problem on thick boards

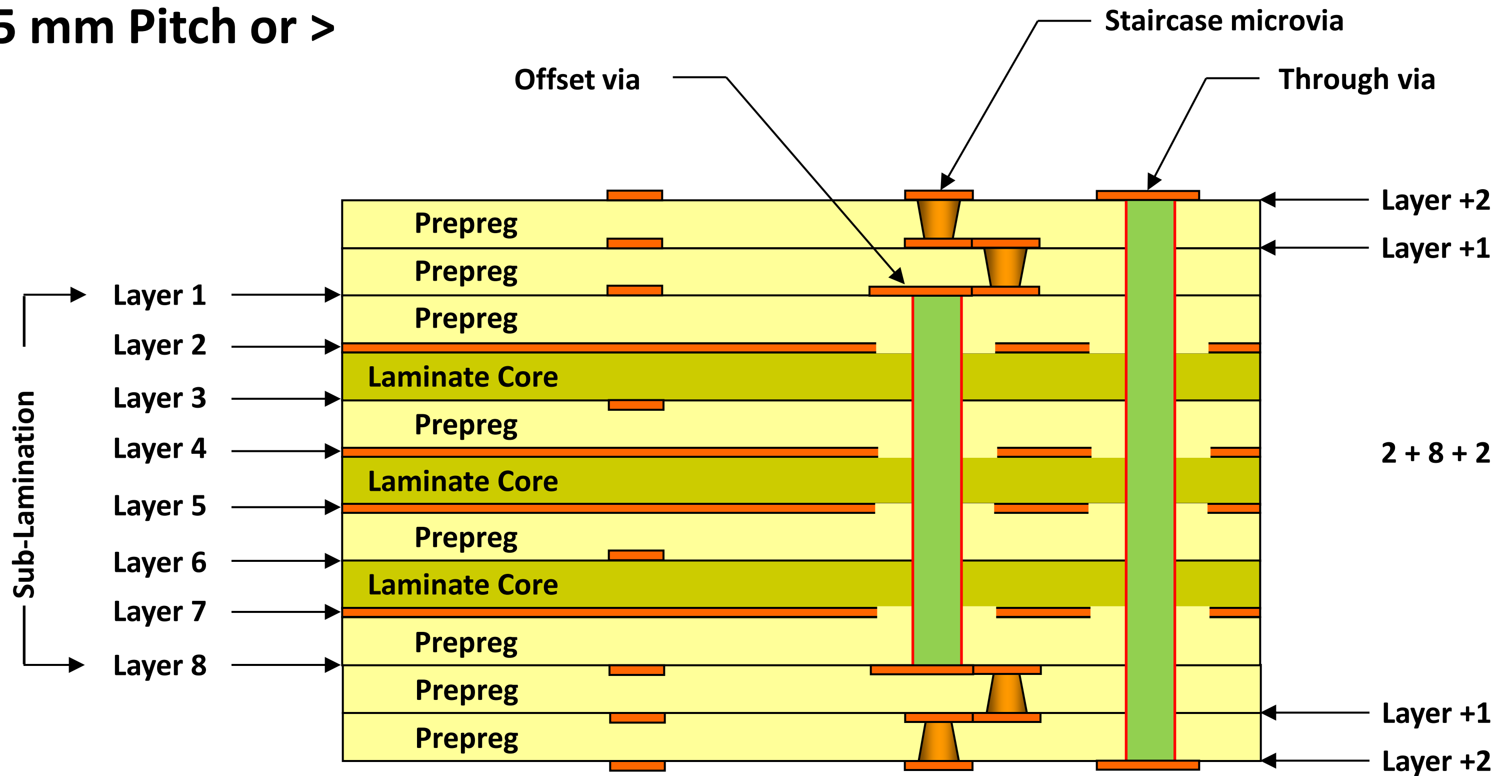


Not Recommended on all designs: Contact engineering

TTM Technologies

Microvia Sub-Lamination Interface: Offset Via

0.5 mm Pitch or >



Preferred Construction

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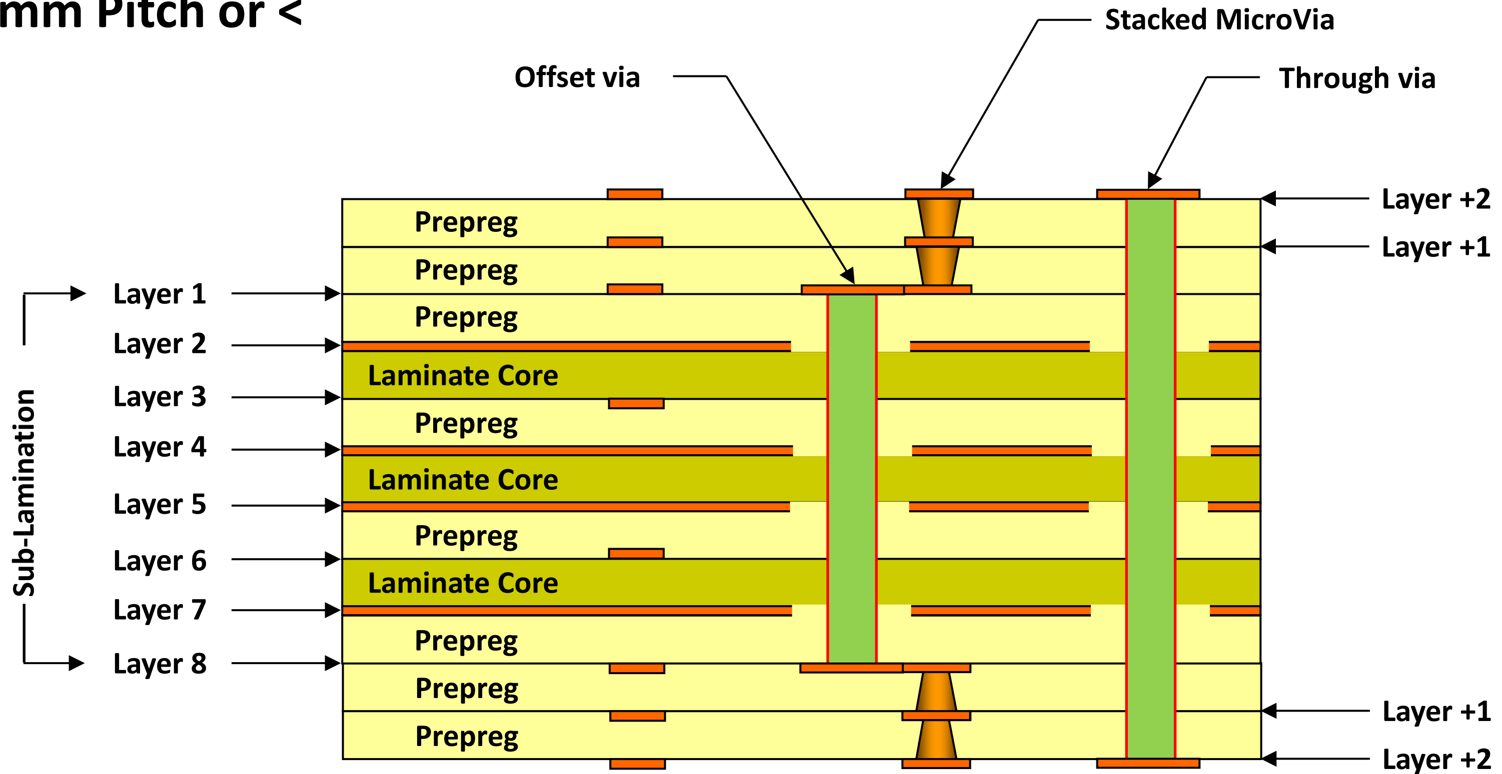
Microvia Sub-Lamination Interface: Offset Via Stacked



Preferred Construction

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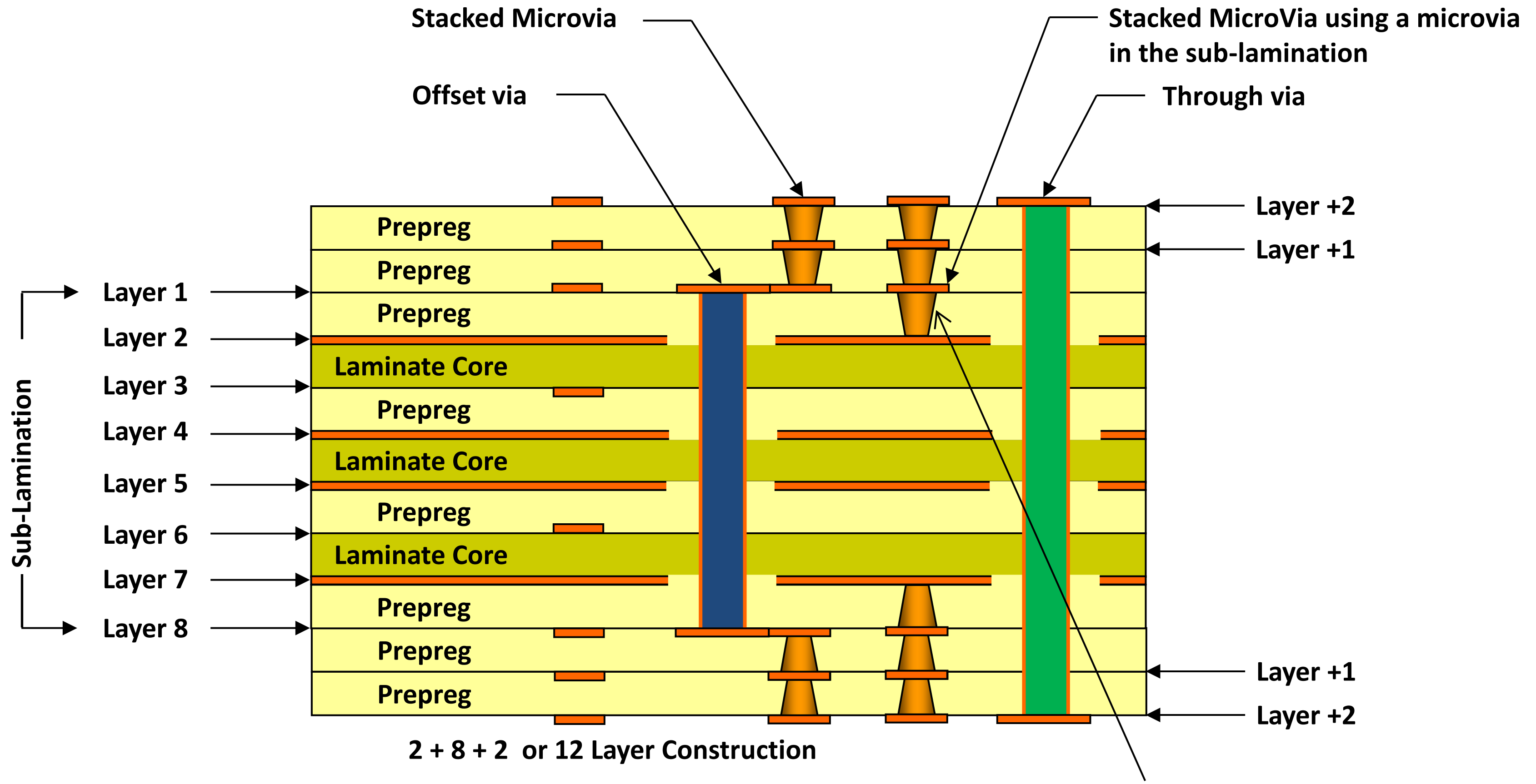
Microvia Sub-Lamination Interface: Sub-Lam Microvia



Preferred Construction with additional low cost Microvia to layer 4

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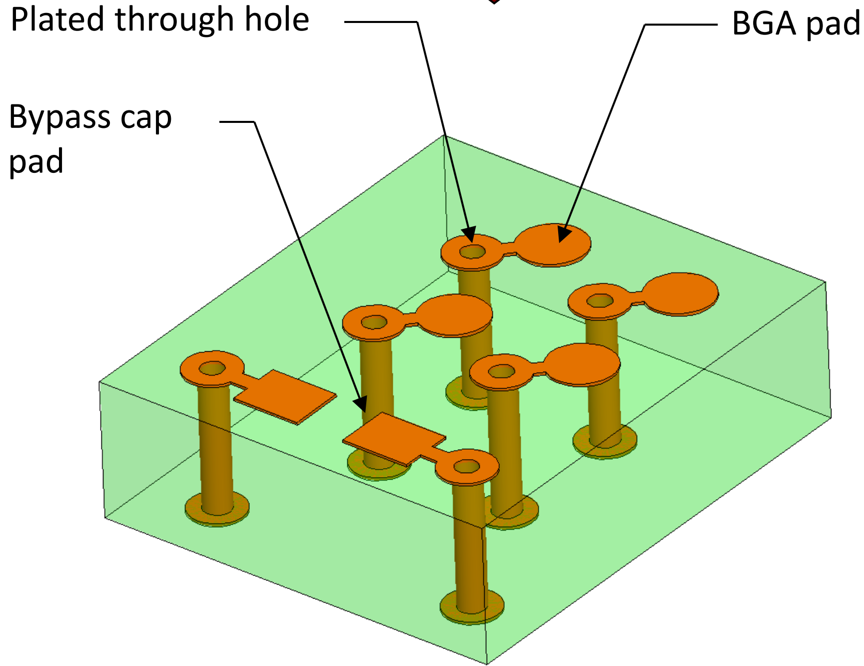
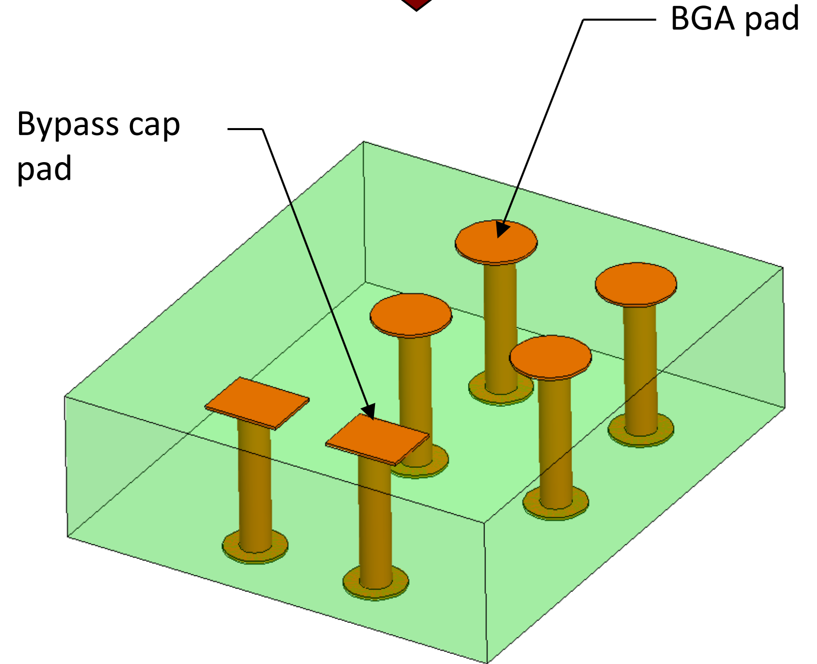
Via-in-Pad, Wrap Plate, & *FLAT-WRAP™*

Standard Construction vs. Via-In-Pad circuit Construction





By using either conductive or non-conductive fillers and over plating with copper, through hole vias can be placed in component pads with no impact on the soldering process

IPC 6012C Specification For Wrap Plating Thickness

Table 3-3 Surface and Hole Copper Plating Minimum Requirements for Buried Vias ≥ 2 Layers, Through-Holes and Blind Vias[1]

	Class 1	Class 2	Class 3
Copper - average[2,4]	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
Thin areas[4]	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Wrap[3]	AABUS	5 µm [197 µin]	12 µm [472 µin]

Note 1. Does not apply to microvias. Microvias are vias that are ≤0.15 mm [0.006 in] in diameter and formed either through laser or mechanical drilling, wet/dry etching, photo imaging or conductive ink formation followed by a plating operation. Blind vias with aspect ratios less than 1:1 **shall** be treated as microvias for plating thickness requirements. See Table 3-4.

Note 2. Copper plating (1.3.4.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. Wrap copper plating for filled PTHs and vias **shall** be in accordance with 3.6.2.11.1.

Note 4. See 3.6.2.11.

Table 3-4 Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)[1]

	Class 1	Class 2	Class 3
Copper - average[2,4]	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
Thin areas[4]	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Wrap[3]	AABUS	5 µm [197 µin]	6 µm [236 µin]

Note 1. Microvias are vias that are ≤ 0.15 mm [0.006 in] in diameter and formed either through laser or mechanical drilling, wet/dry etching, photo imaging or conductive ink formation followed by a plating operation. The values given for blind and buried microvias are not applicable for stacked microvias. As of the publication of this specification, there is little known about this structure and the reliability results are not consistent with buried and blind microvias. Stacked microvias may also require different inspection criteria.

Note 2. Copper plating (1.3.4.2) thickness **shall** be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. Wrap copper plating for filled microvias **shall** be in accordance with 3.6.2.11.1.

Note 4. See 3.6.2.11.

IPC 6012C Specification For Wrap Plating Thickness

Table 3-5 Surface and Hole Copper Plating Minimum Requirements for Buried Via Cores (2 Layers)

	Class 1	Class 2	Class 3
Copper - average[1,3]	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
Thin areas[3]	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
Wrap[2]	AABUS	5 µm [197 µin]	7 µm [276 µin]

Note 1. Copper plating (1.3.4.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.
Note 2. Wrap copper plating for filled buried via cores **shall** be in accordance with 3.6.2.11.1.
Note 3. See 3.6.2.11.

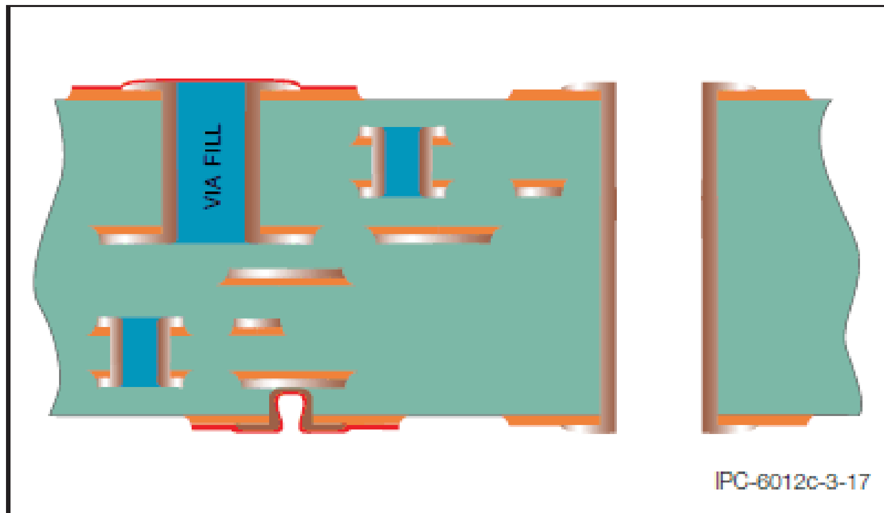


Figure 3-17 Wrap Copper in Type 4 Printed Board (Acceptable)

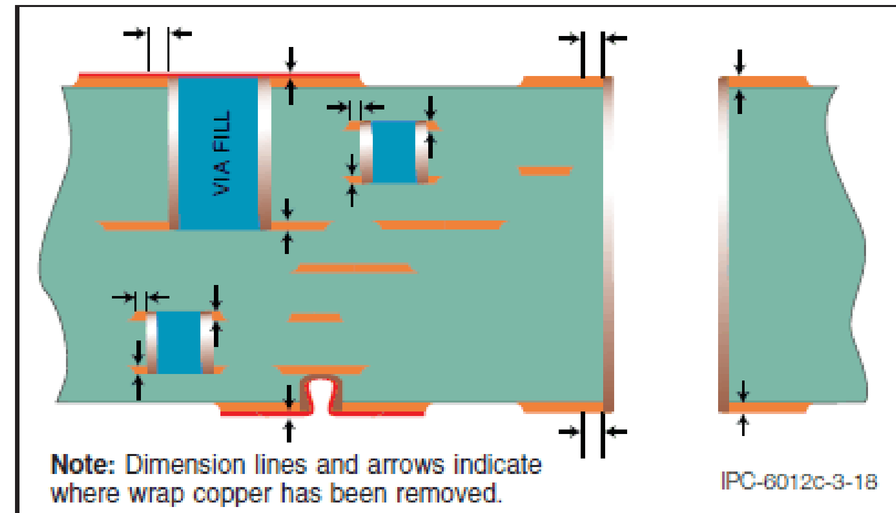


Figure 3-18 Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable)

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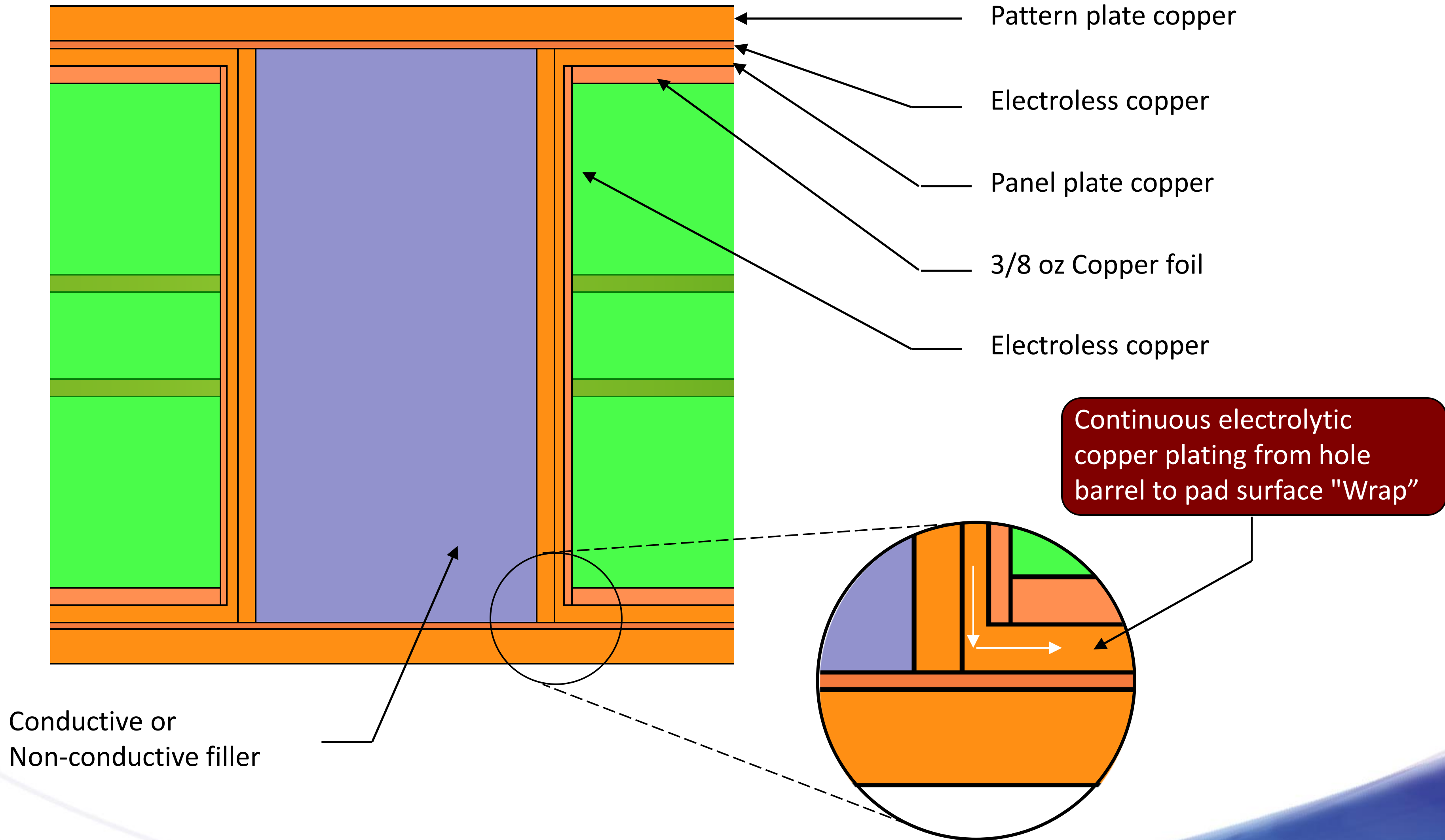
Filled Via With Wrap Plating



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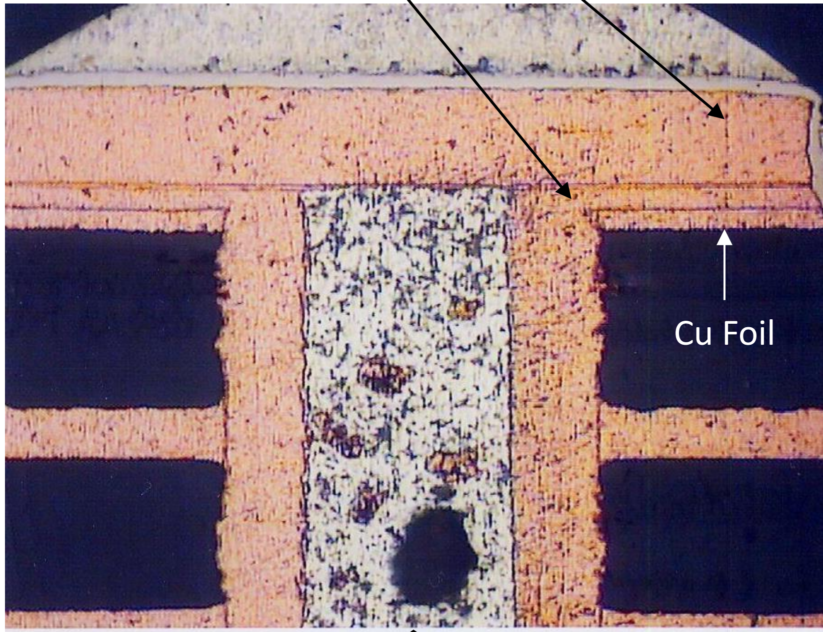
Filled Via With Wrap Plating (VIPPO)

Pattern plate

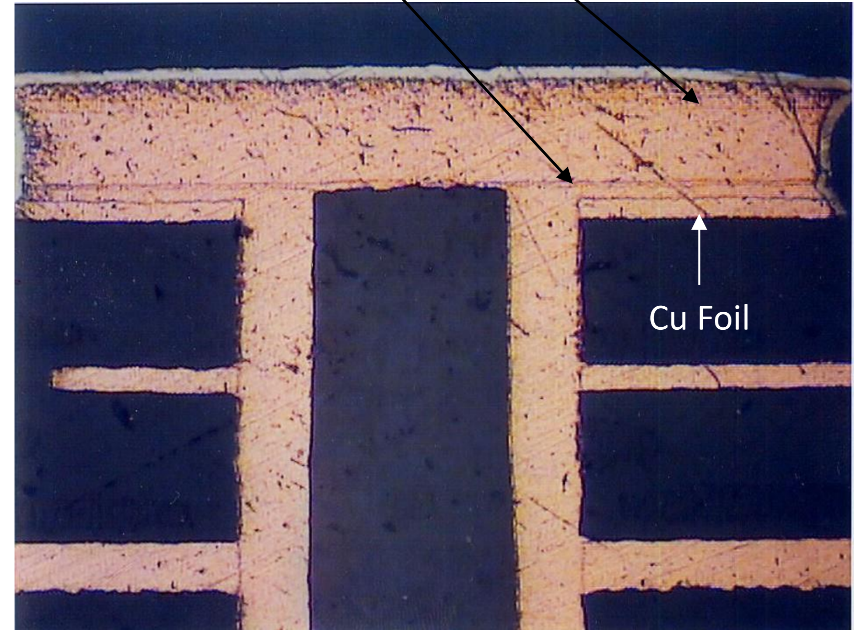
Wrap plate



Conductive Via fill

Pattern plate

Wrap plate

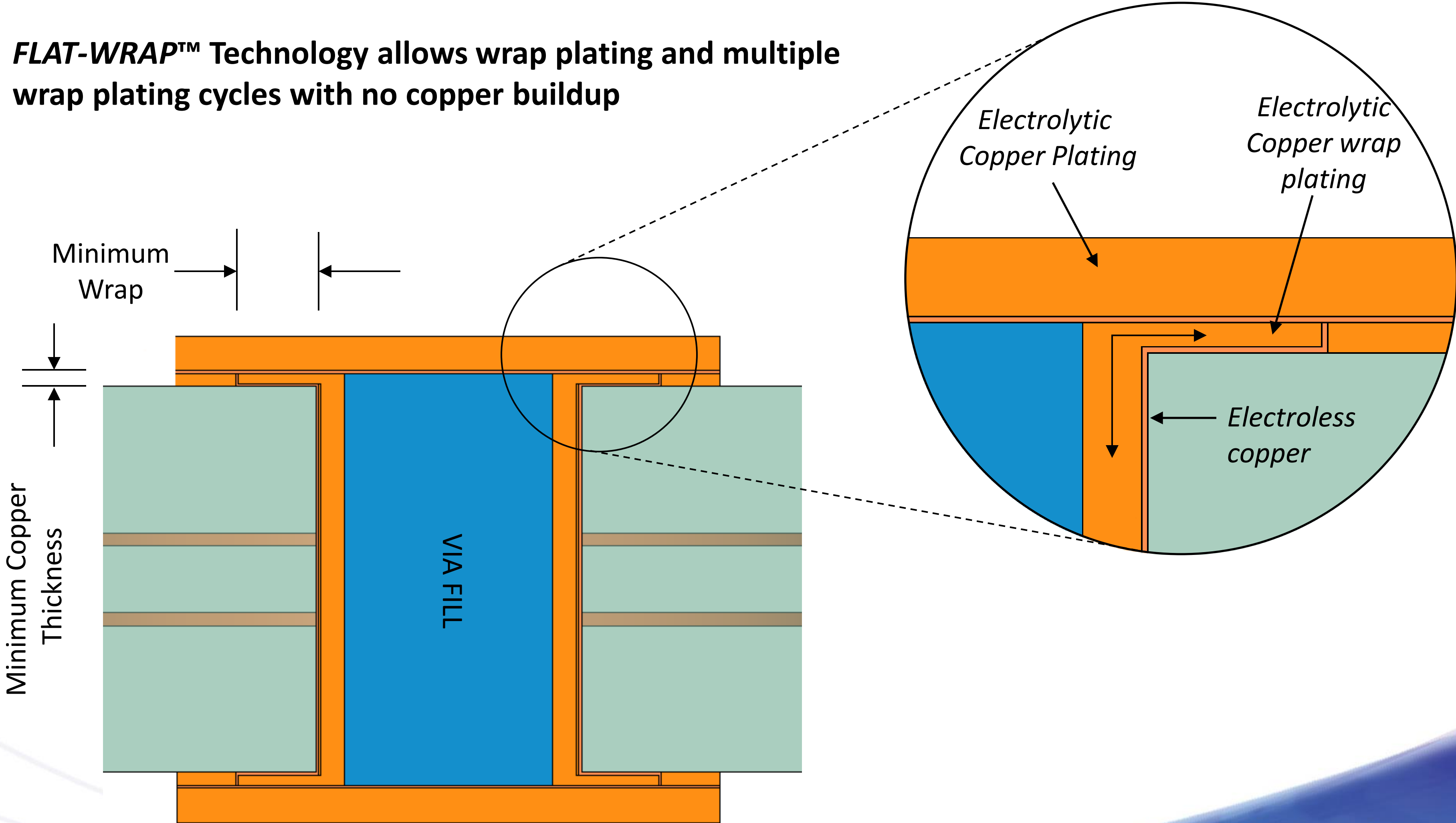


Non-conductive Via fill

Alternative Wrap Plating Technology

Minimizing Copper Buildup *FLAT-WRAP®*

***FLAT-WRAP*™ Technology allows wrap plating and multiple wrap plating cycles with no copper buildup**



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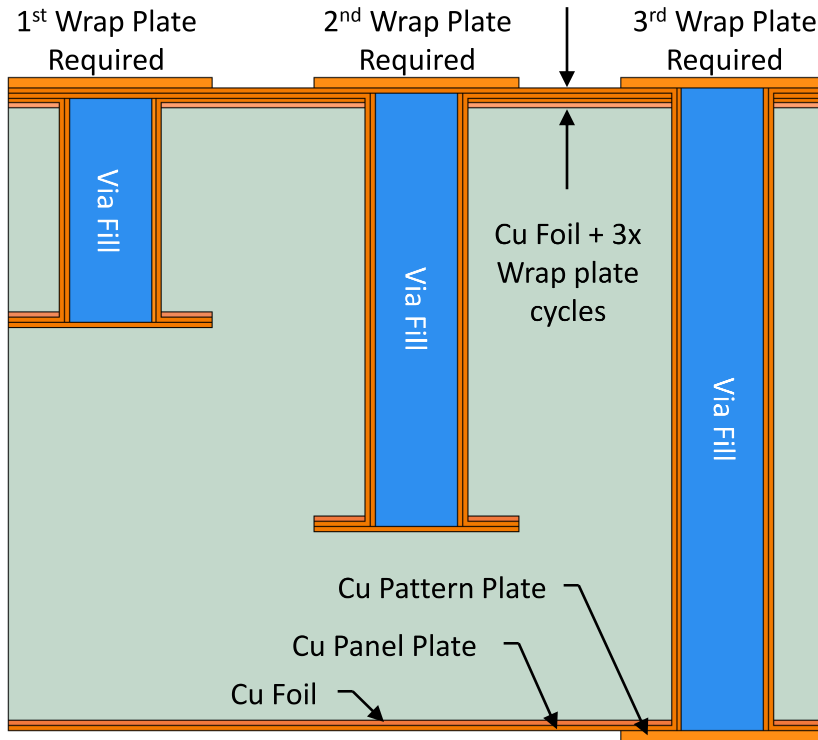
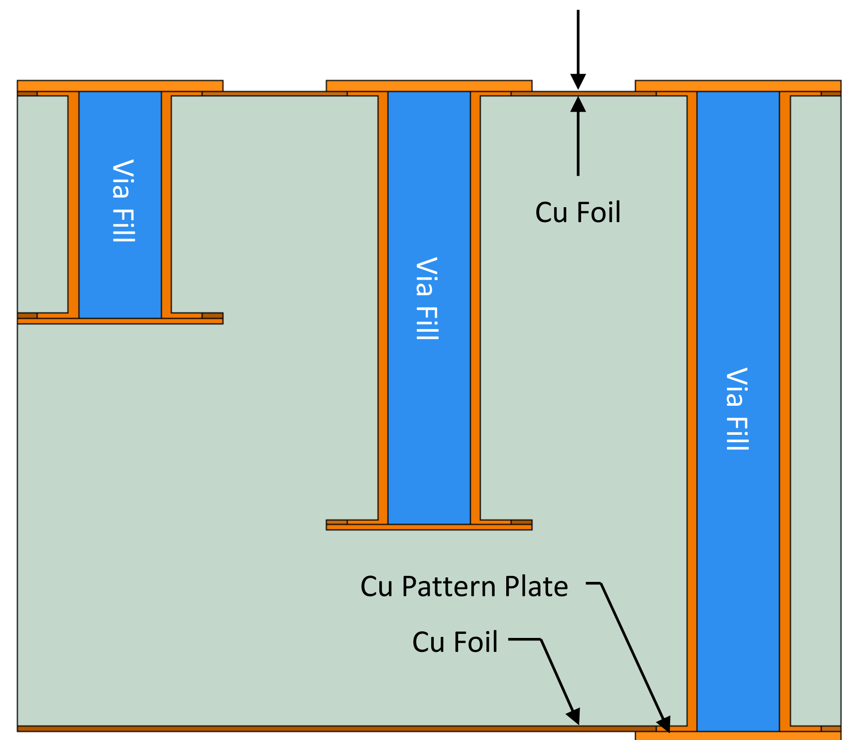
What Happens When More Than One Wrap Plating Cycle Is Required ?

Conventional Wrap Plating
(3x wrap on a common layer)

FLAT-WRAP™
(3x wrap on a common layer)



Total surface copper after 3x wrap

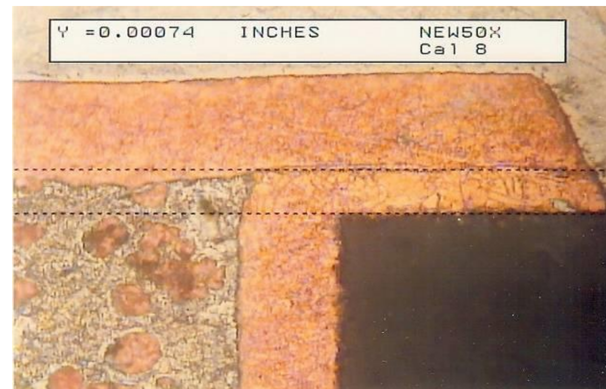


Total surface copper after 3x wrap
(Equal to starting base foil thickness)

FLAT-WRAP™ Technology

Current standard for

IPC 6012B Class 3, 3 x wrap



DDi's *FLAT-WRAP™* Technology

IPC 6012B Class 3, 3x wrap

• Industry specification (IPC 6012C) requires wrap-around plating for filled blind and buried via technology

• Current industry practices produce excessive plated copper on the required layer and limits the capability for surface feature packaging density (LWS dimensions)

• ***FLAT-WRAP®*** technology reduces surface copper thickness on multiple lamination product and enables finer geometries and facilitates improved design capabilities

Wrap Plating Design Guideline Comparison

Conventional Wrap Plate Design Guidelines

Design Rule	IPC 6012 Class 2 - assume a starting copper foil of 3/8 oz				IPC 6012 Class 3 - assume a starting copper foil of 3/8 oz			
	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater
Preferred	0.003" Line	0.005" Line	0.006" Line	0.006" Line	0.003" Line	0.005" Line	0.006" Line	Call
	0.0035" Space	0.005" Space	0.007" Space	0.009" Space	0.0035" Space	0.00575" Space	0.0085" Space	
Advanced capability = reduced yield (call engineering prior to quote)	0.003" Line	0.004" Line	0.005" Line	0.006" Line	0.003" Line	0.005" Line	0.006" Line	Call
	0.003" Space	0.005" Space	0.006" Space	0.008" Space	0.003" Space	0.0055" Space	0.0075" Space	

Note: Due to the overhang (caused by undercut during etch) all Gold body jobs or designs that utilize Gold as an etch resist and require wrap plating to meet IPC 6012, Class 2 or 3 specification, will need engineering approval prior to quote……no exceptions

FLAT-WRAP™ Technology Design Guidelines

Design Rule	IPC 6012 Class 2 - Starting copper weight 3/8 oz				IPC 6012 Class 3 - Starting copper weight 1/2 oz			
	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater
Preferred	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.0035" Line	0.0035" Line	0.0035" Line	0.0035" Line
	0.0035" Space	0.0035" Space	0.0035" Space	0.0035" Space	0.004" Space	0.004" Space	0.004" Space	0.004" Space
Advanced capability = reduced yield (call engineering prior to quote)	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line
	0.003" Space	0.003" Space	0.003" Space	0.003" Space	0.0035" Space	0.0035" Space	0.0035" Space	0.0035" Space

Note: Gold body jobs or designs that utilize Gold as an etch resist and require wrap plating to meet IPC 6012, Class 2 or 3 specification, will not need engineering approval if PCB's are fabricated with **this new t**echnology

FLAT-WRAP™ - Reliability Test Matrix

Description of Tests					Remarks	Test Status	Test Results
Manufacturability Tests	As received - Microsection PTH Quality	Plated Barrel Copper Thickness	Record Avg Plating Thickness		Microsection analysis performed by DDi	Completed	Passed
Pb-Free Assy Process Compatibility	Solder Float Test - Microsection PTH Quality	Temperature Deg C (Deg F)	260 (500)	3X	BGA coupons - DDi	Completed	Passed
				6X	BGA coupons - DDi	Completed	Passed
			288 (550)	3X	BGA coupons - DDi	Completed	Passed
				6X	BGA coupons - DDi	Completed	Passed
	Pb Free Reflow Assembly Simulation	Temperature Deg C (Deg F)	260 (500)	4X	Microtek Labs to process BGA coupons through Pb Free profile through IR Reflow oven and DDi to do microsection analysis	Completed	Passed
				6X			Passed
Reliability Tests	IST - Interconnect Stress Test	IST Pre-conditioning cycles at 260 C	4X		3 coupons / preconditioning (Total of 18 coupons). Dual sense test performed by DDi VA. Two different test conditions with San-Ei & CB100 via fill materials	Completed & Reported by Avg Cycles	Blind Vias No Failure & Thru Vias Pass 864 @ 6X & 1176 @ 4X
			6X				
		Pb Free Assembly Profile Pre-conditioning, peak temp 260 C	4X		IST testing to be perfromed by PWB Corp, Dual Sense to 1000 cycles	Completed & Reported by Avg Cycles	Blind Vias No Failure & Thru Vias Pass 731 @ 6X & No Failure @ 4X
			6X				
	HATS - Highly Accelerated Thermal Shock	Pb Free Assembly Profile Pre-conditioning, peak temp 260 C	0		12 coupons tested. Test performed by Microtek Labs. Two different test conditions with San-Ei & CB100 via fill materials	Coupons tested by MicroTek to 1000 cycles	Passed
			4X				Passed
			6X				987 average cycles

TTM Technologies

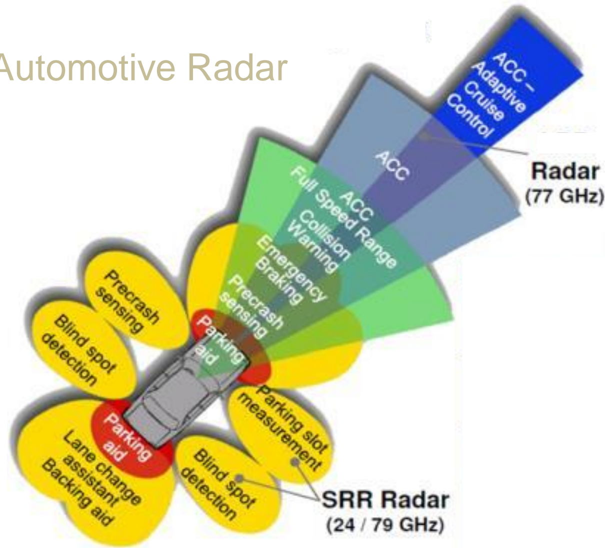
C^2eT

Controlled Copper Etch Technology

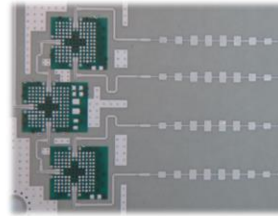
Precision Features For RF and Microwave Applications

Why Use Foil Only Features ?

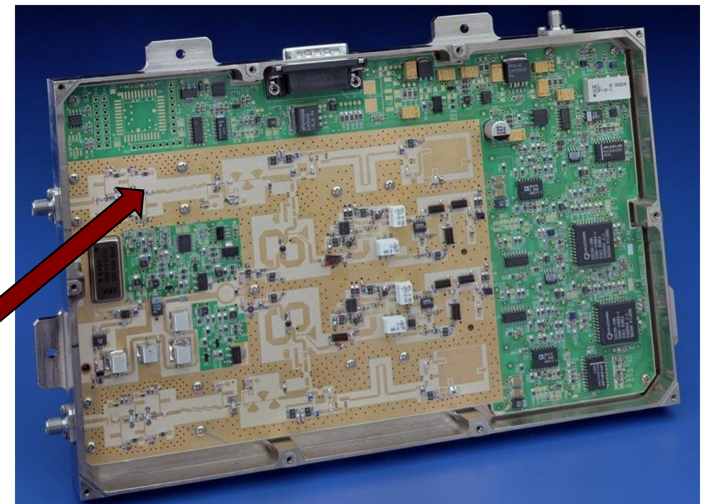
Automotive Radar

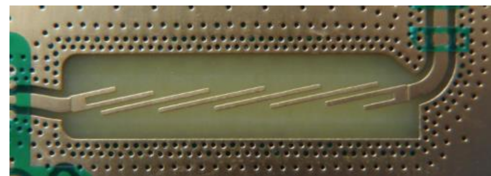


Precession etching for microwave antenna



Integrated Microwave Circuits



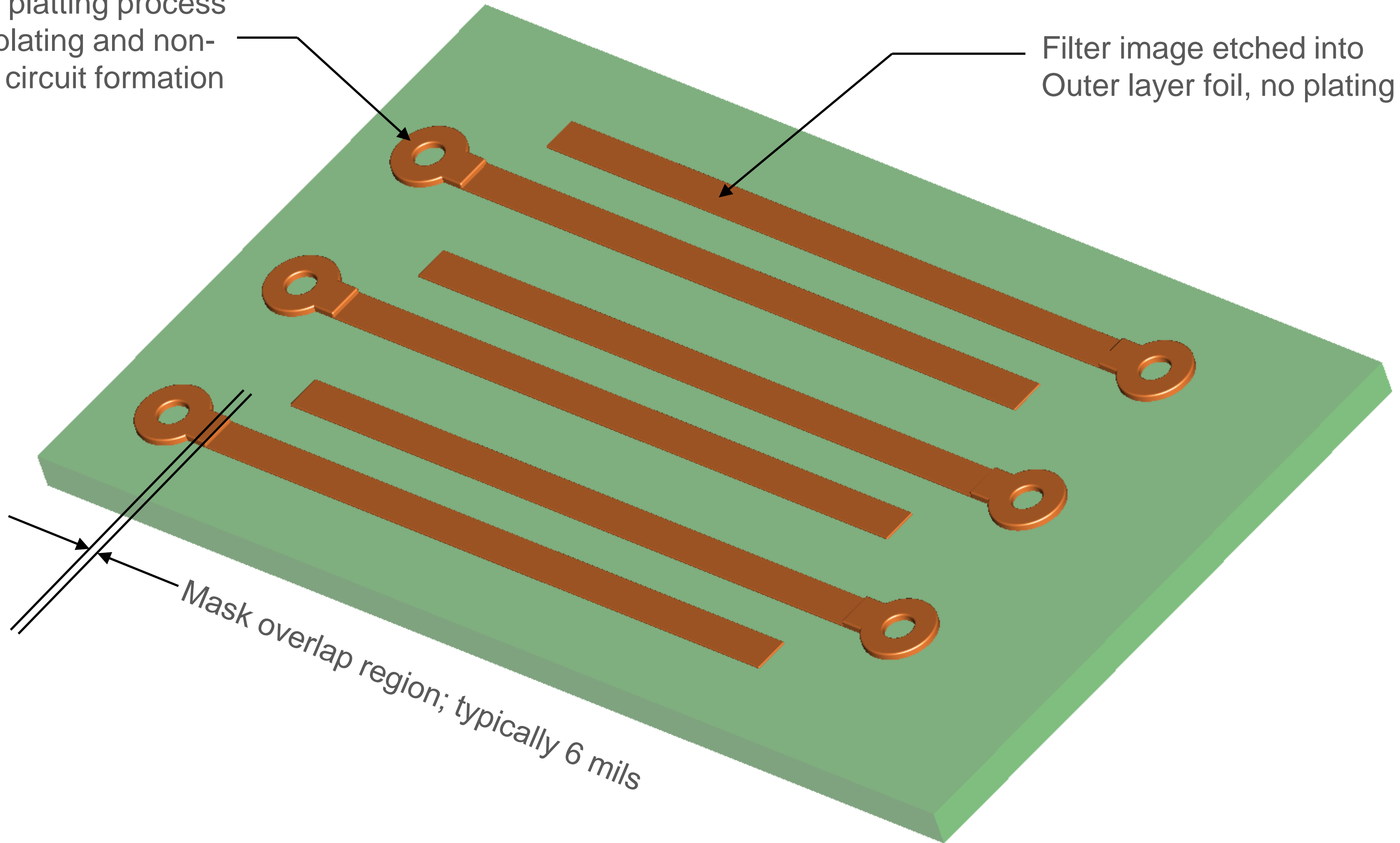


Filters and other precision etched components

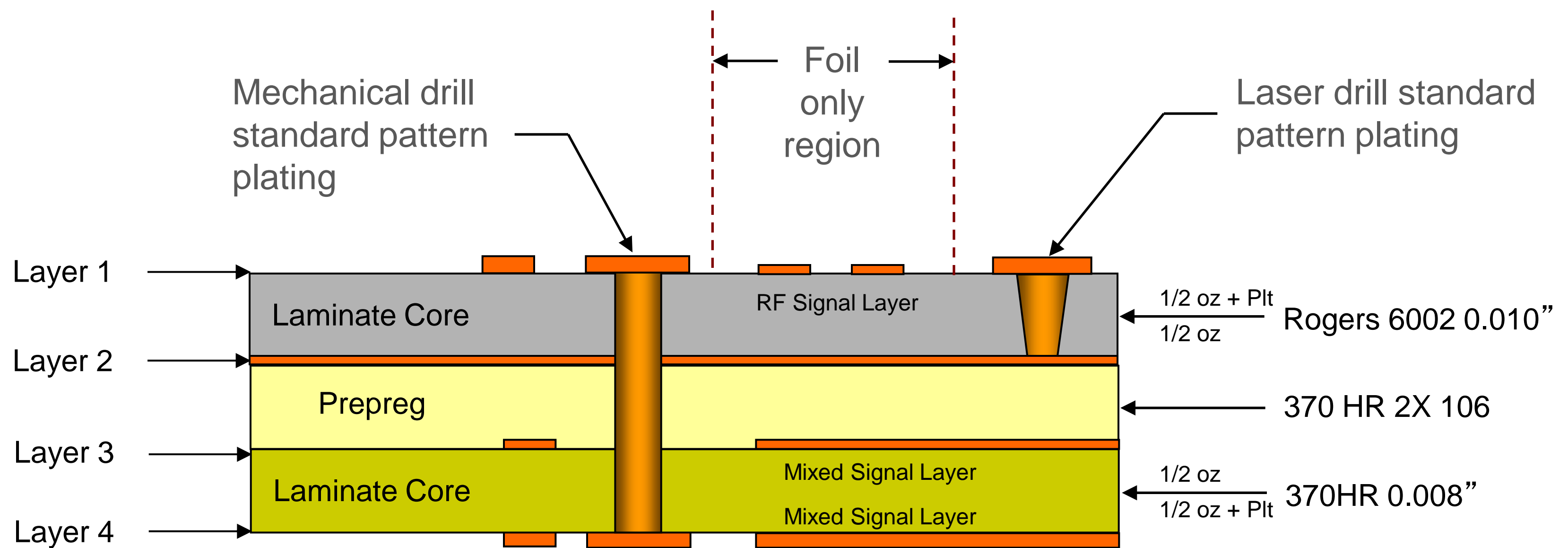
Why Use Foil Only Features ?

- RF and microwave circuits generally require printed components such as antenna, filters, couplers, resonators and precision taps
- As frequencies increase printed component size decreases with a demand for improved conductor resolution i.e. precise trace and space
- Current designs are demanding finished trace and space tolerance to be +/- 0.0005” to 0.0007” (predicated on customers demand for performance)
- Pattern plating on surface layers reduced conductor resolution
- Via-In-Pad required in many designs introduces wrap plating, increasing the background copper that must be etched, further reducing resolution
- Producing Foil Only etched features eliminates the plating and wrap plating in feature regions improving resolution

Applications In RF & Microwave Circuits

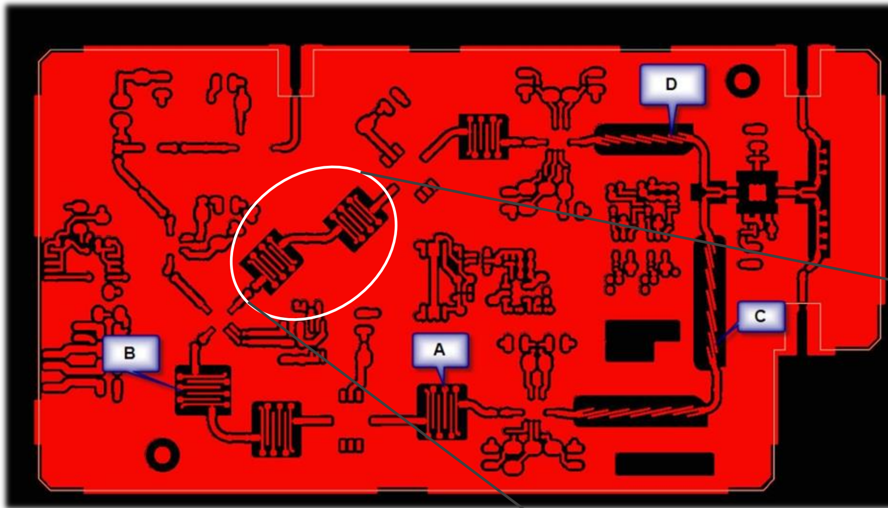


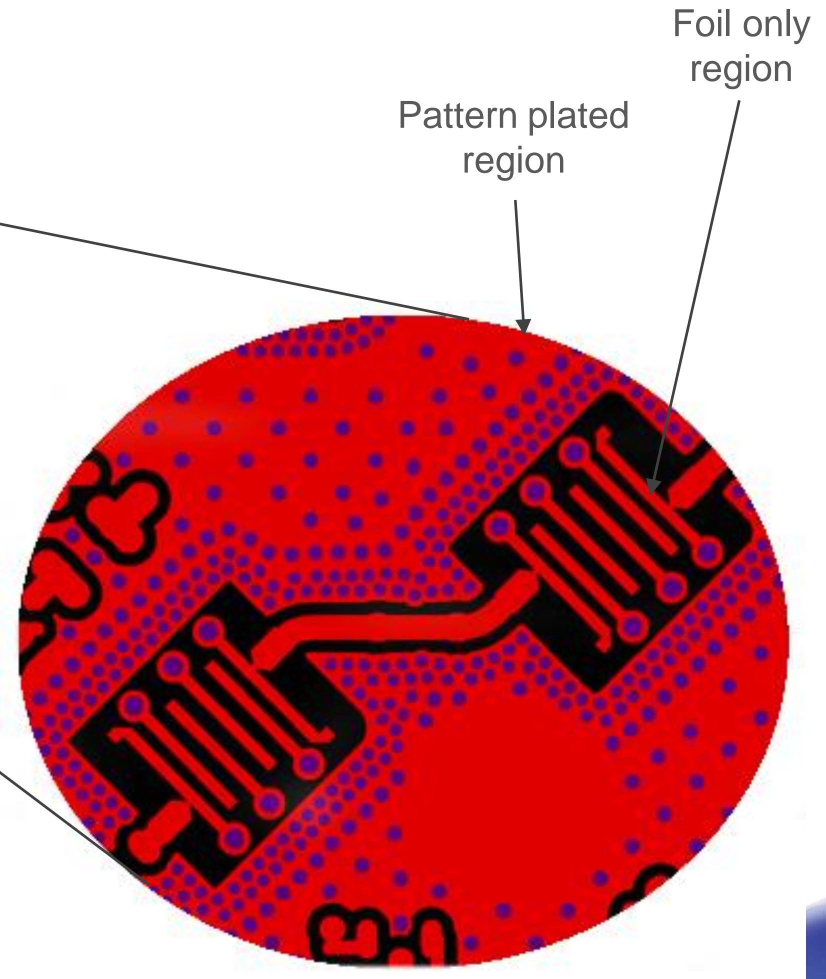
Sample stack-up of RF & Microwave job



Example of PCB Outer Layer

RF Outer Layer With Printed Filters





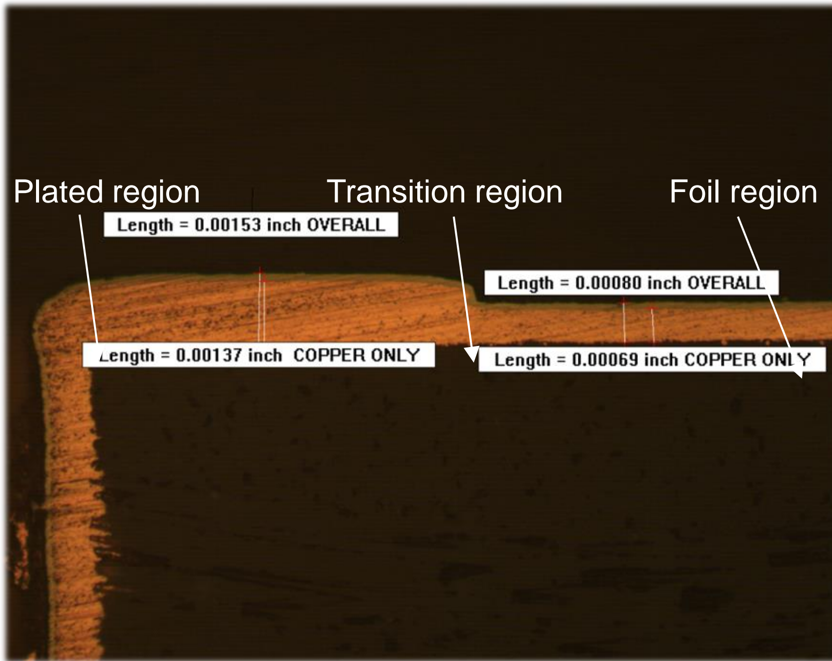
- Foil region consists of only foil and Cu flash plate
- Pattern plate region, standard copper thickness
- Photo tools are required for:

  Foil only print and etch

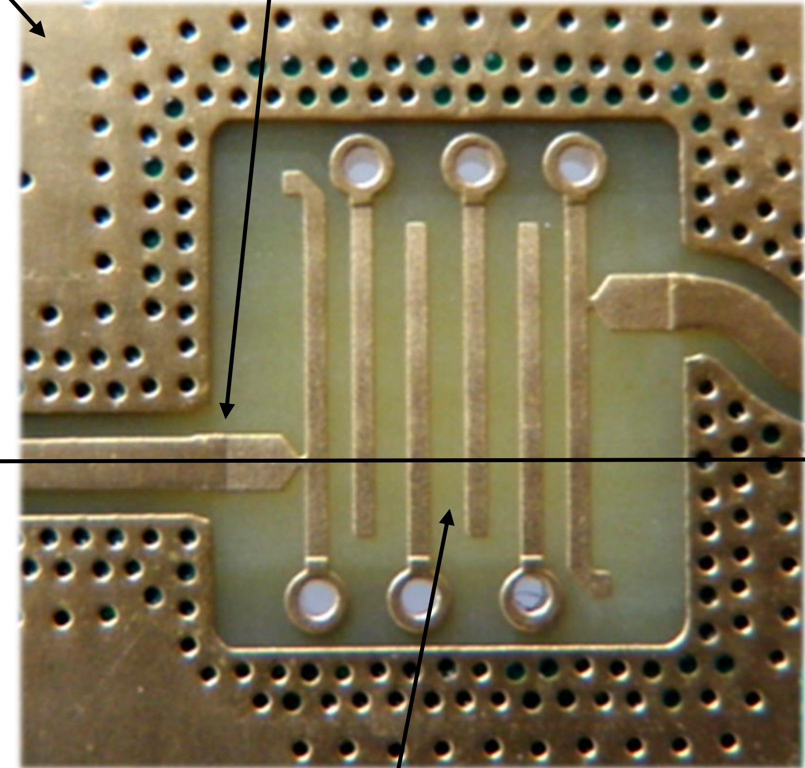
  Pattern plate tools with foil only isolation

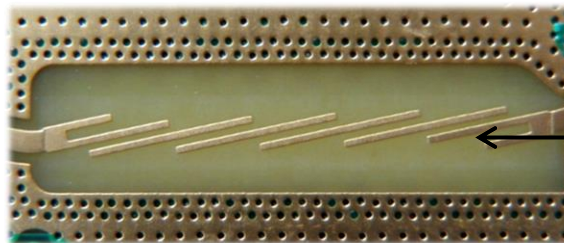
  Foil only photo tool to protect Foil Only region in final etch

Foil Only Features On Surface Plated Layers



Trace cross-section A-A

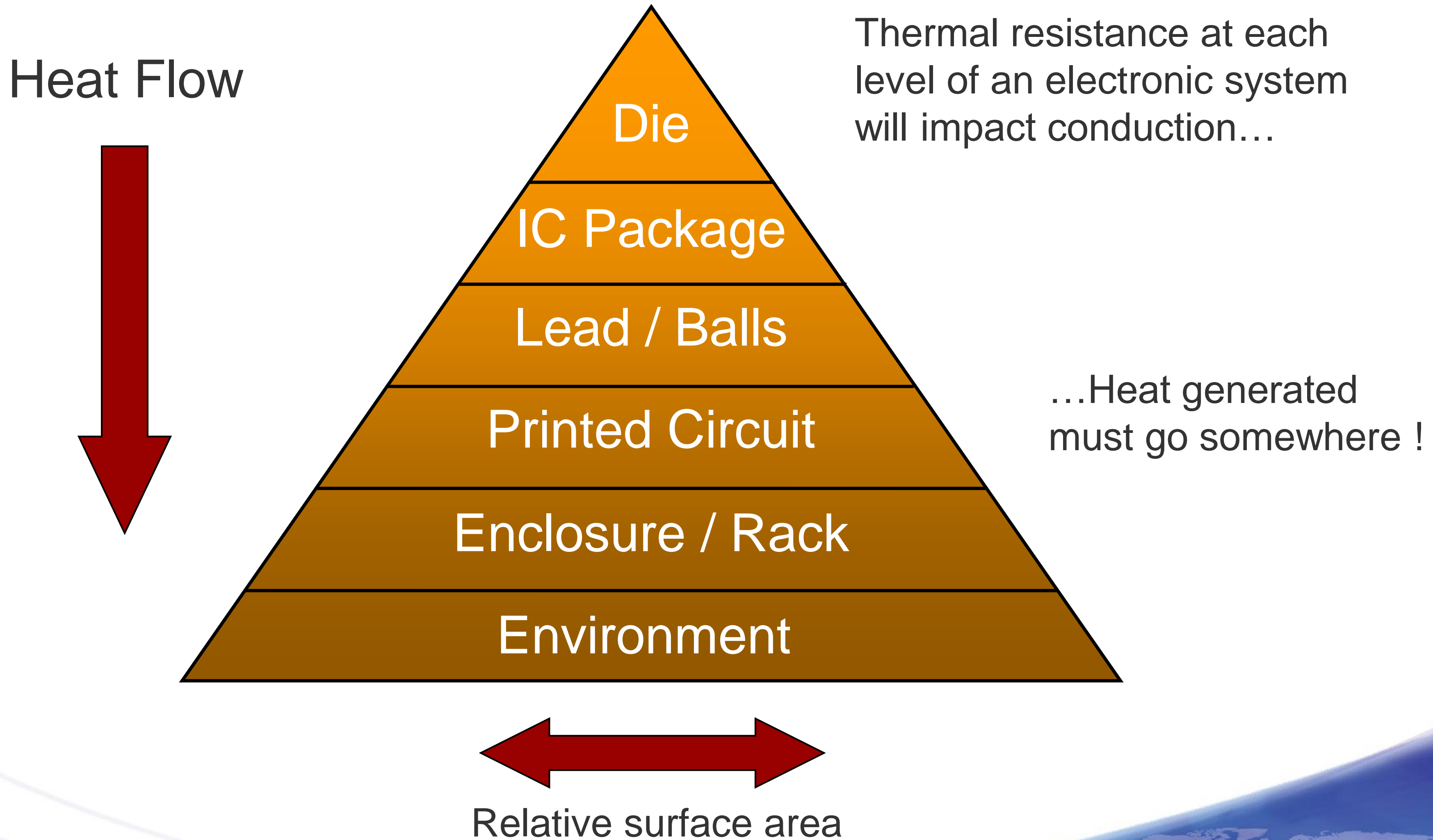




Advanced Thermal Management Techniques

TTM Technologies

Thermal Conduction In PCBs



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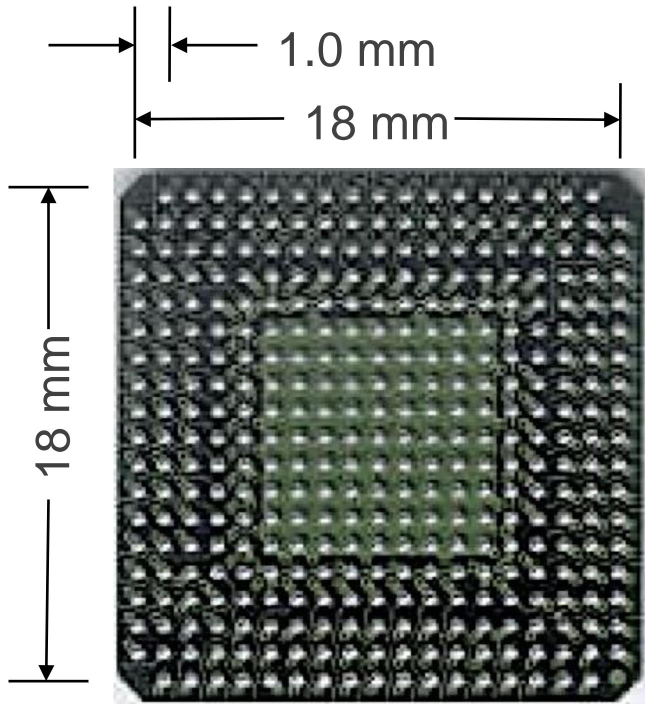
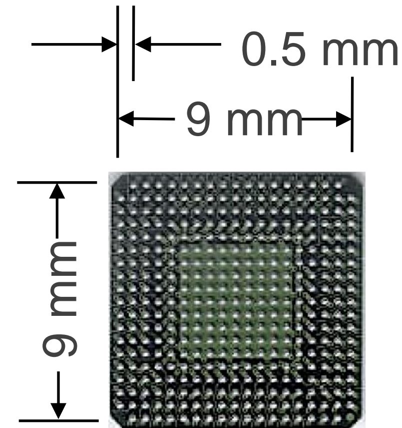
Factors Increasing Thermal Density

- Dramatic increase in Semiconductor power
- Rapid reduction in component size



Power dissipation 3 watts

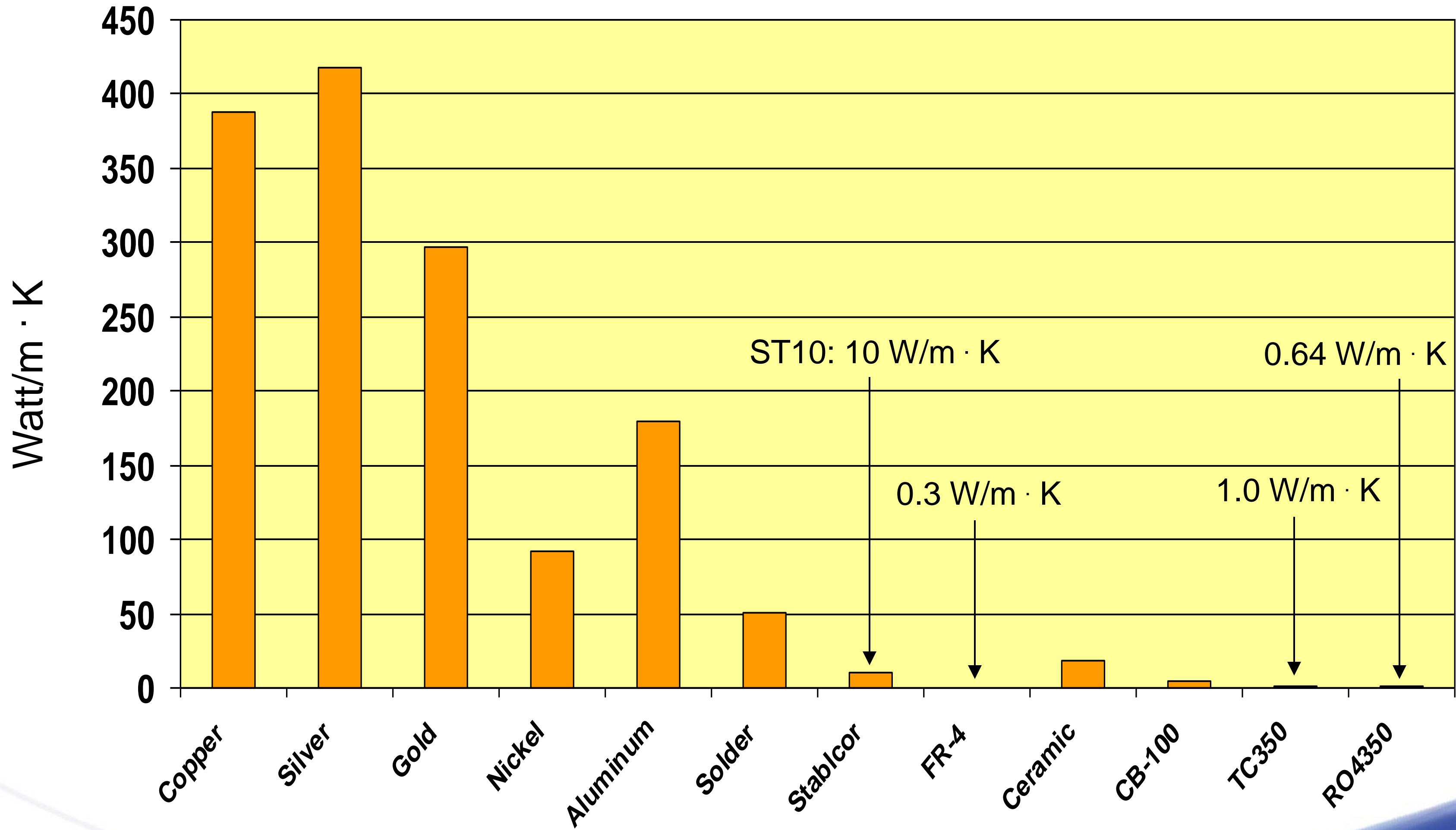
Power density 1.08 watts/cm



Power dissipation 3 watts

Power density 3.7 watts/cm

Thermal Conductivity



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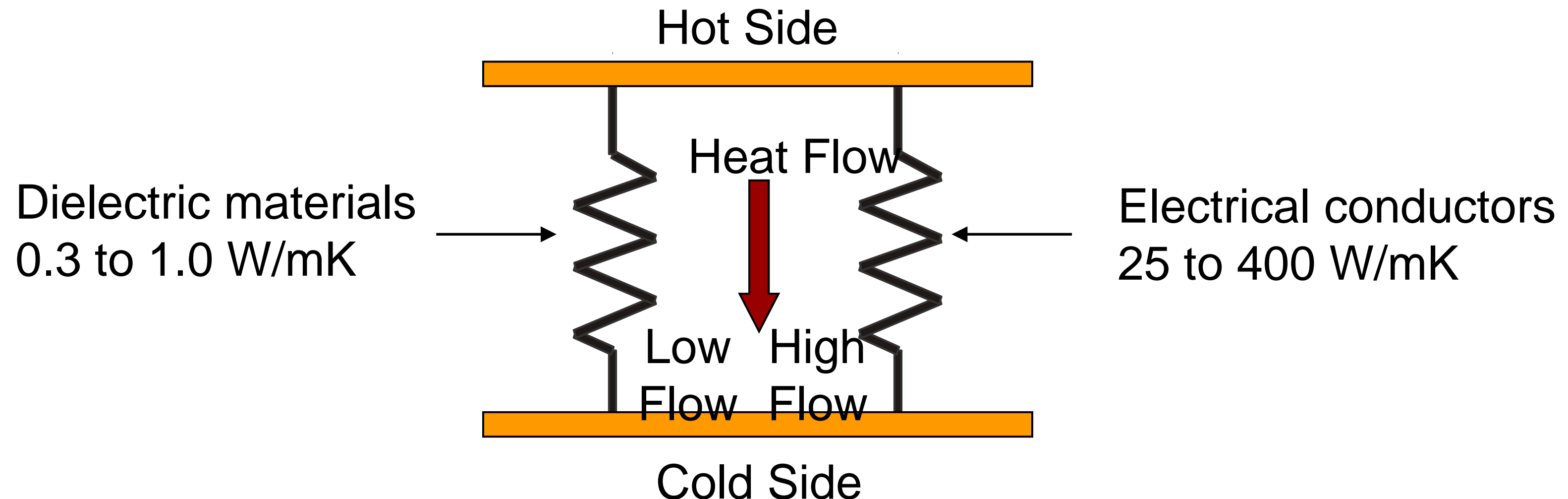
Thermal Limitations Of Dielectric Materials

Common dielectric materials have relatively low thermal conductivities where as electrical conductors have relatively high conductivities…



… Increased thermal conductivity is achieved with conductors

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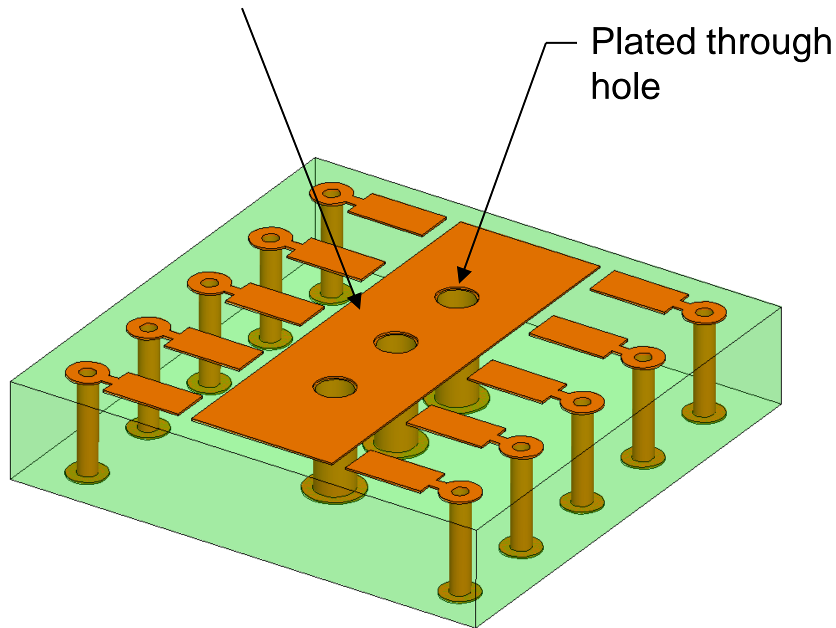
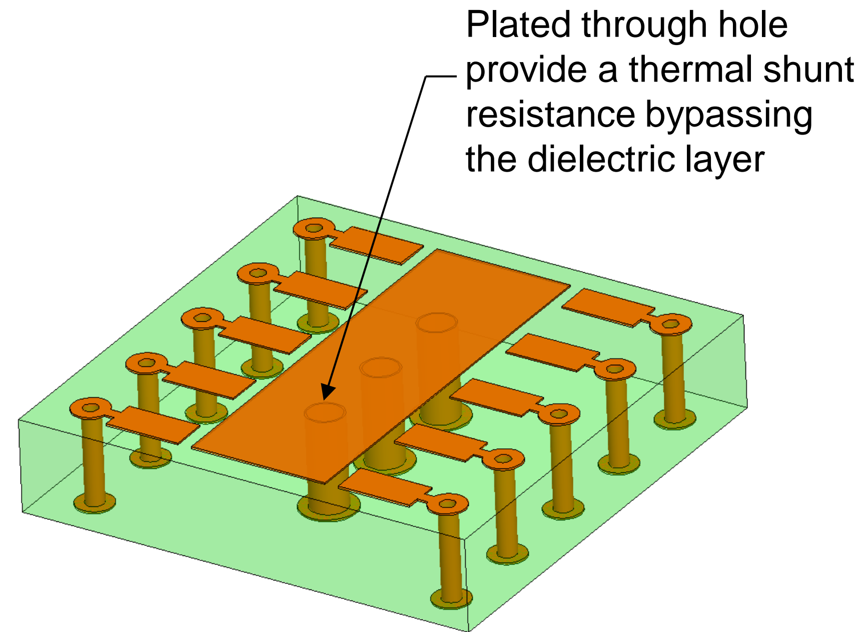
Thermal Via Applications

Thermal pad for conducting head from the component to internal planes or external heat sink on the back of the board



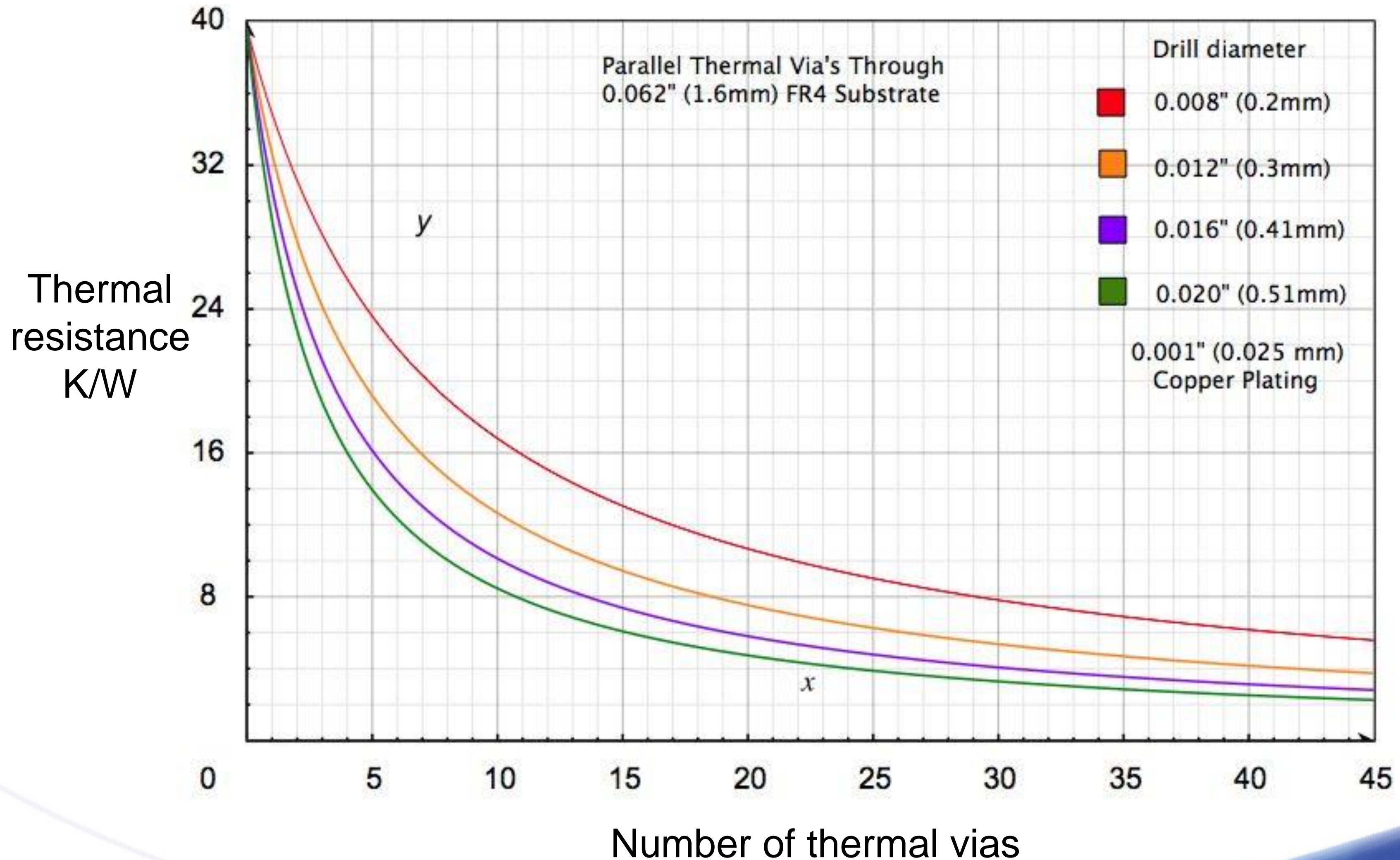
Via-In-Pad Construction



Issues: Through holes will wick solder away from the component connection and deposit on the back side of the board !

Assembly issues have been eliminated !

Thermal Resistance: Parallel Thermal Vias

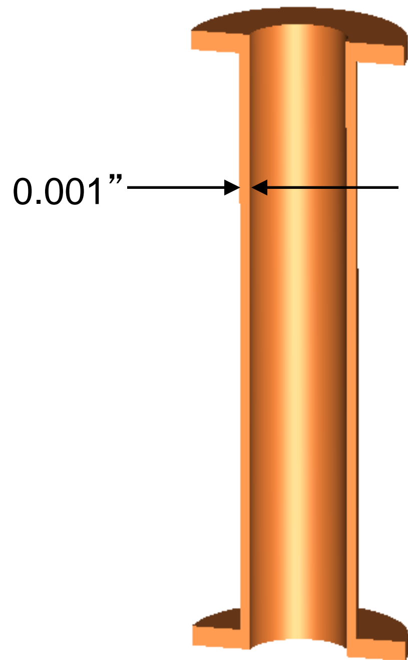


Note: Thermal via's placed in a 1.0 cm (0.0394) square

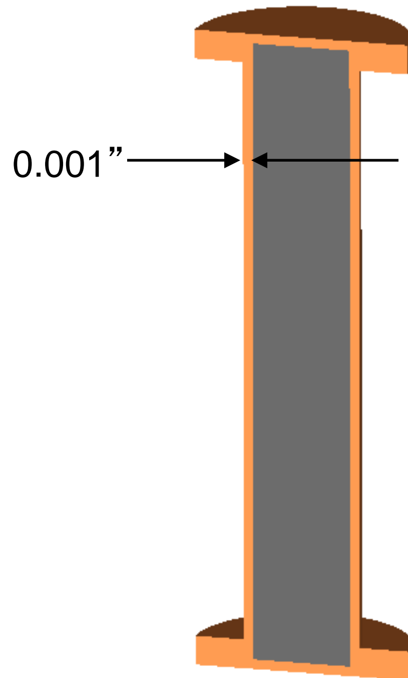
Methods To Increase Thermal Via Conductivity

Common thermal via constructions:

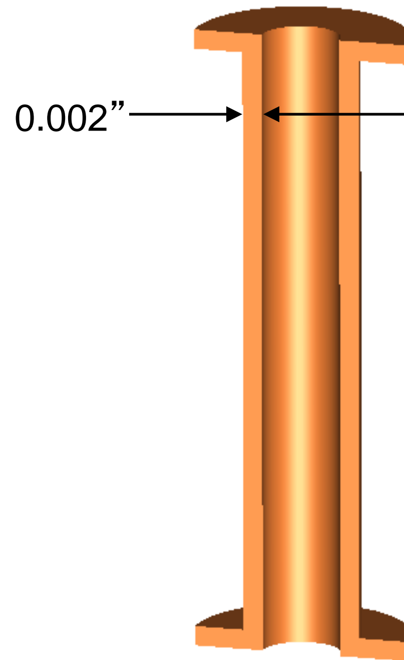
Copper = 380 W / m K
Conductive filler =3.5 to 6.7 W /m K



Standard



Conductive Filled



Thicker Copper

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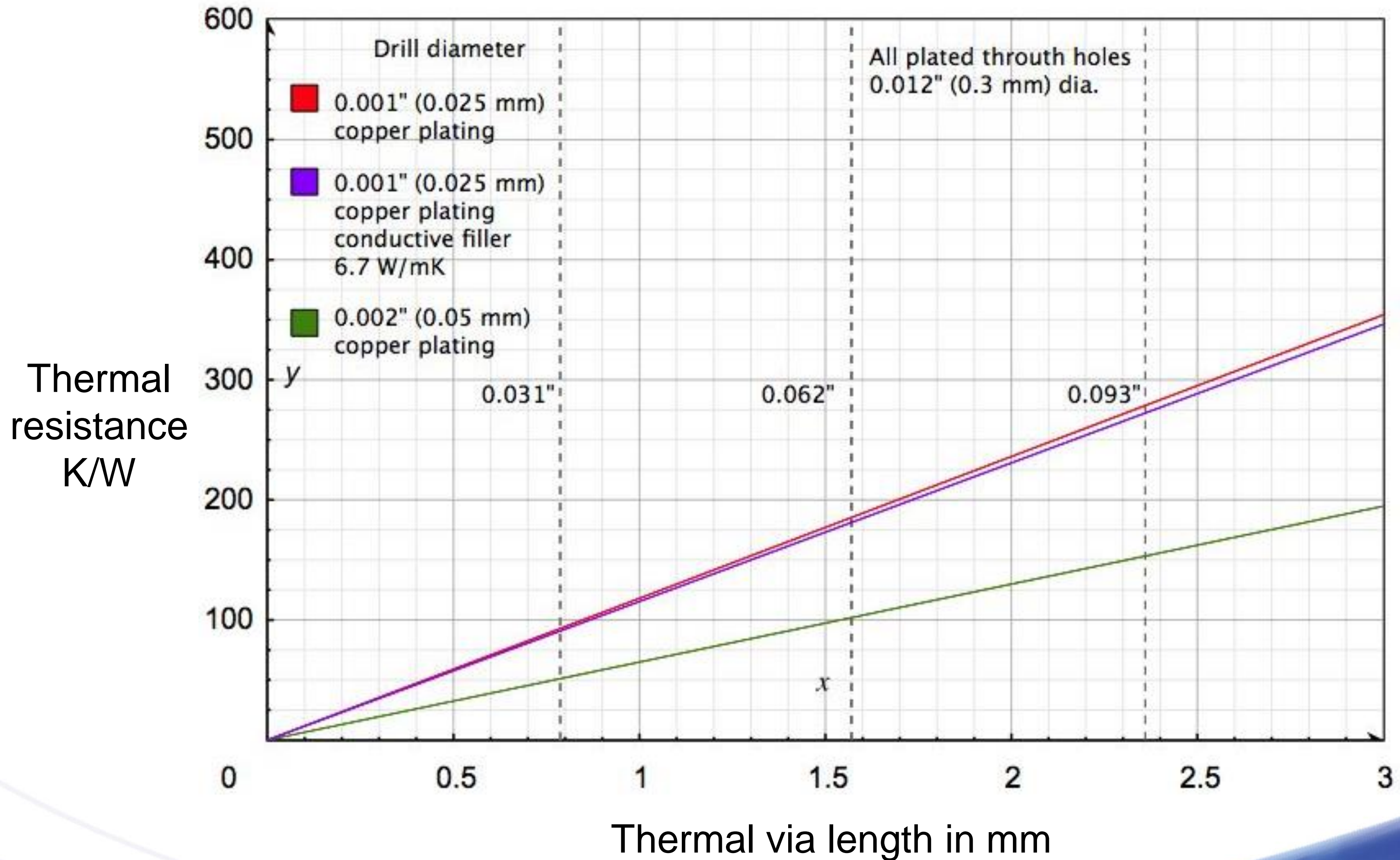
Thermal Resistance vs Via Technologies



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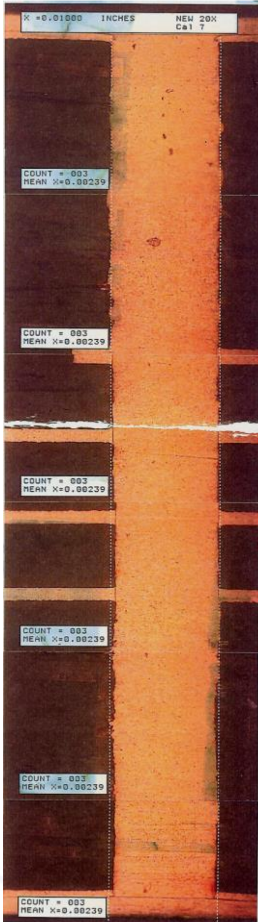
Solid copper Thermal Vias

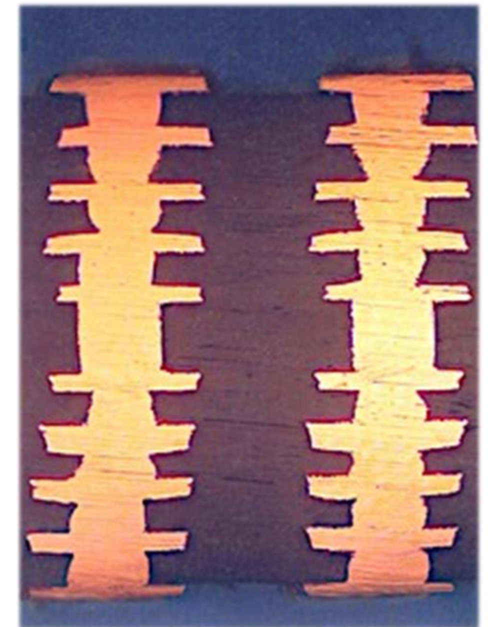
Solid Copper Via

0.010” Diameter

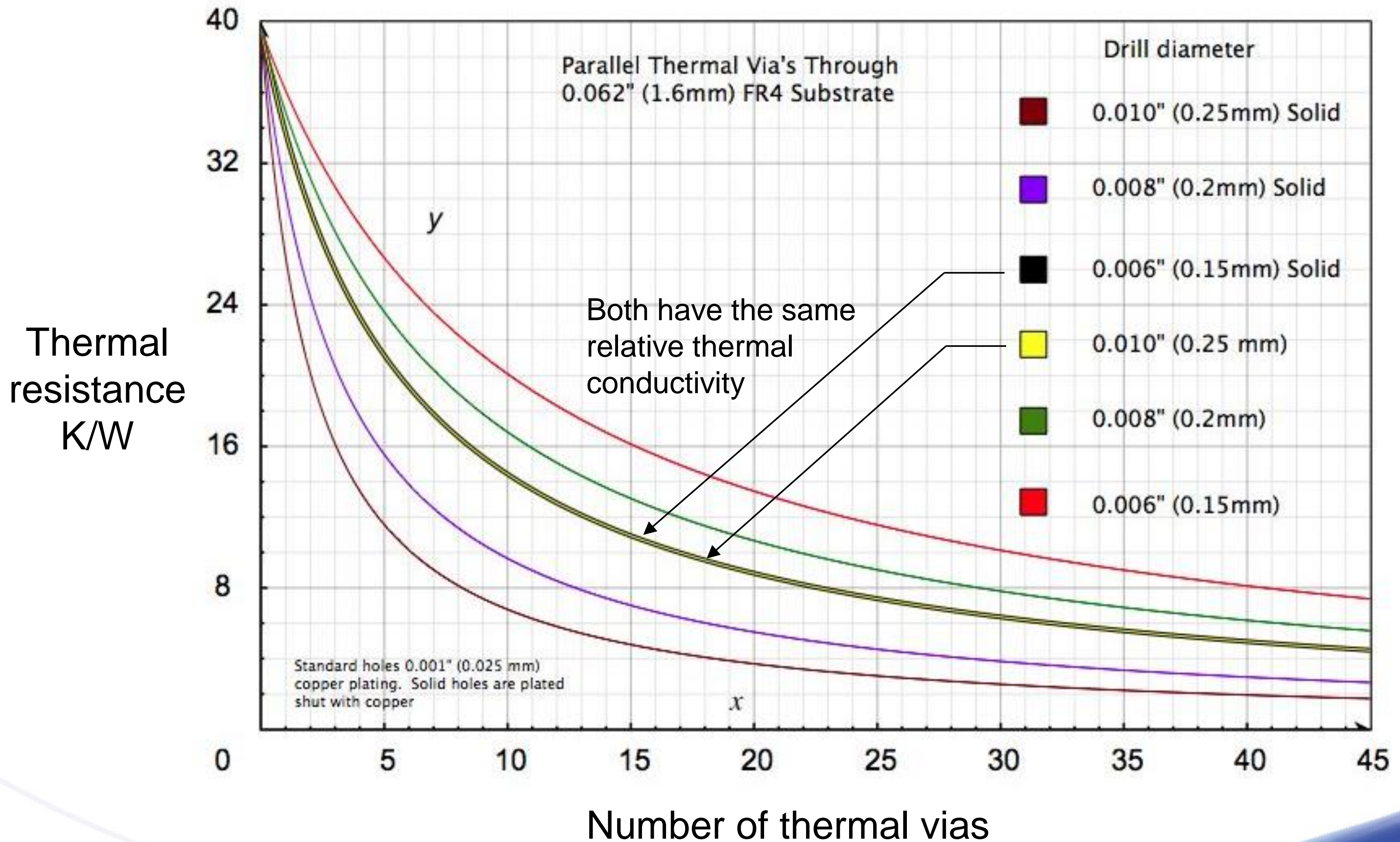


- Process to provide solid copper fill at accelerated plating rates
- 10:1 aspect ratios are currently achievable
- Applications include:
  - Low resistance via’s allowing high current or reduced diameter
  - Thermal via’s with high conductivity
  - Potential replacement for wrap plating

Solid Copper Stacked Microvia



Thermal Resistance Parallel Vias



Note: Thermal via's placed in a 1.0 cm (0.0394) square

TTM Technologies

Long term PCB Technology Roadmap

5 Year Technology Roadmap

Line / Space	Internal	0.0025" / 0.003"	0.0025" to 0.002" / 0.003" to 0.0025"	0.002" / 0.0020"	0.0015" to 0.002" / 0.0015" to 0.0020"	0.001" to .0015" / 0.0015" to 0.002"
	External	0.003"/ 0.0035"	0.003" to 0.0025" / 0.003" to 0.0025"	0.002" / 0.0025" to 0.002"	0.002" / 0.002"	0.0015" / 0.002"
Plated Layer Etch Tolerance		+/- 0.001" to +/- 0.0005"	+/- 0.00075" to 0.0005"	+/- 0.0005"	+/- 0.0003"	+/- 0.0003"
Drilled Via	Drill Size	0.010" / 0.008" / 0.006"	0.010" / 0.008" / 0.006"	0.008" / 0.006"	0.006" / 0.004"	0.006" / 0.004"
	Pad Size	0.020" / 0.018" / 0.016"	0.018" / 0.016" / 0.014"	0.014" / 0.012"	0.012" / 0.010"	0.010" / 0.008"
	Hole to Cu	0.008" to 0.006"	0.007" to 0.006"	0.006" to 0.005"	0.005" to 0.004"	0.004"
PTH Aspect Ratio		12:1 to 16:1 / 16:1 to 20:1 (ATE 31:1)	16:1 to 20:1 (ATE 31:1)	20:1 to 24:1 (ATE 40:1)	24:1 to 28:1 (ATE 40:1)	28:1 to 33:1 (ATE 50:1)
Via Fill (Via-In-Pad)		10:1 to 12:1 (ATE 31:1)	12:1 to 16:1 (ATE 31:1)	16:1 to 20:1 (ATE 40:1)	20:1 to 24:1 (ATE 40:1)	24:1 to 30:1 (ATE 50:1)
BGA Pitch		**0.65mm / 0.5mm / 0.4mm**	**0.5mm / 0.4mm**	**0.5mm / 0.4mm**	**0.4mm / 0.3mm**	**0.4mm / 0.3mm**
Micro Via	Via Size	0.006" / 0.005" / 0.004"	0.005" / 0.004"	0.005" / 0.004"	0.004" / 0.003"	0.003" / 0.002"
	Pad Size	0.012" / 0.010" / 0.009"	0.010" / 0.009" / 0.008"	0.009" / 0.008"	0.008" / 0.006"	0.006" / 0.005"
Micro Via Aspect Ratio		0.6:1 to 1:1	0.8:1 to 1.2:1	1:1 to 1.25:1	1.25:1	1.25:1
CSP Pitch		**0.3mm / 0.25mm**	**0.3mm / 0.25mm**	**0.25mm / 0.2mm**	**0.2mm / 0.15mm**	**0.15mm / 0.10mm**
Micro Via	Via Size	0.004"	0.004" / 0.003" to 0.002"	0.004" / 0.003" to 0.002"	0.002" via or fan out from standard 0.004" microvia structures	0.0015" / 0.001"
	Pad Size	0.008" / 0.0068"	0.008" / 0.006"	0.006" / 0.005"	0.004"	0.003" / 0.003"
Line & Space - SMV with perimeter rout using std design		Perimeter rout only with 0.003"/ 0.0035" design rule	Perimeter rout only with 0.0025"/0.003" design rule	Perimeter rout only with 0.002"/0.0025" design rule	Perimeter rout only with 0.002"/0.002" design rule	Perimeter rout only with 0.0015" / 0.002" design rule
→		**2011**	**2012**	**2013**	**2014**	**2015**

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5 Year Technology Roadmap

Micro Via Aspect Ratio	0.6:1 to 1:1	0.8:1 to 1.2:1	1:1 to 1.25:1	1:1 to 1.25:1	1:1 to 1.25:1
SMV & High Aspect Ratio Seed Metallization & Electro Plating	4+N+4, evaluate PPR vs. DC	One step copper fill + pattern plate	High speed plating system	Plating distribution +/- 10%	High Speed High Throw Plating System & Chemistry
	One step copper fill + pattern plate	Vertical vs. Horizontal	Low temp vapor deposition of copper	Fully additive process	
SMV NextGen	Reliability testing and production readiness	Phase II, expand capabilities	Integrate to Occam (explore)	Leverage modular concept to next level stacking application	
Expand R-Flex Capability	Instal SMV process in OH	Rigid Flex capability in AH (should w e explore the	CSP on R-Flex	Embedded Components	Embedded Components
			BC & BR in R-Flex PCB		
Materials	Pb Free & Halogen Free, low Tg filled, High Perfromance filled, Z-axis Interconnect w ith conductive paste	Film based materials, High Perfromance Filled, FEP and bonding film	Advanced RF application	Film based, 0.001" to 0.002"	Film based, 0.001" to 0.002"
Surface Finishes	ENEPIG (Universal Finish), Pb Free HASL, depends on market demand	Ormecon (Ag finish using nano technology)	Electroless Gold (Neutral), depends on market demand	Direct Immersion Gold (DIG), depends on market demand	Nano technology surface finishes
Equipment / Process	LDI Solder Mask & Maskless Lithography, XACT, Pinnless Lamination, Vision Drill 180K+RPM	Maskless or Ink Jet Solder Mask, Vision Drill & Rout w ith variable RPM	Ink Jet Liquid Photo Resist, Next Generation Laser Drill	Quick Lamination Press	High speed laser structuring systems or w ater jet technology
Embedded Technology - Passives & Actives	EPT (BC = ultra thin filled substrate (<0.001") / BR = Ohmega & TICER)	Embedded Active Technology - Active devices in PCB (IC, capacitors, resistors, etc.)		Ink Jet Technology for BR	High Dk heavily filled materials
Thermal Management	Copper Core & Stablcor	Copper Core & Stablcor	Advanced materials w ith nano technology		Light w eight thermally conductive and not electrically conductive
Future Technologies	Emb Active Tech, Embedded Circuit w / transfer technology and laser trench process, Photovoltaics, Optoelectronics, MEMS, Printable Electronics, and other industry				
→	**2011**	**2012**	**2013**	**2014**	**2015**

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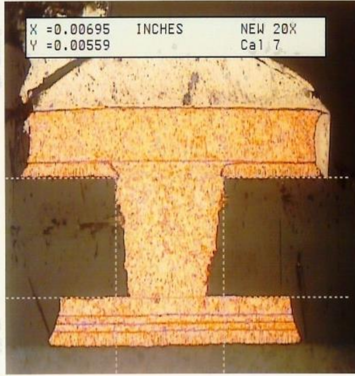
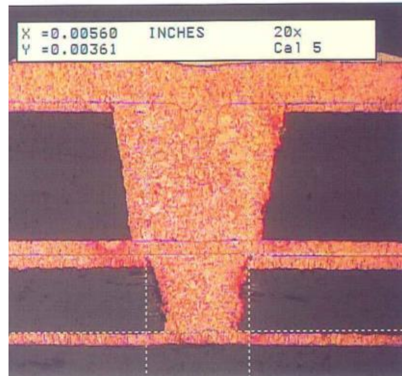
Viasystems Interconnect Technology

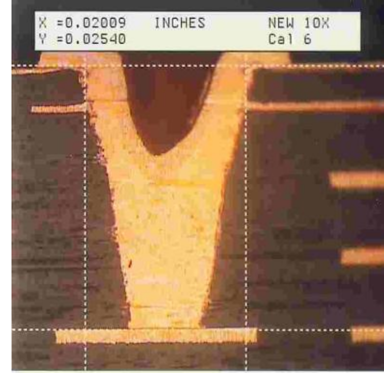
SMV®



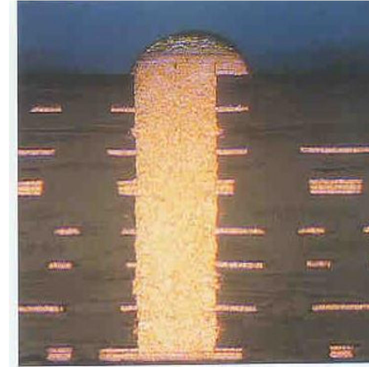
DpMV™



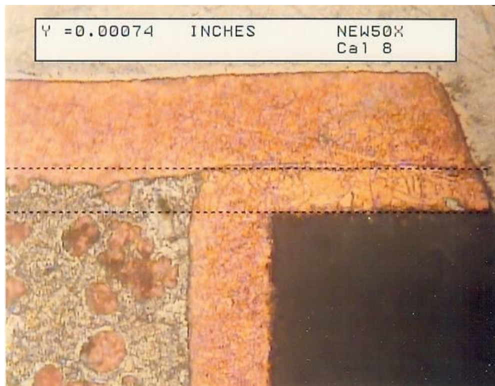
DpSMV™



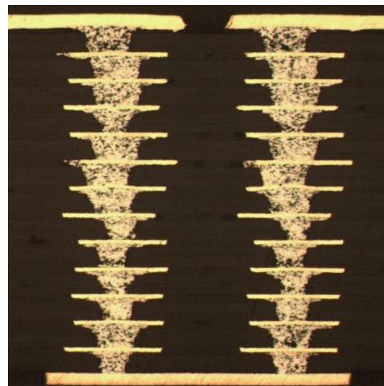
DpBV™



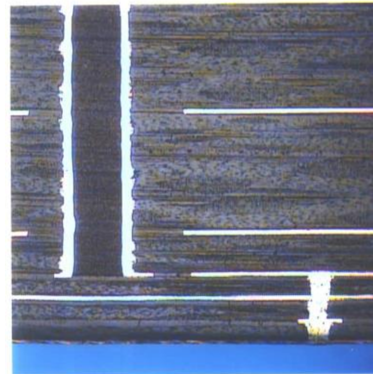
ThermalVia™



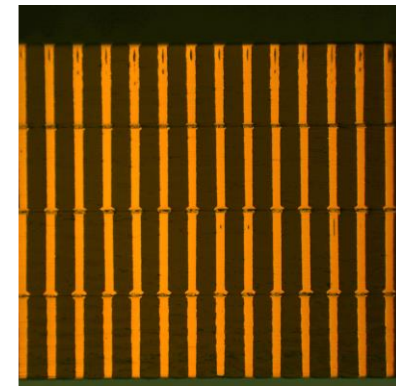
FLAT-WRAP™



NextGen-SMV®



HDI-Link™



Sub-Link™

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Summary

Today's Challenges are met by Enabling PCB Technologies…

- Start designs by defining the technology limiting packages
- Define the minimum technology set for the PCB design
- Look for a power delivery solution
- Review the design interactions with the technologies selected
- Make sure the technology level is compatible with your PCB supply chain
- Rethink design strategies before "bending" the rules

…Sometimes a little more time spent on a design can dramatically reduce cost

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Thank you!

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