

# What is New in IPC-7351C

by Tom Hausherr

*CEO & Founder of PCB Libraries, Inc.*

[www.pcblibraries.com](http://www.pcblibraries.com)

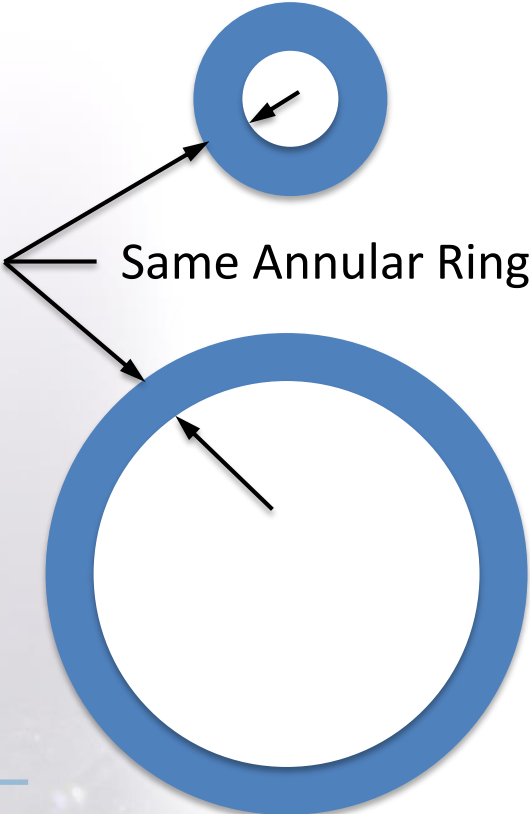




# 3-Tier IMD (Inserted Mount Device)

## The original IPC-7251 Concept for 3-Tier Pad Stack

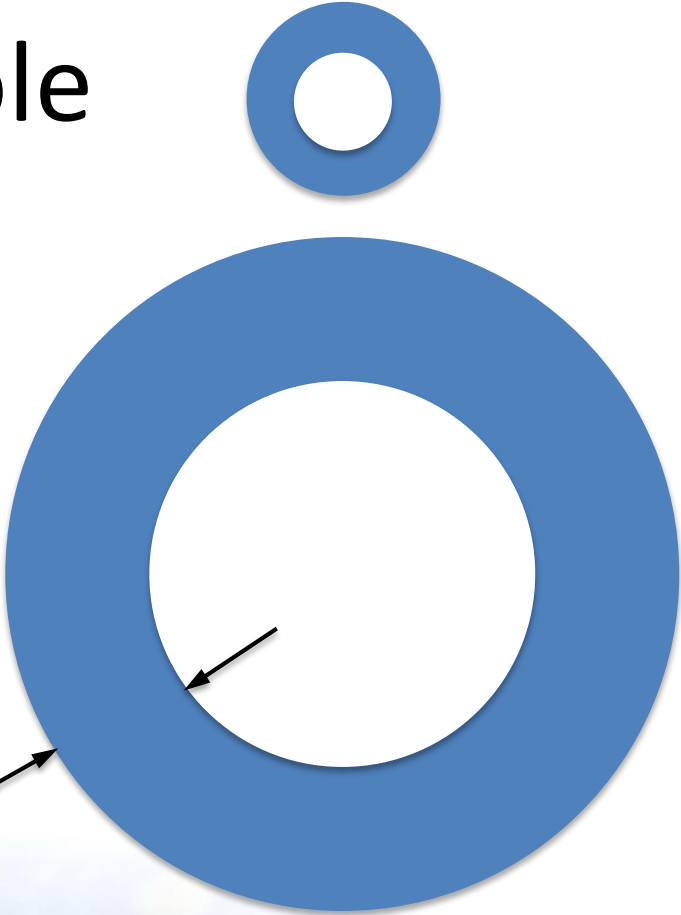
Joint Characteristics	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Hole Diameter Factor (over max lead)	0.25	0.20	0.15
Int. & Ext. Annular Ring Excess (added to hole dia.)	0.50	0.35	0.30
Anti-pad Excess (added to hole dia.)	1.00	0.70	0.50
Courtyard Excess from Component Body and/or Pads (which ever is greater)	0.50	0.25	0.12
Courtyard Round-off factor	Round up to the nearest even two place decimal, i.e., 1.00, 1.01, 1.02, 1.03 etc.		



Small Hole

Large Hole

Proportional Annular Ring

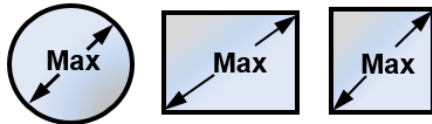


# No 3-Tier Library System

## IPC-7351C Proportional Pad Stacks



### PCB Library Expert IMD (TH) Reference Calculator

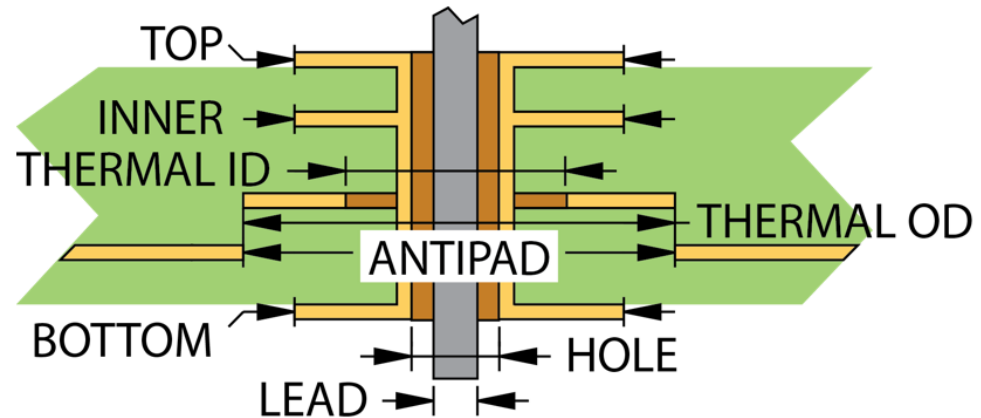


Enter Data:	
Maximum Lead (see above)	0.60
Hole over Lead	0.20
Pad to Hole Ratio	1.50
Thermal ID over Hole	0.40
Min. Thermal OD over ID	0.30
Thermal OD to Hole Ratio	1.10
Spoke Width(% of Th OD)	75
Round Off	0.05
Round Factor =	20

Restore Defaults

Version 1.0 (November 2014)  
© 2014 PCB Libraries, Inc.

Result:	
Hole =	0.80
Top, Inner, Bottom =	1.20
Thermal ID =	1.20
Thermal OD =	1.60
Anti-Pad =	1.60
Spoke Width =	0.30

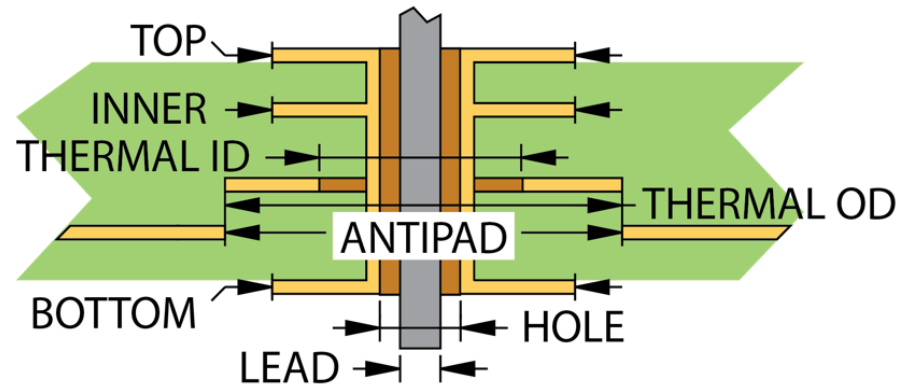
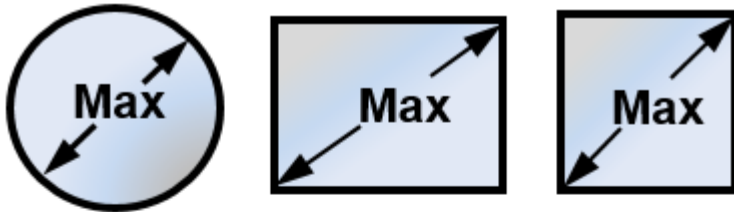


**FREE PCB Library Expert**  
[www.PCBLibraries.com/Downloads](http://www.PCBLibraries.com/Downloads)



**Questions?** Visit our online forum  
[www.PCBLibraries.com/Forum](http://www.PCBLibraries.com/Forum)

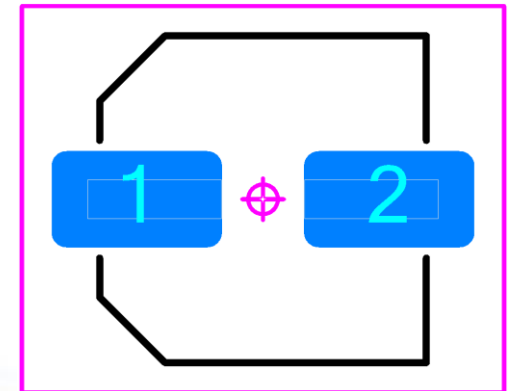
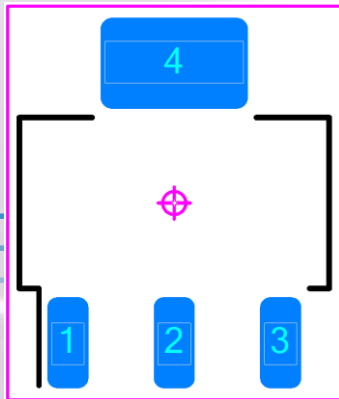
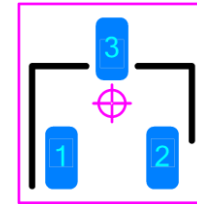
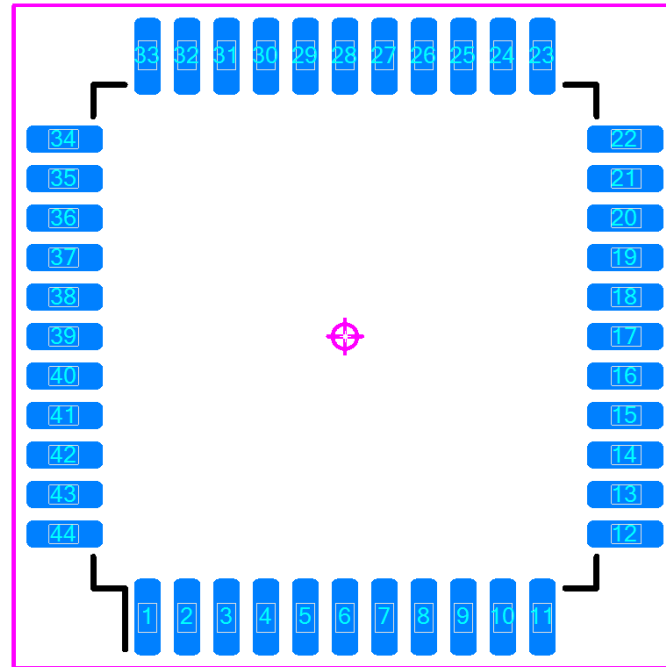
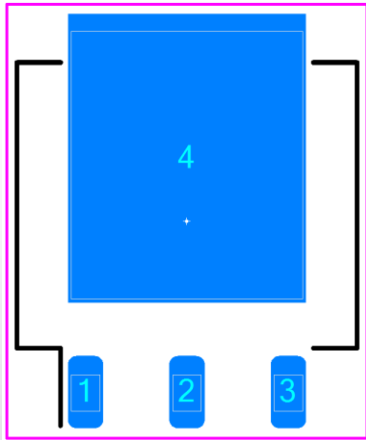
# IPC-7351C Proportional Pad Stacks



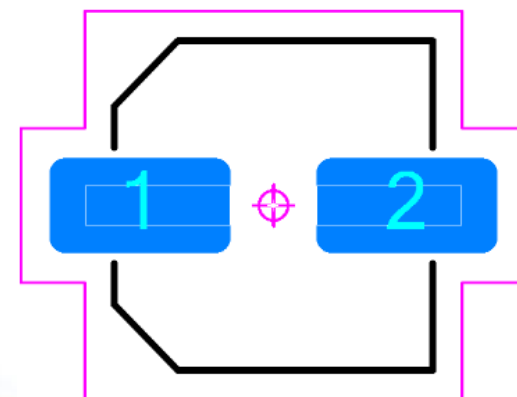
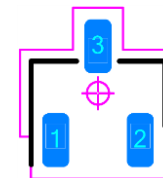
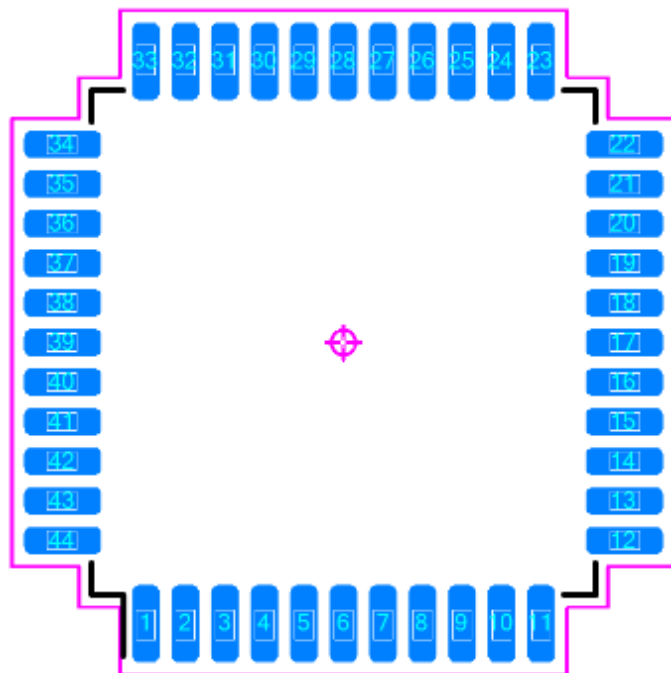
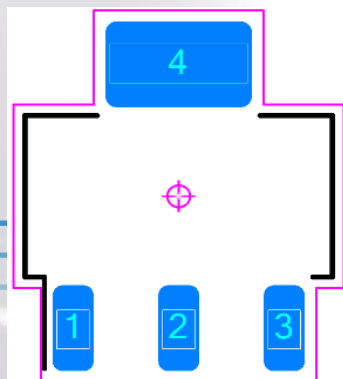
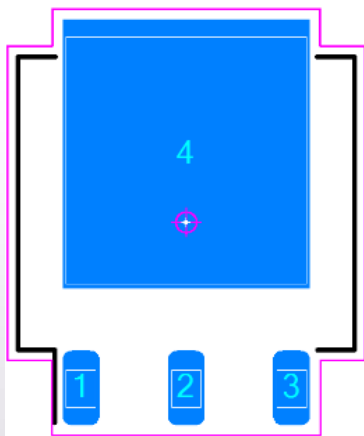
Enter Data:	
Maximum Lead (see above)	0.60
Hole over Lead	0.20
Pad to Hole Ratio	1.50
Thermal ID over Hole	0.40
Min. Thermal OD over ID	0.30
Thermal OD to Hole Ratio	1.10
Spoke Width(% of Th OD)	75
Round Off	0.05
Round Factor =	20

Result:	
Hole =	0.80
Top, Inner, Bottom =	1.20
Thermal ID =	1.20
Thermal OD =	1.60
Anti-Pad =	1.60
Spoke Width =	0.30

# IPC-7351B Rectangular Courtyards



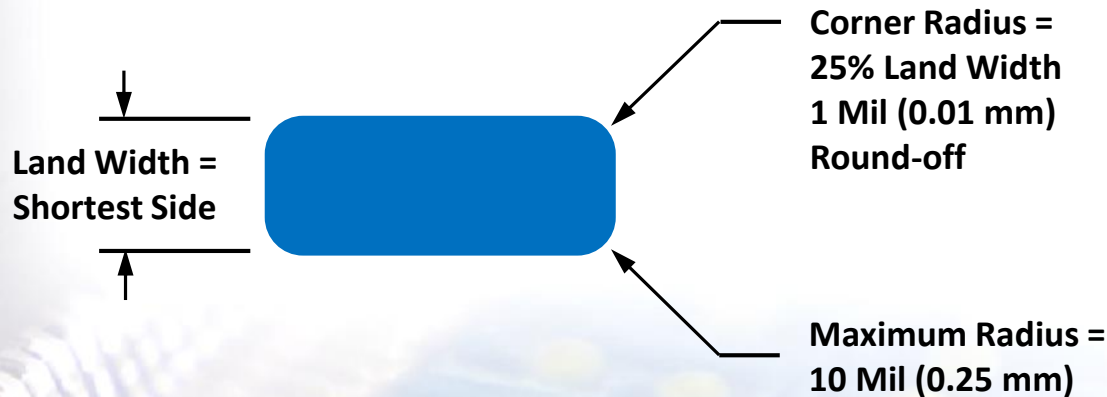
# IPC-7351C Contour Courtyards





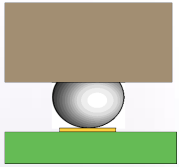
# Rounded Rectangle Pad Shape

- Most Component Manufacturer's Recommended Pad Shape is Rectangle
- IPC-SM-782 and IPC-7351B Recommended Pad Shape is Oblong
- IPC-7351C – Rounded Rectangle Pad

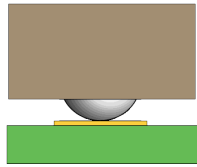


# Surface Mount Component Lead Styles

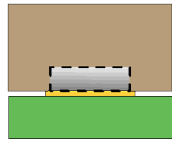
Ball Grid Array



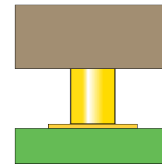
Bump Grid Array



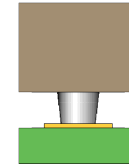
Land Grid Array



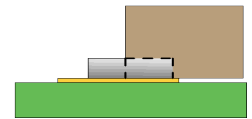
Column Grid Array



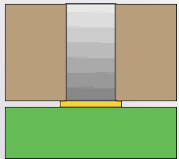
Pillar Grid Array



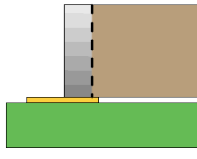
Flat Lug



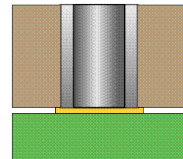
Flat Side



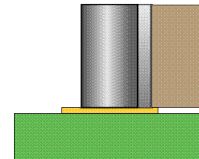
Convex Side



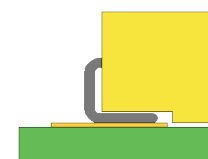
Concave Side



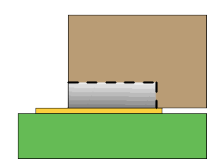
Corner Concave



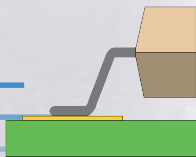
Inward L



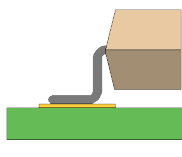
Flat Bottom



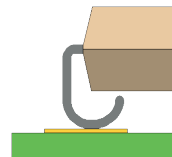
Gull Wing



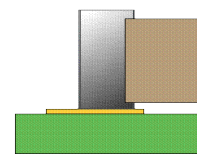
Outward L



J-Lead



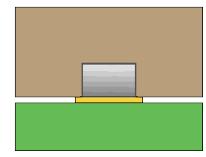
End Cap



Under Body L



No-Lead



# Lead Styles and Rounded Rectangle Pads

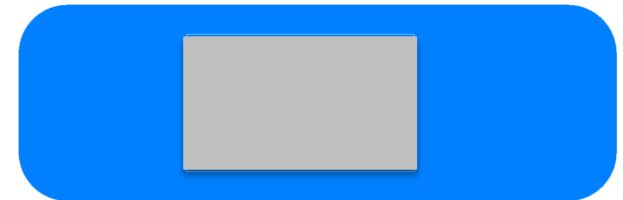
Under Body "L"



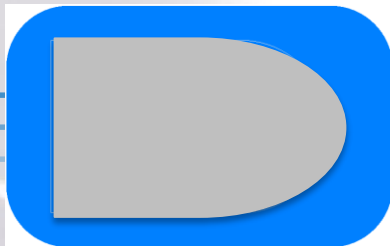
End Cap



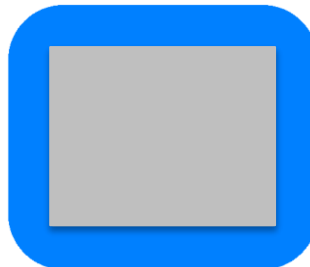
Gull Wing



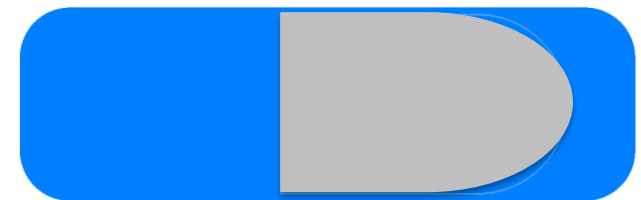
PQFN D-Shape



Corner Concave



QFN D-Shape



# Lead Styles Exempt from Rounded Rectangle Pads

---

---

- Ball Grid Array
- Column Grid Array
- Land Grid Array
- Dual Flat No-lead
- Thermal Pads
- Through-hole Square Pads

# Guidelines for Drafting Items

---

---

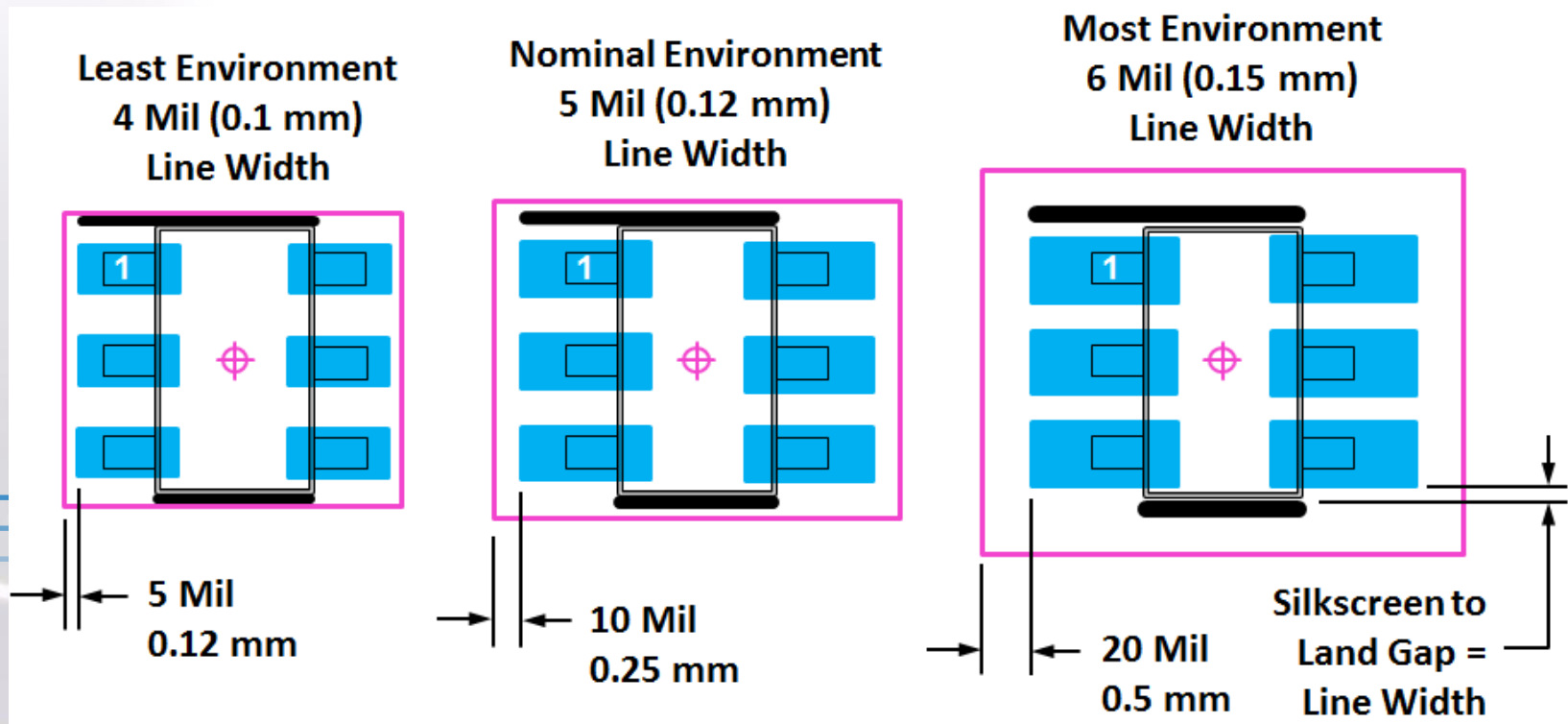
- Silkscreen Outline and Polarity Marking
- Assembly Outline and Polarity Marking
- Courtyard Outline
- Land Pattern Origin Marker
- Component Outline & Terminal Leads

# Silkscreen Outline Guidelines

1. No silkscreen outline under the component body; these get covered up during assembly and don't provide any useful purpose (waste of good ink)
2. Silkscreen outlines visible after assembly process and provide a functional use as alignment marking for assembly registration accuracy
3. Silkscreen outlines should be inside placement courtyard
4. Silkscreen outlines should be mapped to the Maximum Component Body with one exception, the Silkscreen to Pad spacing rule "overrides" the Component Body Mapping
5. Silkscreen outlines should map the component body and not go around pads. Excess silkscreen outlines should be avoided to make room for ref des locations. Silkscreen outlines should perform a "hatch" outline along the component package body.
6. Pin 1 is identified by extending the silkscreen along Pin 1 length of pads when component leads extend outward. Bottom only terminals Pin 1 is identified by a missing line.

# 3-Tier Silkscreen Outlines

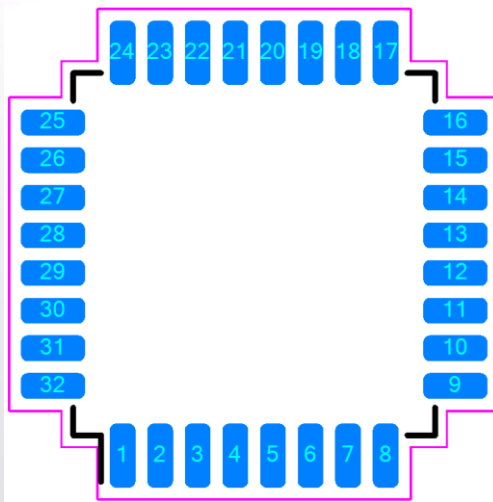
The preliminary recommendation for 3-Tier line widths and Silkscreen to Pad Gap are illustrated in the pictures below representing a SOT23-6 component package



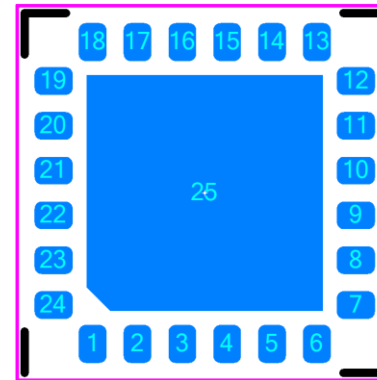
# Silkscreen Polarity Marking

## Gull Wing, Bottom Only & Chip

Gull Wing & J-Lead Polarity



Bottom Only Polarity  
Absence of Silkscreen



2-pin Component Polarity



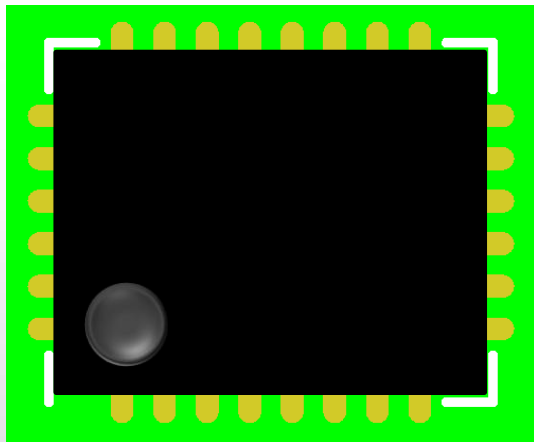
2-pin Component Non-polarity



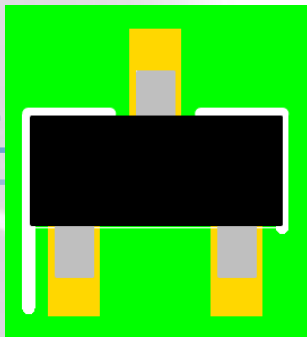


# Silkscreen Visible After Assembly

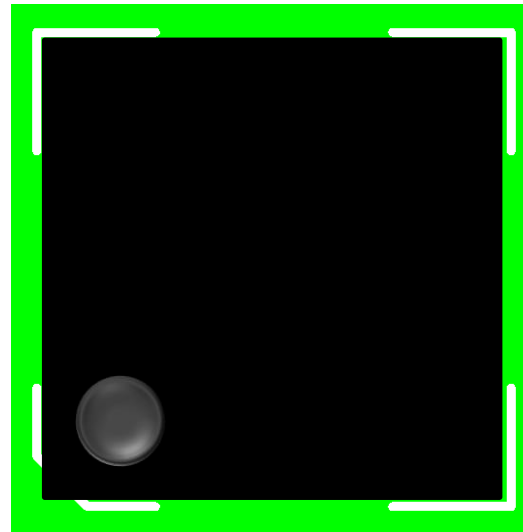
Quad Flat No-lead (QFN)



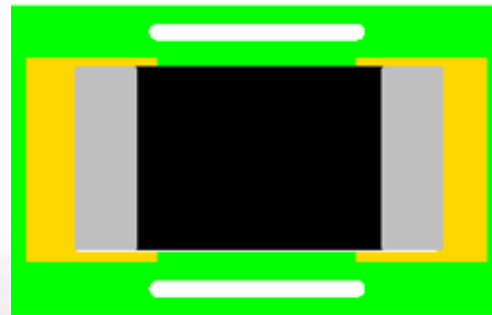
SOT23



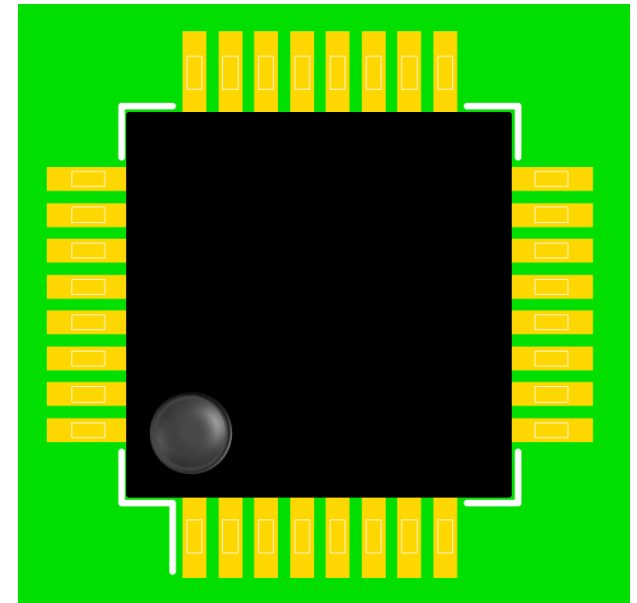
Ball Grid Array (BGA)



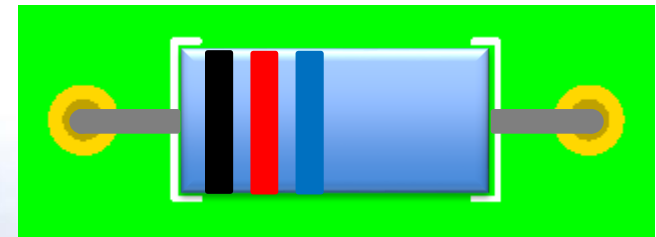
Non-polarized Silkscreen



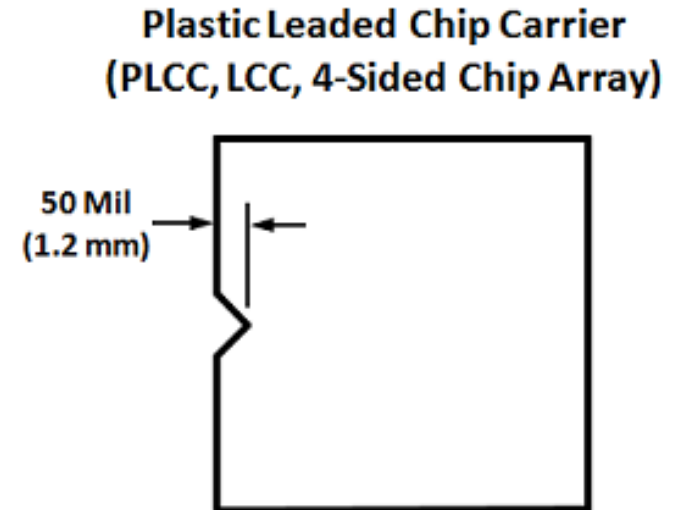
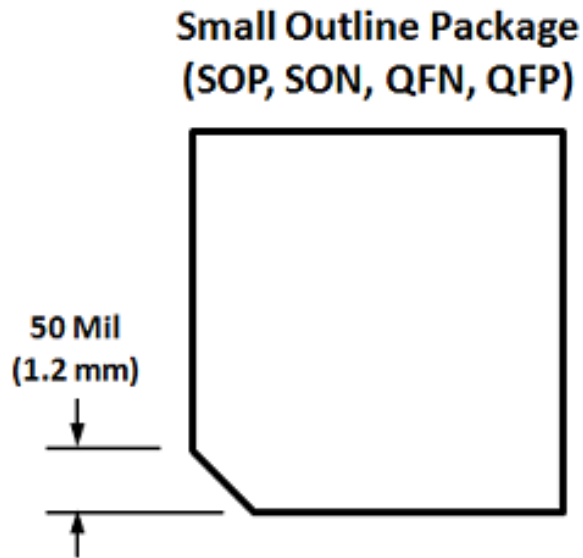
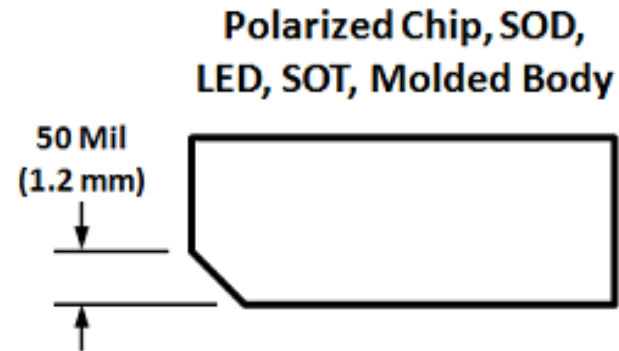
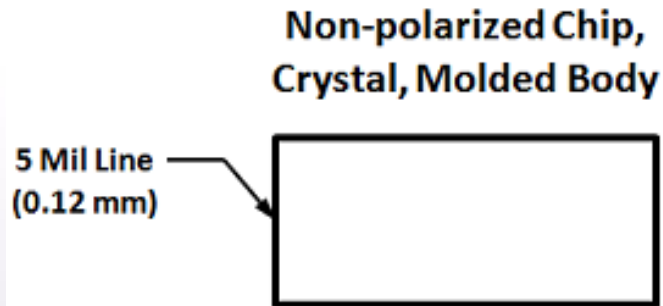
Quad Flat Pack (QFP)



Axial Resistor

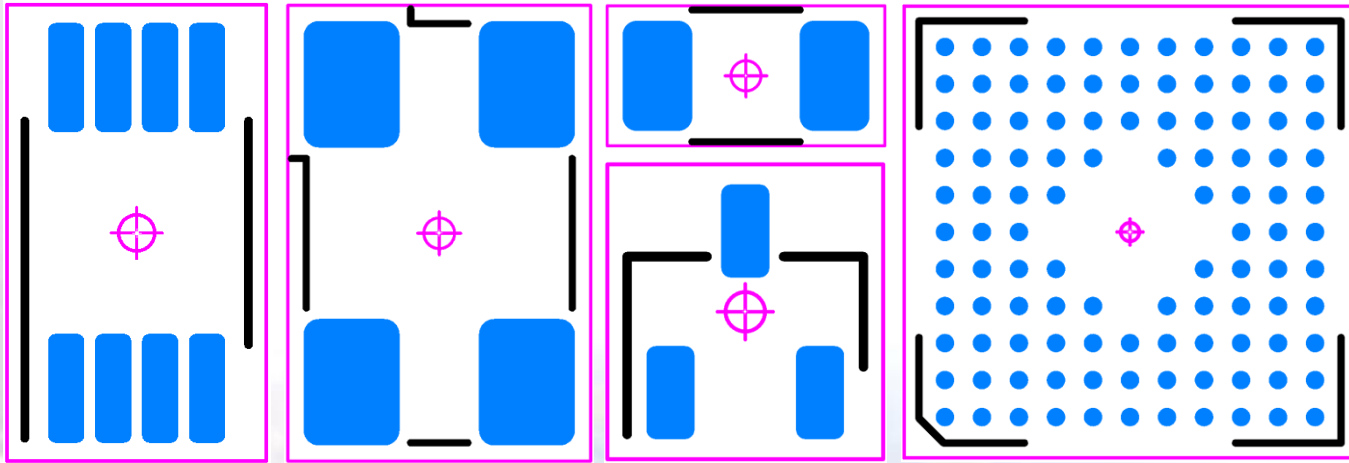


# Assembly Outline Guidelines



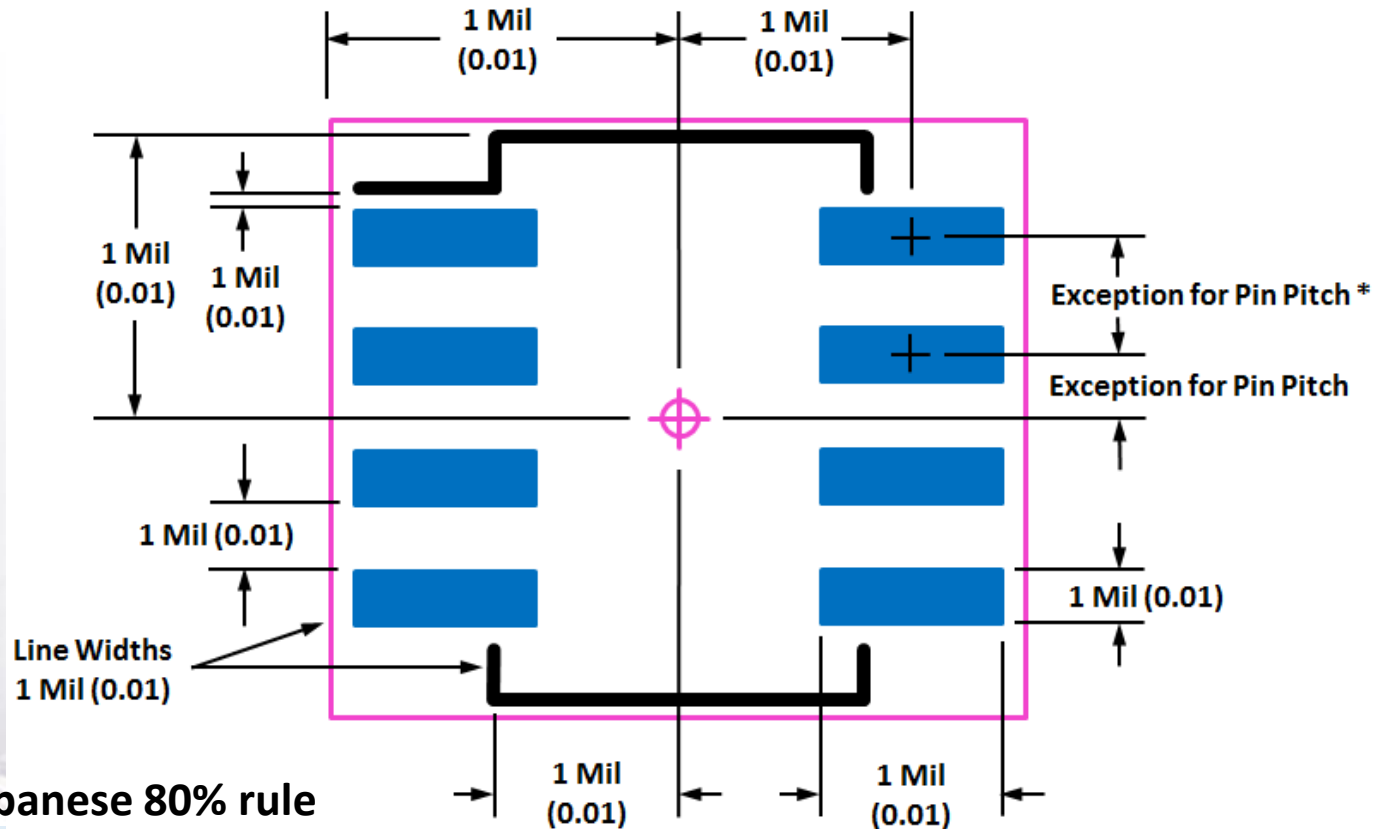
# Land Pattern Origin Guidelines

- The land pattern origin is typically located at the center of gravity of the component, but sometimes this is difficult to calculate with irregular shaped components, so Pin 1 is used in these cases. Also Pin 1 in most through-hole connectors.
- The centroid origin marking in the picture below is an unfilled 20 Mil (0.5 mm) diameter circle with a 1 Mil (0.01) line width with a 32 Mil (0.8) crosshair for cursor alignment.



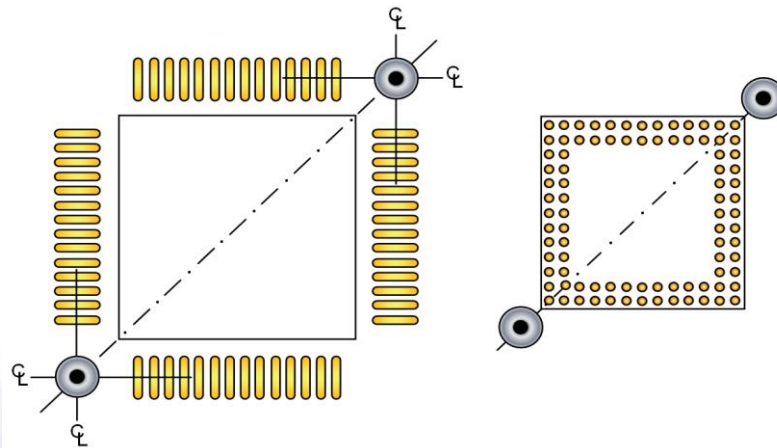
# Snap Grid Round-off 0.01 mm

All Footprint Features are in 1 Mil increments when using Imperial units and 0.01 mm or 0.05 mm Increments when using Metric units



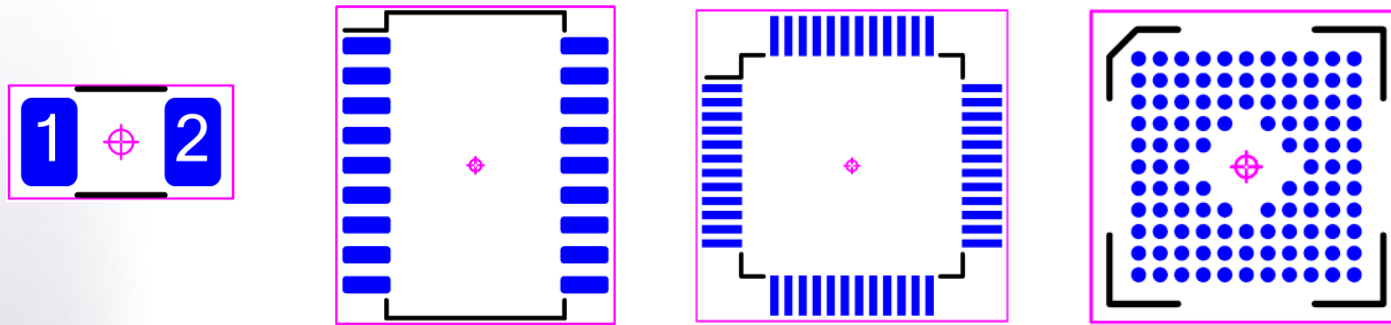
# 3-Tier Local Fiducials

- Local Fiducials have been used only on fine pitch QFP and BGA Land Patterns
  - Fine pitch QFP = Less than 25 mil (0.635 mm) pitch
  - Fine pitch BGA = Less than 32 mil (0.8 mm) pitch
- Future Local Fiducial sizes will be:
  - Level A (Most) = 40 mil (1.0 mm) with 80 mil (2.0 mm) solder mask & keep-out
  - Level B (Nominal) = 30 mil (0.75 mm) with 60 (1.5 mm) solder mask & keep-out
  - Level C (Least) = 20 mil (0.5 mm) with 40 mil (1.0 mm) solder mask & keep-out

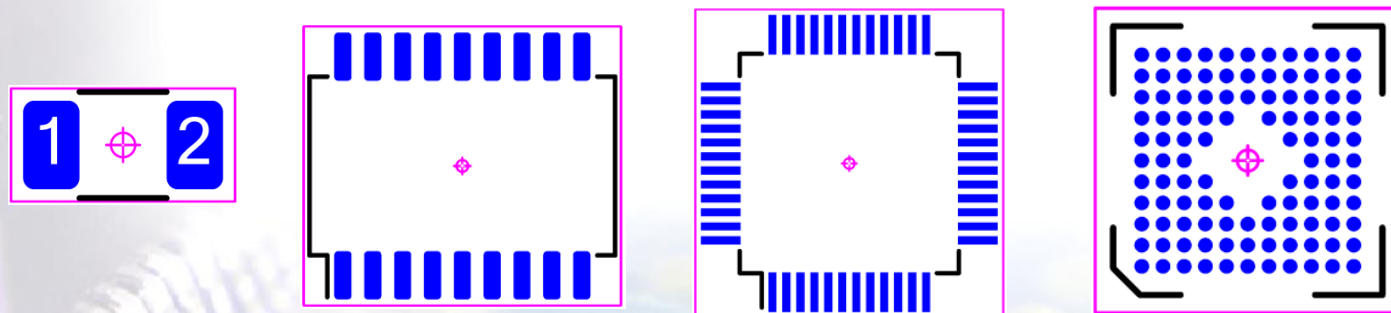


# Zero Component Orientation – Levels A & B

Zero Orientation with Pin 1 in Upper Left Corner Introduced in 2007 in the IPC-7351A Publication – IPC-7351C “**Level A**”

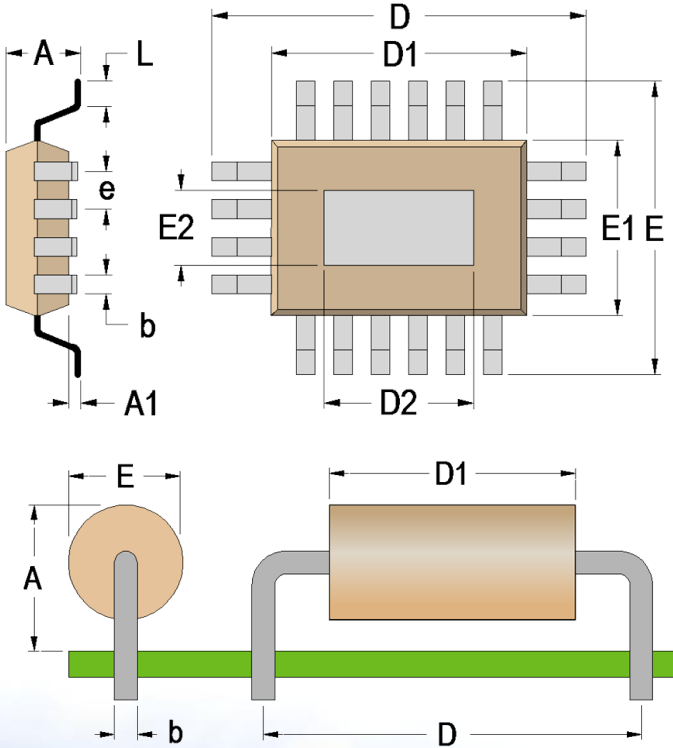
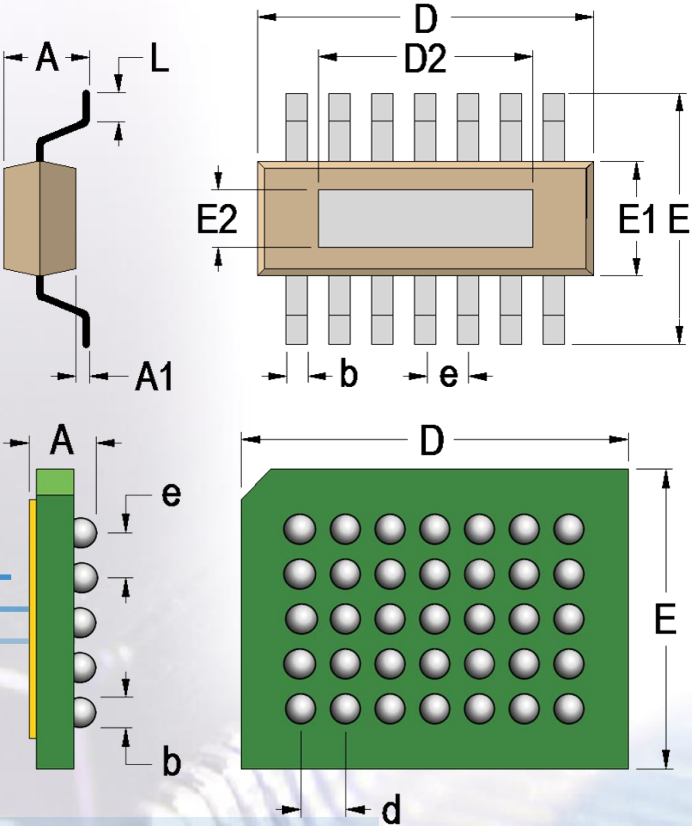


Zero Orientation with Pin 1 in Lower Left Corner Introduced in 2009 in the IEC 61188-7 publication – IPC-7351C “**Level B**”



# EIA & JEDEC

## EIA Component Dimensions vs: JEDEC Dimensional Letters



# Land Pattern Naming Convention

## Extended Names Eliminate Duplication

- The original IPC-7351 footprint naming convention does not include Gull Wing component lead tolerances, Thermal Pad sizes, BGA Ball sizes or various pin assignments into account. Therefore, the same component with different tolerances can produce a different land size and spacing with the same footprint name.
- A footprint name of **SOP50P710X120-14N** can have version A, B, C, D which do not indicate the variances in Thermal Tab or Lead Length
- There are 3 component features that affect the footprint name
  - Square Thermal Tab Size = **SOP50P710X120-14T300**
  - Rectangle Tab Shape = **SOP50P710X120-14T300X500**
  - Gull Wing Lead Length Tolerance = **SOP50P710X120-14L50**
  - BGA Ball Size = **BGA121C50P11X11\_600X600X100B23**
- For component mfr. recommended footprint drop the environment level character after the pin qty. - **SOP50P710X120-14**



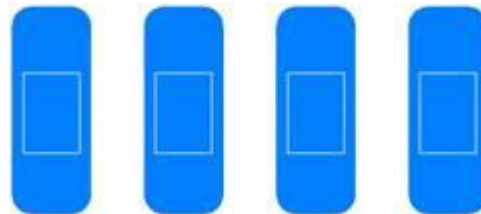
# Solder Joint Goals for Chip Components < 0603

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe ( $J_T$ )	0.55	0.35	0.15
Heel ( $J_H$ )	0.00	0.00	0.00
Side ( $J_S$ )	0.05	0.00	-0.05
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.01, 1.02, 1.03		
Courtyard excess	0.50	0.25	0.12
Rectangular Chip Components Smaller than 1608 (0603) (unit: mm)			
Toe ( $J_T$ ) 0402		0.15	
Toe ( $J_T$ ) 0201		0.12	
Toe ( $J_T$ ) 01005		0.10	
Heel ( $J_H$ )		0.00	
Side ( $J_S$ )		0.00	
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.01, 1.02, 1.03		
Courtyard excess		0.15	

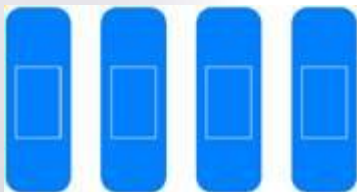
# New Solder Joint Goal Recommendations

- 1.00 mm pitch = 0.35 mm Toe/Heel
- 0.80 mm pitch = 0.33 mm Toe/Heel
- 0.65 mm pitch = 0.31 mm Toe/Heel
- 0.50 mm pitch = 0.29 mm Toe/Heel
- 0.40 mm pitch = 0.27 mm Toe/Heel
- 0.35 mm pitch = 0.25 mm Toe/Heel

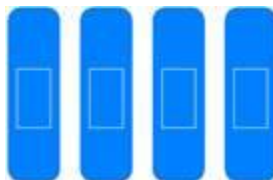
1.00 mm pitch w/0.35 mm Toe/Heel



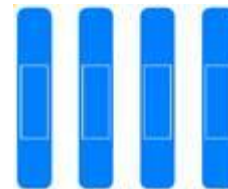
0.80 mm pitch w/0.35 mm Toe/Heel



0.65 mm pitch w/0.35 mm Toe/Heel



0.50 mm pitch w/0.35 mm Toe/Heel



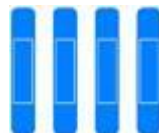
0.40 mm pitch w/0.35 mm Toe/Heel



0.35 mm pitch w/0.35 mm Toe/Heel



0.40 mm pitch w/0.27 mm Toe/Heel



0.35 mm pitch w/0.25 mm Toe/Heel



# Chapters 8 & 9 – Total Rewrite

---

- Component Family Description
- 3D Model Picture of Component
- Land Pattern Pictures with Level A & B Rotations
- Solder Joint Goal Tables
- Common Package Sizes and Case Codes
- Relocating all Assembly Related Data to the new *IPC-7070 Component Mounting Issues and Recommendations*

# PCB Library Expert

Multiple User  
and Company Defined  
Rules & Preferences



FPX Library

The screenshot shows the PCB Libraries EXPERT software interface. It displays a table of components with columns for Name, Description, Category, Manufacturer, Part Number, and Logical Description. A box labeled 'Component Dimensions' is overlaid on the table, highlighting a specific component's dimensions.

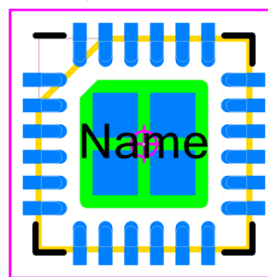
Name	Description	Category	Manufacturer	Part Number	Logical Description
IPC-7351-1-01-01	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-01	High-Resolution Chip Carrier
IPC-7351-1-01-02	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-02	High-Resolution Chip Carrier
IPC-7351-1-01-03	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-03	High-Resolution Chip Carrier
IPC-7351-1-01-04	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-04	High-Resolution Chip Carrier
IPC-7351-1-01-05	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-05	High-Resolution Chip Carrier
IPC-7351-1-01-06	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-06	High-Resolution Chip Carrier
IPC-7351-1-01-07	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-07	High-Resolution Chip Carrier
IPC-7351-1-01-08	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-08	High-Resolution Chip Carrier
IPC-7351-1-01-09	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-09	High-Resolution Chip Carrier
IPC-7351-1-01-10	High-Resolution Chip Carrier, P-20, 1.27mm pitch, 10µm technology	IPC-7351-1-01	IPC	IPC-7351-1-10	High-Resolution Chip Carrier

## DAT Preference Files

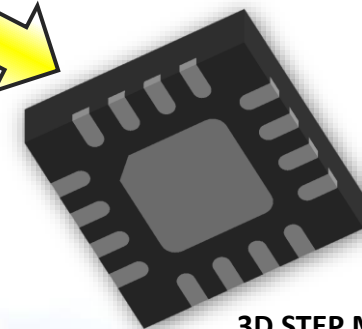
- Imperial or Metric
- Pad shapes
- Component rotations
- Solder joint goals
- Tolerances
- Line widths
- Dozens more!



Print  
Data  
Sheet



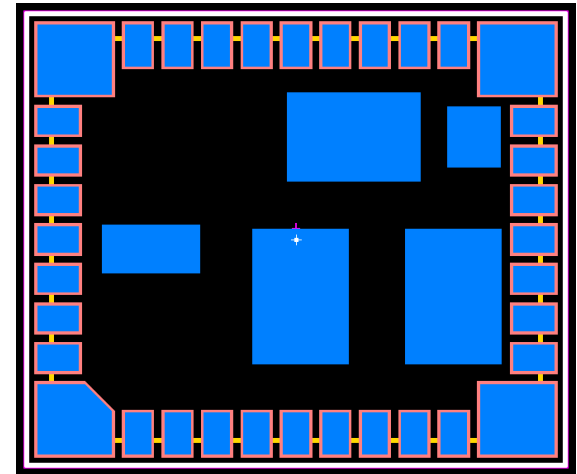
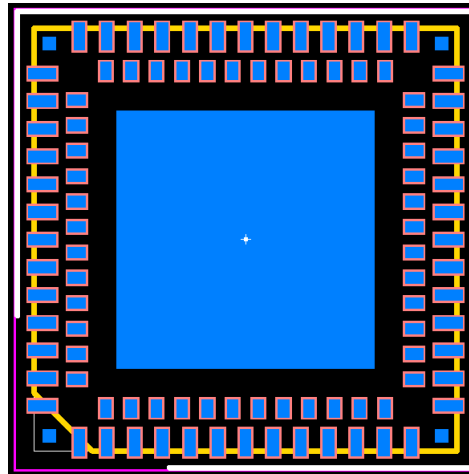
Footprints for  
18 CAD Formats



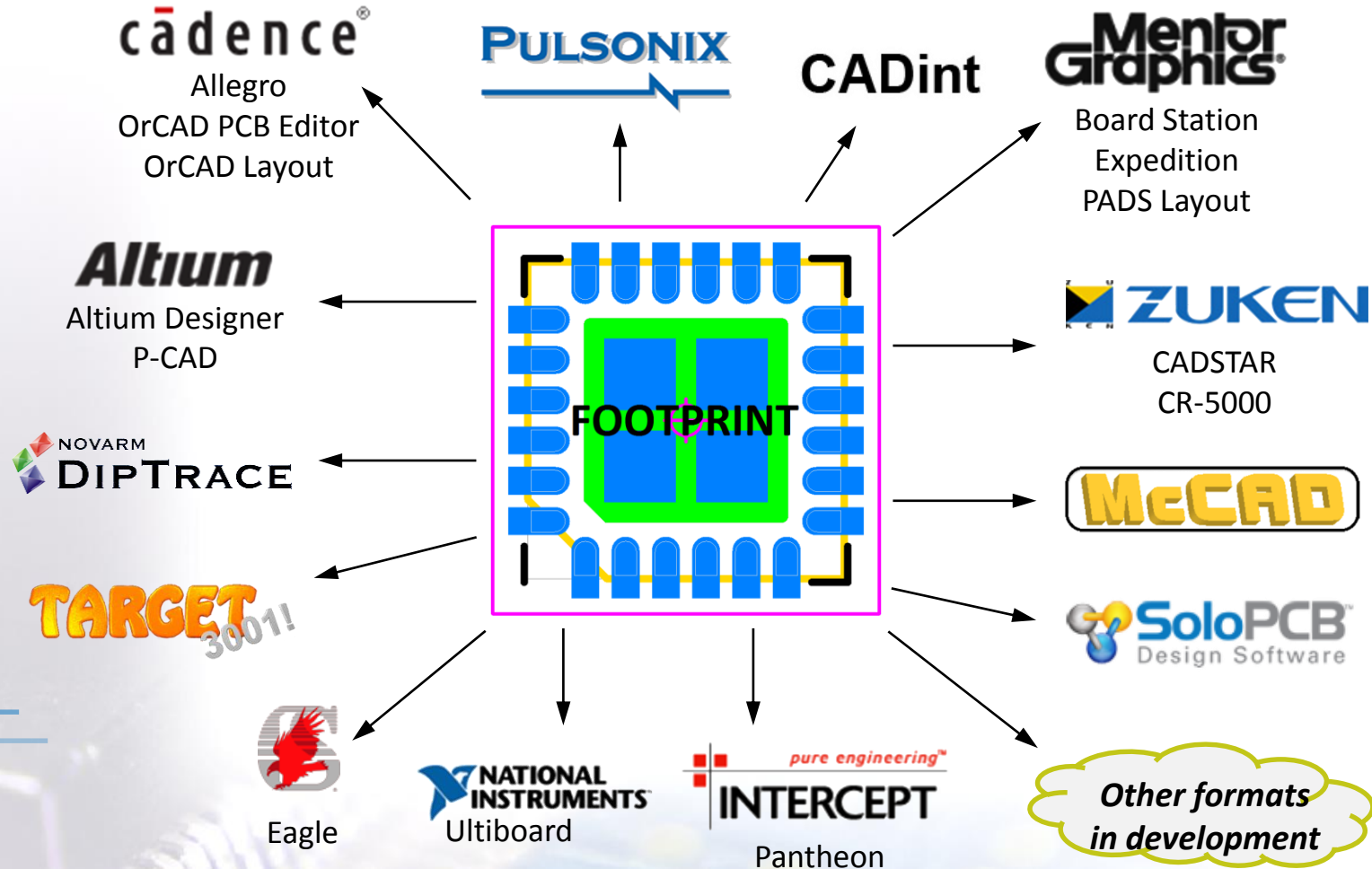
3D STEP Model

# The “Footprint (FP) Designer” Module

- Traditional footprint software only calculates standard parts, constraining usage to only 50% of the components in the industry.
- PCB Library Expert also creates mfr. recommended footprints for components with the following characteristics:
  - Asymmetrical
  - Various sizes of pads
  - Different pad shapes



# PCB Library Expert CAD Tool Interfaces





# *Questions?*

**Tom.Hausherr@PCBLibraries.com**  
**www.pcblibraries.com**

