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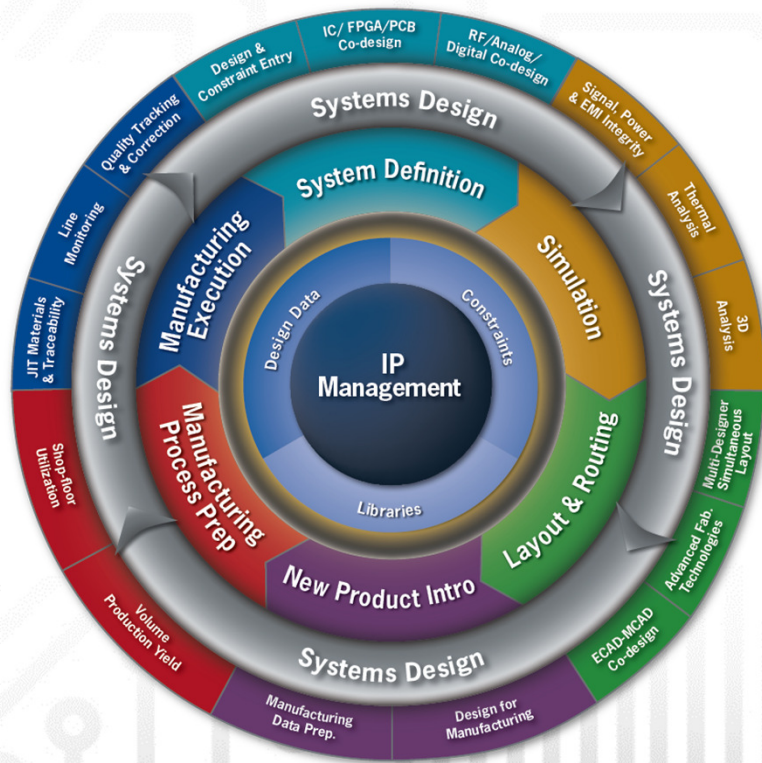
Xpedition Routing Automation Technologies That Drive Routing

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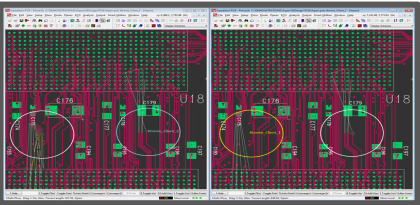
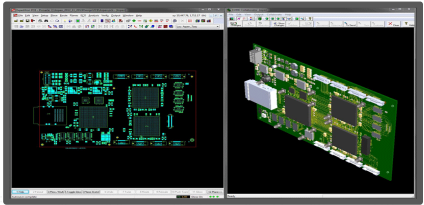
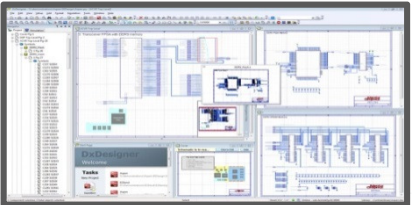
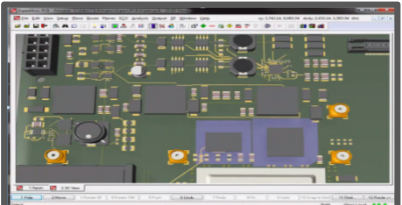
Change The Way You Develop With **xpedition**™

The Next Generation of PCB Systems Design



- ➔ **Full data integrity**
Capturing the design intent once and manage design IP consistently throughout the flow. Improves project schedules, reduces risks and eliminates error-prone manual data manipulation and file based interfaces
- ➔ **Correct-by-design Methodology and Flow Automation**
Can increase engineering productivity by 50% or more by reducing error rate and eliminating time consuming batch post-processes. Productivity increase through unprecedented layout automation
- ➔ **Flow-wide concurrent engineering**
Reduction of 30-60% cycle time and up to 80% decrease in integration effort across disciplines. Enables multiple engineers to work in parallel at any stage of the design process—even from dispersed global locations
- ➔ **Virtual prototyping and 3D design**
Cuts down costly and time-consuming physical prototypes, freeing up resources for cost and quality optimization by improving electrical, thermal and electromechanical design quality and reliability
- ➔ **Integrated design-through-manufacturing**
Eliminate new product introduction risks by reducing design spins by 60% or more, and optimizing first pass yield by integrating the design chain with the extended supply chain

The Xpedition Evolution

2005	2007	2009	2013
<p>Expedition Enterprise 2005</p> <p>Integrated flow for schematic & layout</p>	<p>Expedition Enterprise 2007</p> <p>Migrating to a full concurrent architecture</p>	<p>Expedition Enterprise 7.9.x</p> <p>Mainstream deployment</p>	<p>Xpedition Enterprise VX</p> <p>Meeting the demands of modern development organizations</p>
			

Capturing and Managing Design Intent Throughout the Entire Flow

- Single & Integrated Constraint System
- Scalable, Easy To Use
- Integrated with SI/PI Analysis Tools
- Concurrent

Table 1-1. ICES Show-Me Movies

Task	Show-Me Movie
Viewing Clearance Constraints (New for EE 7.9.3!)	
Viewing and Changing Match Group Contents (New for EE 7.9.3!)	
Viewing Trace Width Constraints (New for EE 7.9.3!)	
Viewing and Changing Constraint Values	
Comparing Front-End and Back-End Constraint Values	
Comparing Constraints to a Target Constraint Value	
Viewing Differential Pair Constraints	

Flow Wide Concurrent Design

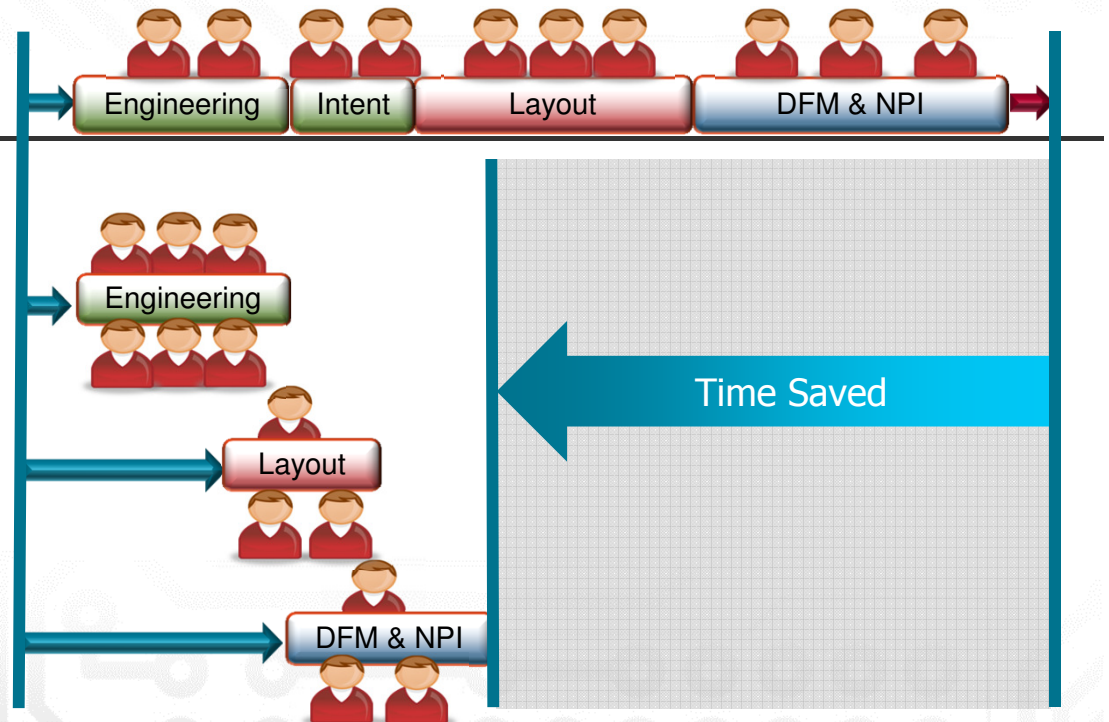
Shorten Design Cycles, Reduce Spins

Traditional process

- Serial engineering

Xpedition concurrent design flow

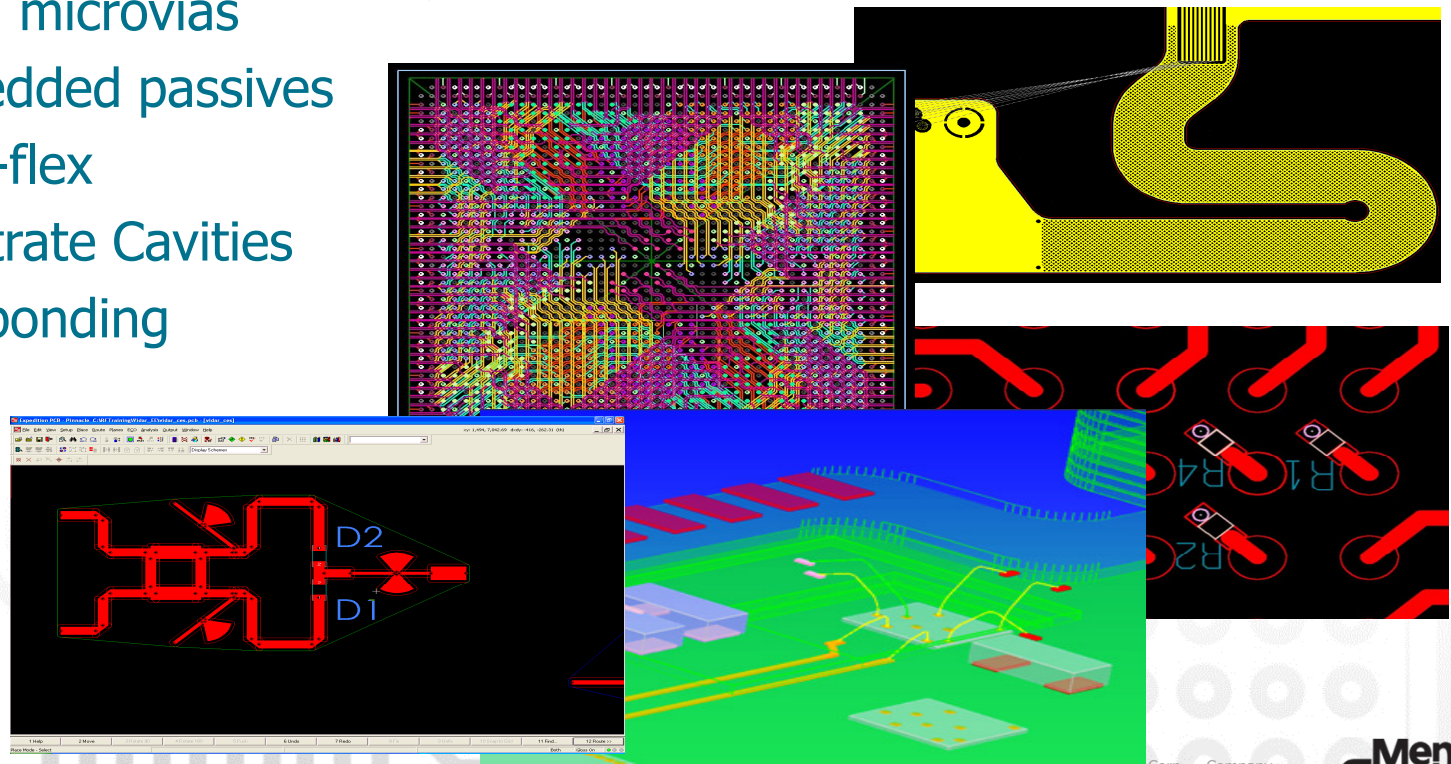
- Concurrent tasks
- Concurrent designers in each task



“Concurrent design is an indispensable tool for faster design cycle time – we successfully reduced it by as much as 65%.”

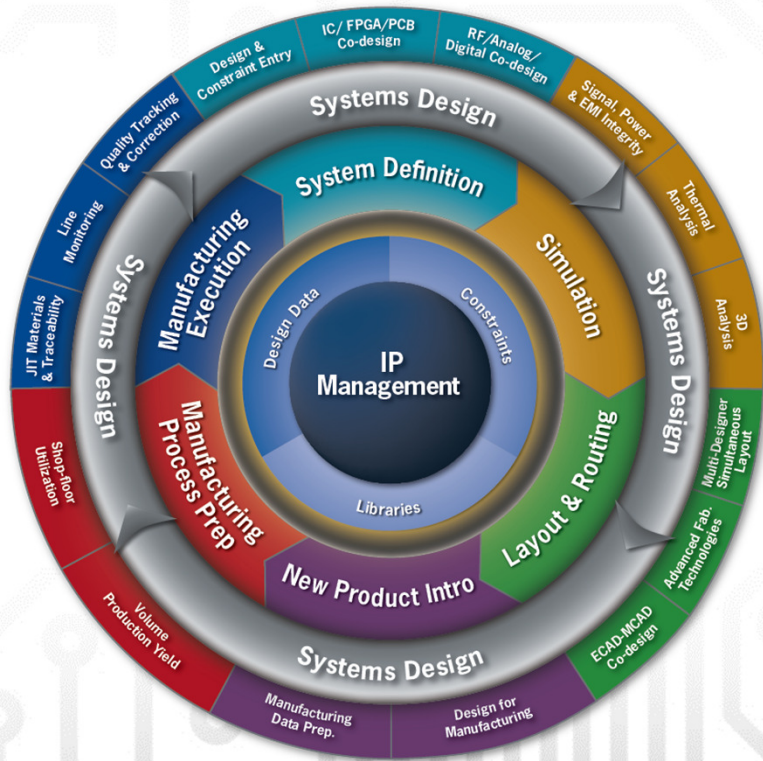
Addressing Advanced Packaging & Design Complexity

- Support for advanced fabrication & assembly technologies
 - HDI / microvias
 - Embedded passives
 - Rigid-flex
 - Substrate Cavities
 - Wirebonding
 - RF



xpedition™ Key Differentiators

The Next Generation of PCB Systems Design



- ➔ Ease-of-use throughout the flow
- ➔ Integration from System to Board to Chip
- ➔ Design-through-manufacturing
- ➔ Higher Productivity through Routing Automation
- ➔ Complete 3D Design Environment
- ➔ Flow Wide Concurrent Design
- ➔ Advanced virtual prototyping

Integration from System to Board to Chip

Automating Board and Multi-Board Design Optimization

The collage displays four key design tool interfaces:

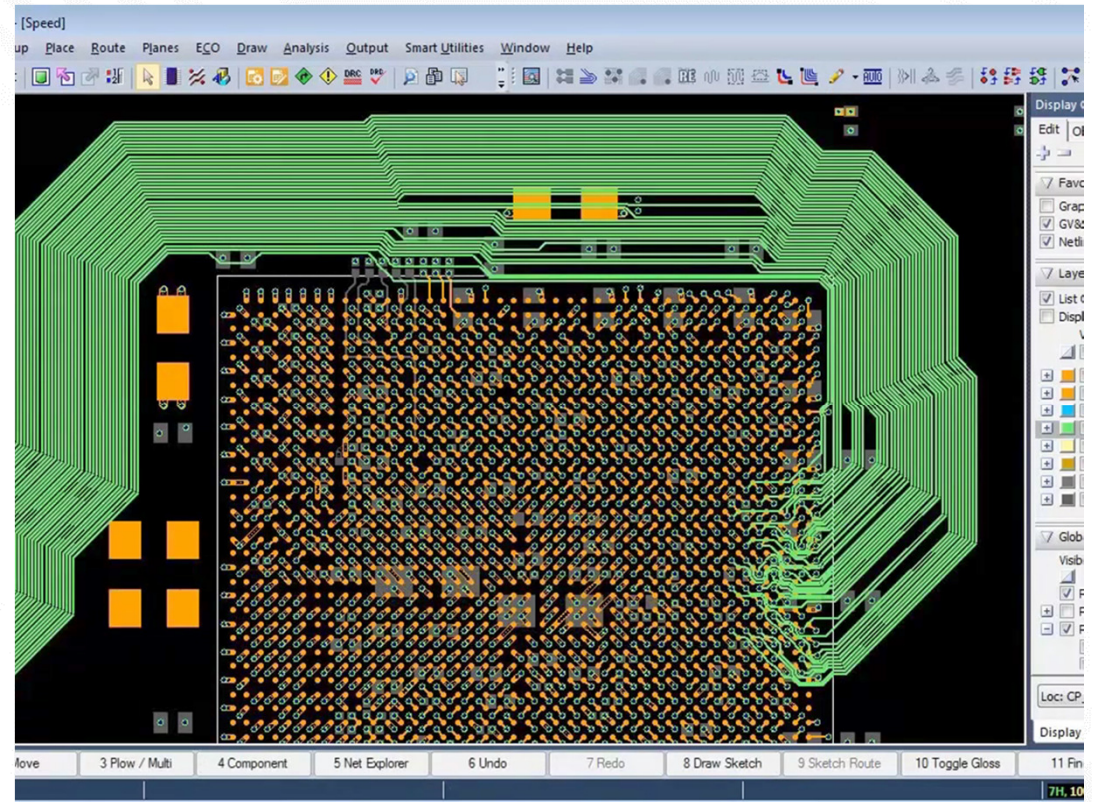
- System Block Diagram:** Shows a high-level system architecture with blocks for Sensor Inputs, Relays, Data Acquisition, Data Distribution, and ADC/DAC Blocks.
- Pin Assignment Table:** A table listing pins and their assignments. Below is a partial view of the table:

Pin	Assignment	Direction	Level
E7	PA0713	Q_DATA<27>	IO LV
A7	PA0692	Q_DATA<25>	RES. LV
H9	PA0628	Q_DATA<25>	IO LV
C18	PA0772	Q_DATA<24>	IO LV
K18	PA0781	Q_DATA<22>	IO LV
L6	PA0647	Q_DATA<22>	IO LV
J32	PA015	Q_DATA<21>	IO LV
C8	PA0623	Q_DATA<20>	RES. LV
R7	PA0559	Q_DATA<19>	IO LV
R7	PA0522	Q_DATA<18>	IO LV
AH54	PA0189	Q_DATA<17>	IO LV
C8	PA0902	Q_DATA<16>	RES. LV
C1	PA0688	Q_DATA<15>	IO LV
A80	PA0558	Q_DATA<14>	IO LV
AH85	PA0181	Q_DATA<13>	IO LV
AA10	PA0561	Q_DATA<12>	IO LV
AF6	PA0518	Q_DATA<11>	IO LV
FT7	PA0786	Q_DATA<10>	IO LV
H18	PA0695	Q_DATA<9>	IO LV
- Routing Grid:** A grid showing a complex network of red routing paths connecting various components.
- Rule Editor:** A window for defining design rules, showing a list of rules and their descriptions.

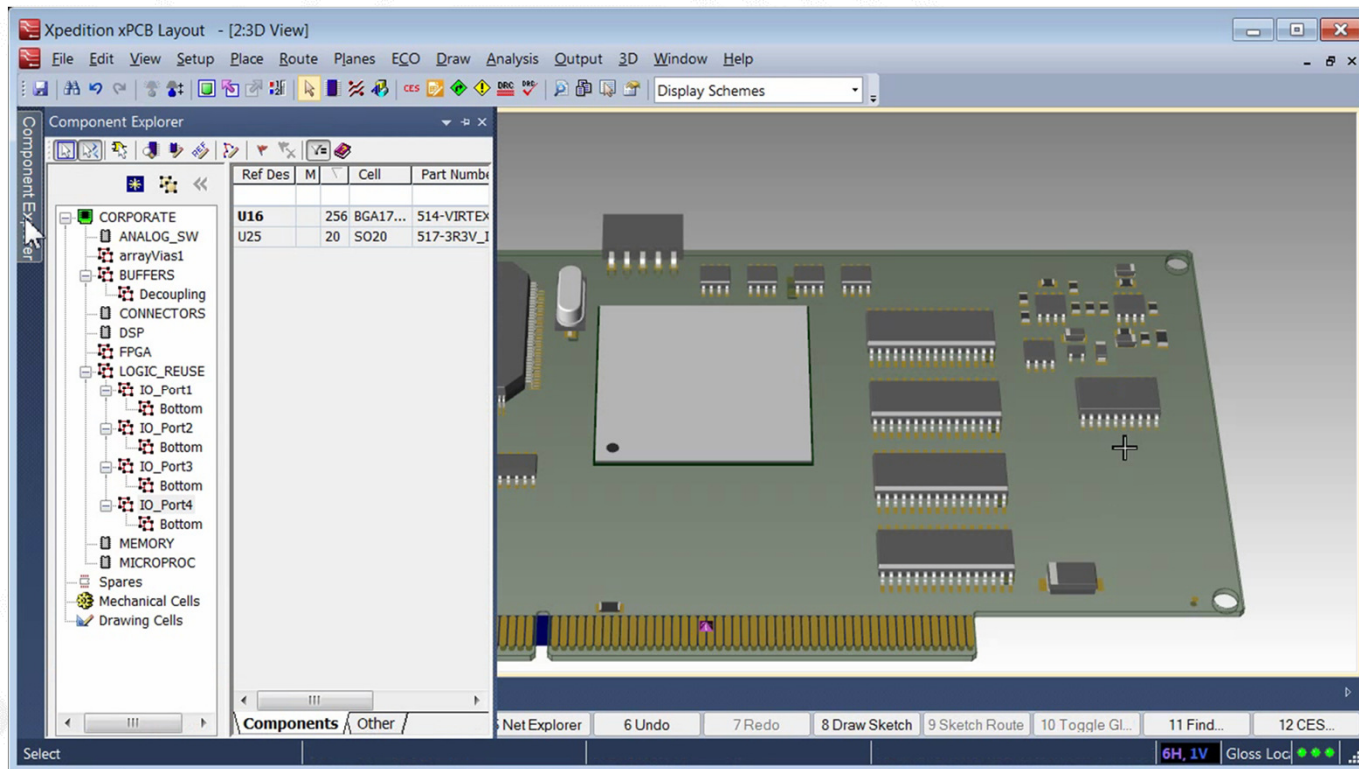
- ⊕ Multi-board system definition
- ⊕ FPGA/PCB co-design
- ⊕ Cross-domain path finding

Xpedition Routing Automation – Sketch Router

- User control
 - Manage location of traces
 - Options for route styles
 - Choose via patterns
- Route quality
 - Matches quality of manual routing
 - Rarely needs clean-up
- High performance
 - Unbelievably fast



New Hierarchical Planning and Placement Complete 3D Design Environment



Xpedition Enterprise – The Forefront of Innovation and Productivity in Electronics Design and Manufacturing

- Find out More about Mentor's Groundbreaking Technology
<http://tinyurl.com/Sketchrouting>
- Visit us online
www.mentor.com/pcb/xpedition
www.youtube.com/MentorXpedition
- Contact us directly: xpedition_questions@mentor.com

Demo

The logo for Mentor Graphics, featuring the word "Mentor" in a bold, red, sans-serif font above the word "Graphics" in a similar bold, red, sans-serif font. A registered trademark symbol (®) is located to the upper right of "Graphics".

**Mentor
Graphics®**

The logo for xpedition, featuring a red 'x' icon followed by the word "pedition" in a black, sans-serif font. A trademark symbol (™) is located to the upper right of "pedition".

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