# **E**.surface



Orange County Chapter

March 11<sup>th</sup>, 2014

Presented by: Alex S. Richardson VP Strategic Operations - eSurface Managing Director - Advanced Circuitry & Electronics Division

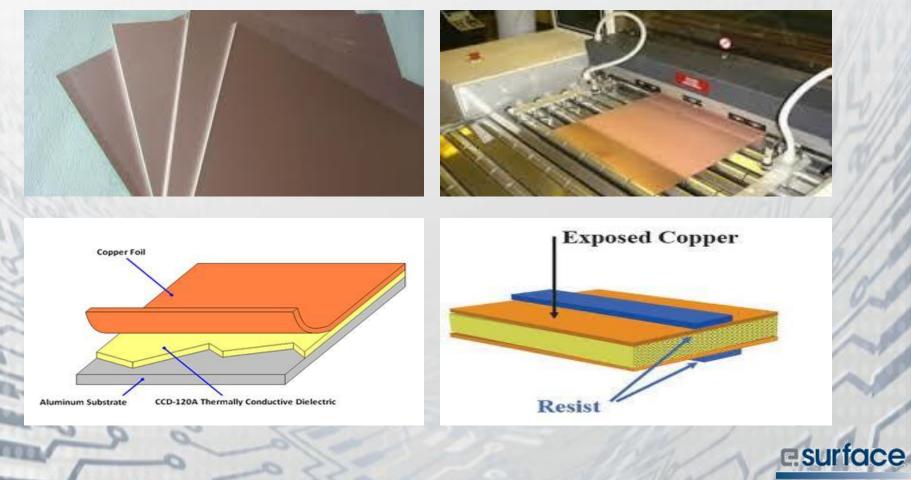


"Comparison of current Print & Etch process to eSurface"

- 1. Overview of Print & Etch Process
- 2. Practical limitations of reductive processes
- 3. Overview of eSurface process
- 4. Benefits of eSurface
- 5. Potential applications & adoption paths for eSurface
- 6. Impact to industry
- 7. Contact Information



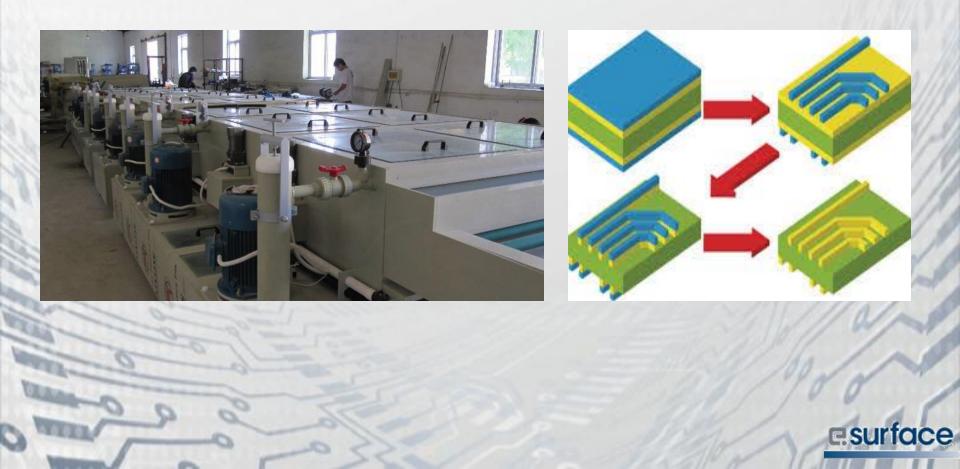
Current process methodologies include utilizing clad materials where several redundant dry film, develop and etch processes are utilized.



Clad substrates typically come in standard (limited) Cu foil options which then need sequential processing (etching and selective plate) to achieve correct requisite plating

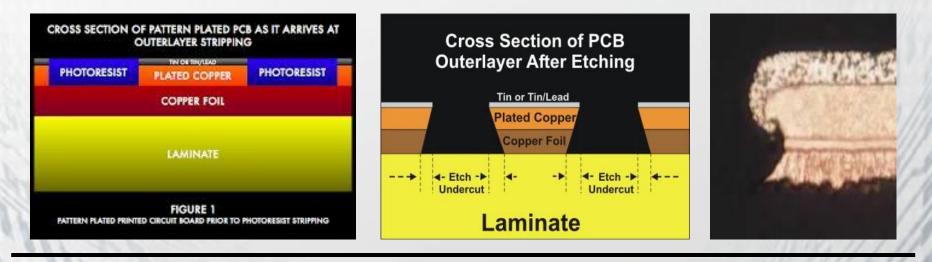


This process can require in excess of 20 process steps per panel, many which use caustic chemistries, having significant variables, causing poor yields in advanced designs



## PCB Print & Etch (Subtractive) Process

Over etching is common in fine features and typically non-recoverable. Poor yields drive cost structures to unacceptable levels and unpredictable process /lead-times with many production restarts.



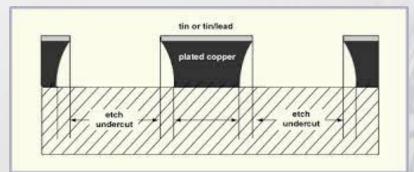
We have many tools that can design and analyze requisite circuitry that exceed todays print and etch manufacturability.

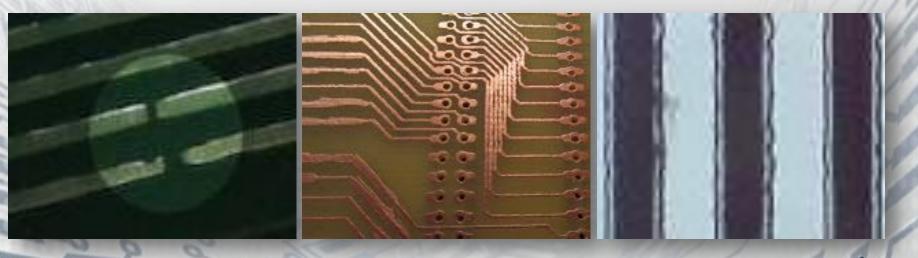
Put simply...the industry can out-design what is currently reliably and effectively produce-able...

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The results in fine features is typically scalloped edges on circuitry, lost or broken traces, and low yields rates:

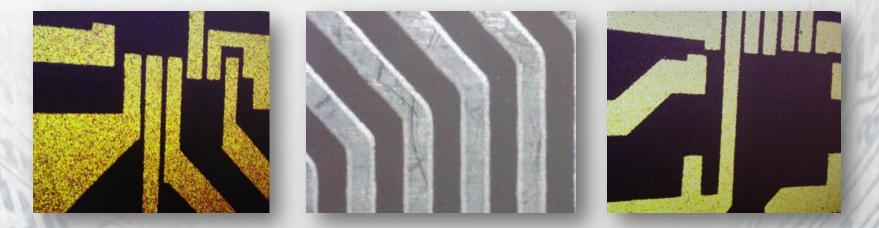
LW/LS in mils	Corresponding Yields
3/3	90-98%
2/2	45-65%
<2/2	5-20%
1/1	low single digit %





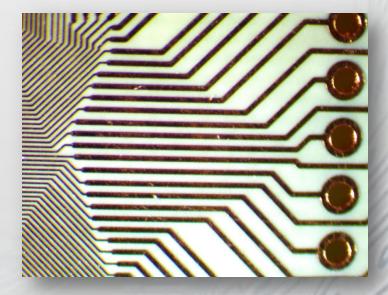


eSurface is an additive process overcoming long sought-after solutions with adhesion typically experienced in historical additive approaches.

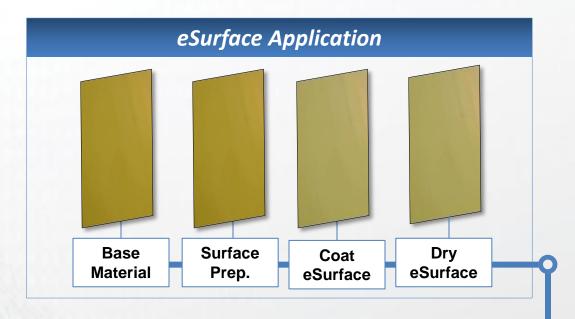


This revolutionary new and innovative technology affords a *covalent bond* and more efficient process resulting in controlled fine feature resolution and enables repeatable manufacturability. "eSurface" is a transformational technology and its process is a unique and fundamental invention in the evolution of the electronics industry that will allow companies to build electronics cheaper, smaller, faster, lighter, and more functional.

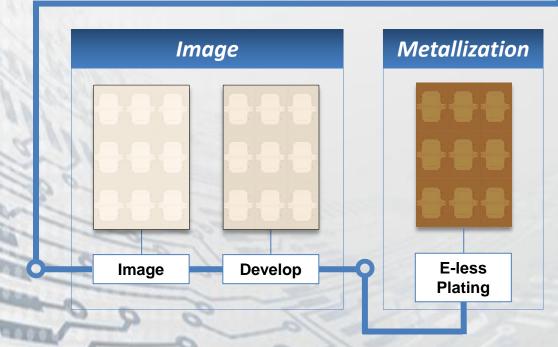
- Disruptive Technology
- More versatile
- More robust
- Less expensive
- Enables new innovation







eSurface process is comprised of four process steps, all of which can be accomplished with standard equipment and processes.

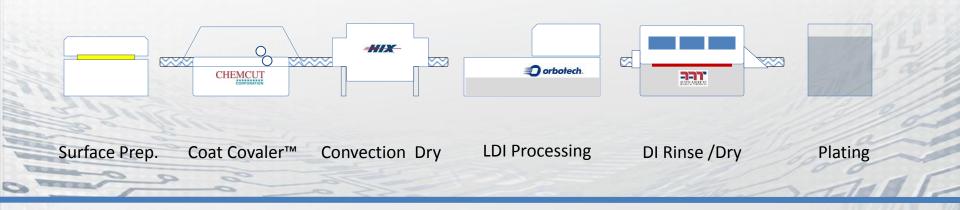


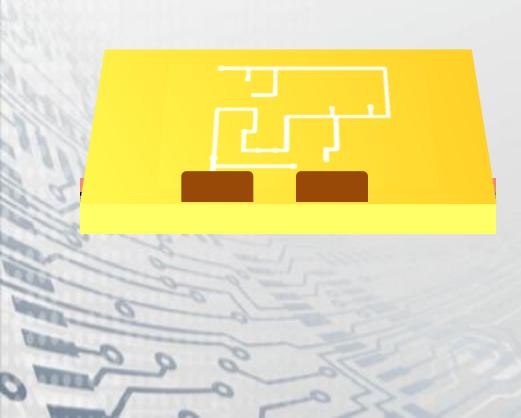
**Unclad material** 

- 1) Surface Preparation
- 2) Apply eSurface/ Dry
- 3) Image
- 4) Develop (D.I. Rinse)

Metallization

#### eSurface – Manual Production line





Unclad Material

- 1. Surface Activation
- 2. Coat unclad with *eSurface Covaler*<sup>™</sup>

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- 3. Dry
- 4. Image
- 5. DI water rinse / Dry
- 6. Electroless metallization

## eSurface

# **Covaler Application**

( I J DI



## eSurface

## **Developer -** Deionized Water Rinse/Dry



## eSurface Competitive Advantages

## **Immediately Eliminates:**

- X Copper Foil
- X Copper Foil Lamination
- X Dry film Photo Resist
- X Dry Film Lamination
- X <del>Developer</del>
- X Etchant
- X Stripper
- X Spent Etchant and Stripper Waste collection
  - Spent Etchant and Stripper Waste Remediation



#### Cross Section of eSurface Cu Plated Circuit



✓ Substrate material: FR4 IPC 4101/24 - .005" thick.
✓ Copper plated circuit thickness: .0016"
✓ Controlled Horizontal growth of the trace during build up

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## eSurface Competitive Advantages

## **Increased Manufacturing Efficiencies:**

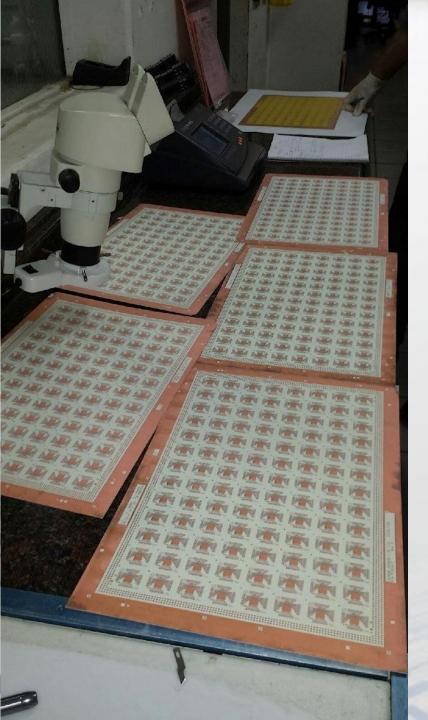
- Reduces production steps
- Shortens turn times
- Improves yield
- Lowers direct production costs
- Reduced hazardous waste and remediation costs

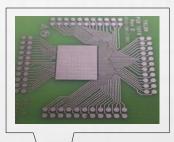


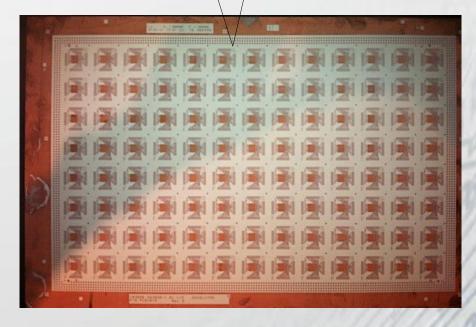
### eSurface Competitive Advantages

## **Increased Manufacturing Capabilities:**

- Circuit trace line width and spacing ≤ 25 microns
- Thin metallization < 2 microns (build to actual spec.)
- Simplify board layout and routing
- Reduce PCB size, thickness and weight
- Add functionality on fixed form factors
- HDI Microelectronics

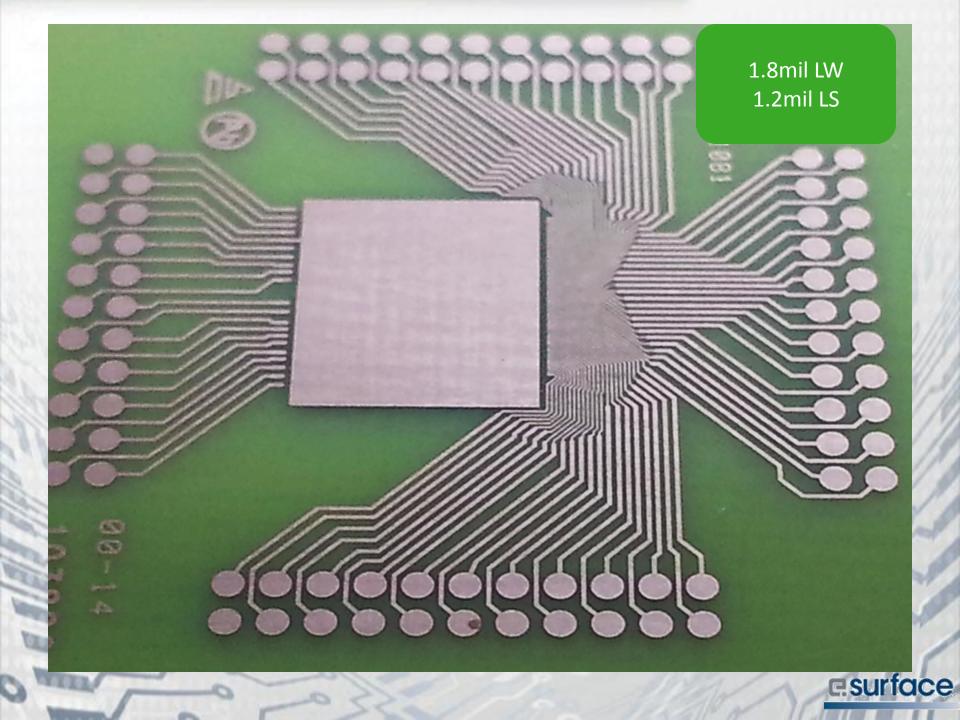


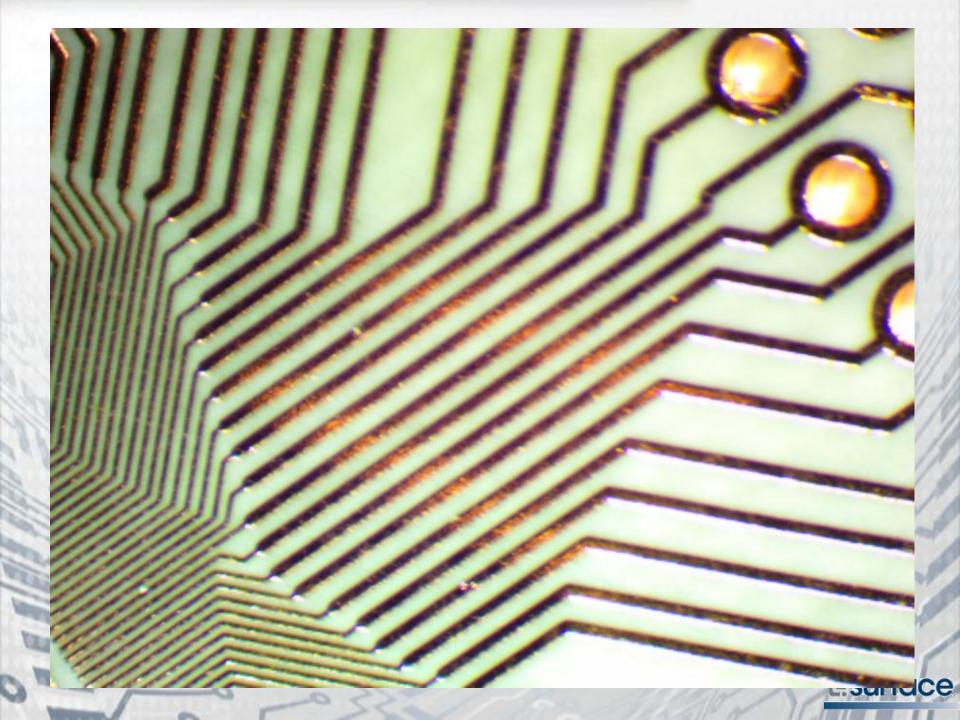


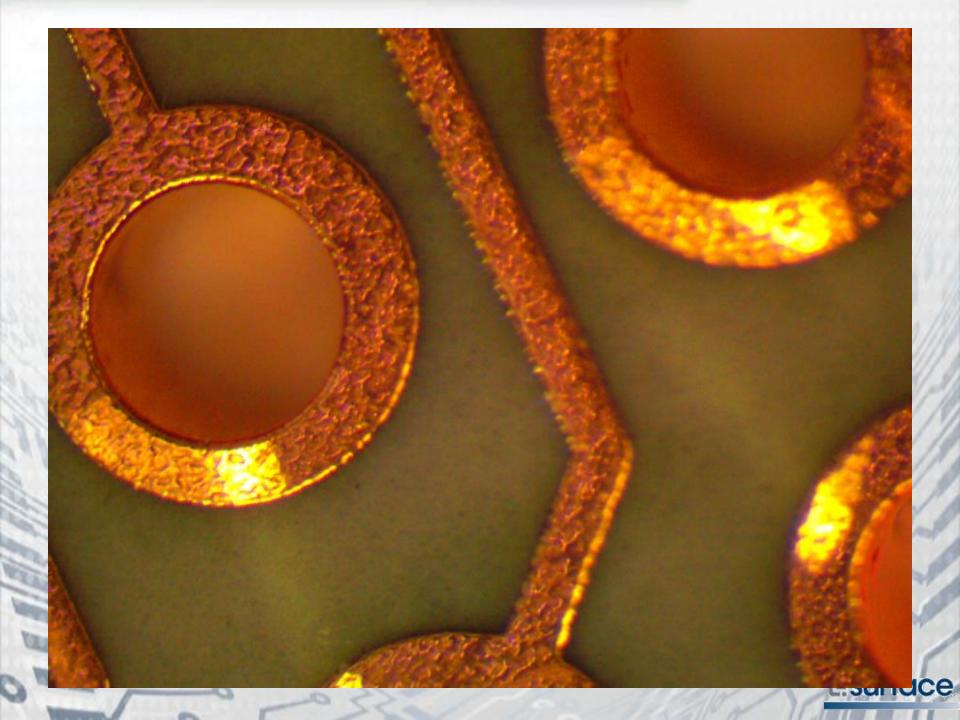


Advanced Technology Design, featuring .0018" trace width and .0012" spacing. Processed on a 12"x18" panel in 104 part array. AOI passed, peel test passed.

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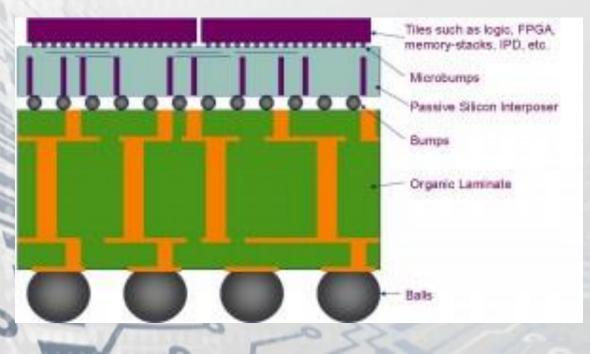


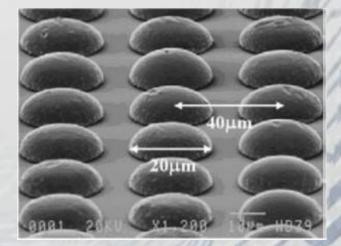
eSurface takes PCB design opportunity to the next level.

Processing risks on fine feature processing are virtually eliminated.

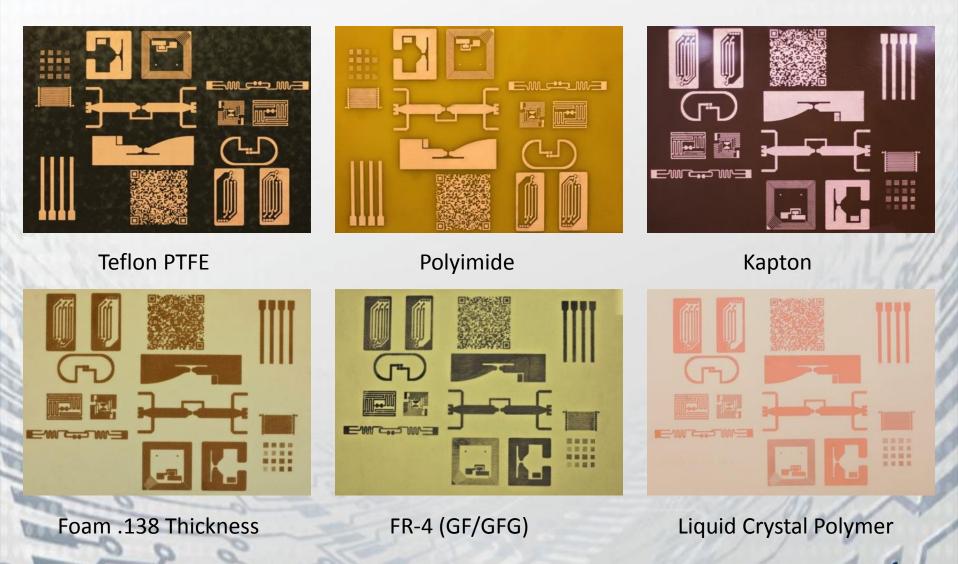
Improvement on HDI to transform interposers and packaging to board level. Onboard uBGA fan outs <.4mm pitch, TSVs, LGA / CSP micro bumps (memory, ASICS, FPGAs, etc...) candidates to be direct mount to PCB. New material selection opportunities for TCE challenges.

Imagine migrating from CSP to CSB!





## eSurface – conventional, exotics and novel materials



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## *eSurface* – representative Adhesion/Peel Strength

IPC 4101/24 FR-4 (GF/GFG) Woven e glass/epoxy				
Test Description	Standard	Test Result		
After 1 hour bake at 250 C⁰	4.00 lbs/in.	Sample 1- 6.00 psi		
		Sample 2- 6.00 psi		
After 550ºF Solder Float	6.00 lbs/in	Sample 1- 8.00 psi		
		Sample 2- 6.00 psi		
After Solvents, A, B, and C	4.57 lbs/in	Sample 1- 6.00 psi		
		Sample 2- 6.40 psi		

IPC 4204/11 Kapton, Copper Cl	ad Adhesiveless Po	olyimide	
Test Description	Standard	Test Result	
After 1 hour bake at 250 C <sup>o</sup>	6.00 lbs/in.	Sample 1- 7.00 psi	1
2. Ma		Sample 2- 7.00 psi	On
After 550ºF Solder Float	6.00 lbs/in	Sample 1- 8.00 psi	2
	1.	Sample 2- 8.00 psi	
After Solvents, A, B, and C	6.00 lbs/in	Sample 1- 8.00 psi	Y
5000		Sample 2- 8.00 psi	1
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- ✓ Finer features only limited to exposure application
- ✓ Covalent bond with superior bonding / adhesion
- ✓ New material selections and combinations of bonded materials
- ✓ Controllable and recoverable process for deposition
- ✓ No high temperature processes or chemistries volatile to substrates
- Unrestricted shapes of patterning metalized objects
- Eco friendly with no caustic chemistries or required permitting
- Significantly less processes, affording faster processing cycle time
- Less variables and more control equating to repeatable high yields
- Enables advanced new designs with greater density



# **E**.surface

For additional information please Contact:



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